8-Channel analog multiplexer/demultiplexer 74LV4051

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 6.0 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Low typ "ON" resistance: 50 Ω at V_{CC} - V_{EE} = 4.5 V 70 Ω at V_{CC} - V_{EE} = 3.0 V 120 Ω at V_{CC} - V_{EE} = 2.0 V**
- **Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals**
- **Typical "break before make" built in**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV4051 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4051.

The 74LV4051 is a 8-channel analog multiplexer/demultiplexer with three digital select inputs (S_0 to S_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S_0 to S_2. With $\overline{E}$ HIGH, all switches are in high impedance OFF-state, independent of S_0 to S_2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	22	ns
t_{PHZ}/t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}		19	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	22	pF
C_s	maximum switch capacitance independent (Y) common (Z)		5 25	pF pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_s = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4051N	16	DIL	plastic	DIL16/SOT38Z
74LV4051D	16	SO	plastic	SO16/SOT109A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
3	Z	common input/output
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_0 to S_2	select inputs
13, 14, 15, 12, 1, 5, 2, 4	Y_0 to Y_7	independent inputs/outputs
16	V_{CC}	positive supply voltage