

8-BIT SINGLE-CHIP MICROCONTROLLER

The μ PD78P098A is a member of the μ PD78098 subseries in the 78K/0 series and is provided with a one-time PROM to which a program can be written only once, or an EPROM to which a program can be written, erased, and rewritten.

Because a program can be written by the user, the μ PD78P098A is ideal for evaluation of a system under development, small-scale production of a variety of systems, and early start of production of a system.

The EPROM model of the μ PD78P098A does not have a reliability level intended for mass production of user systems. Use this model only for evaluation of functions in experiments or trial production of a system.

The functions are explained in detail in the following manuals. Be sure to read these manuals when designing your system.

μ PD78098 Subseries User's Manual : IEU-1381
78K/0 Series User's Manual - Instruction: IEU-1372

FEATURES

- Pin-compatible with mask ROM model (except V_{PP} pin)
- Internal PROM: 60K bytes^{Note 1}
 - μ PD78P098AGC-3B9 : Programmable only once (ideal for small-scale production)
 - μ PD78P098AKK-T : Re-programmable (ideal for system evaluation)
- Internal high-speed RAM : 1024 bytes
- Buffer RAM : 32 bytes
- Internal expansion RAM : 2048 bytes^{Note 2}
- Operating voltage same as mask ROM model ($V_{DD} = 2.7$ to 5.5 V)
- Supports QTOP™ microcontroller

Notes 1. The internal PROM capacity can be changed by using the memory size select register.

2. Internal expansion RAM capacity can be changed by using the internal expansion RAM size select register.

Remark "QTOP microcontroller" is a generic name for one-time PROM-containing microcontrollers totally supported by NEC's writing service (writing, marking, screening, and inspection).

The μ PD78P098A differs from the mask ROM model in the following points:

- The memory can be mapped in the same manner as the mask ROM model by using the memory size select register and internal expansion RAM size select register.
- The P60 through P63 pins are not provided with pull-up resistors.

In this document, the functions common to the one-time PROM model and EPROM model are referred to as "PROM".

The information in this document is subject to change without notice.

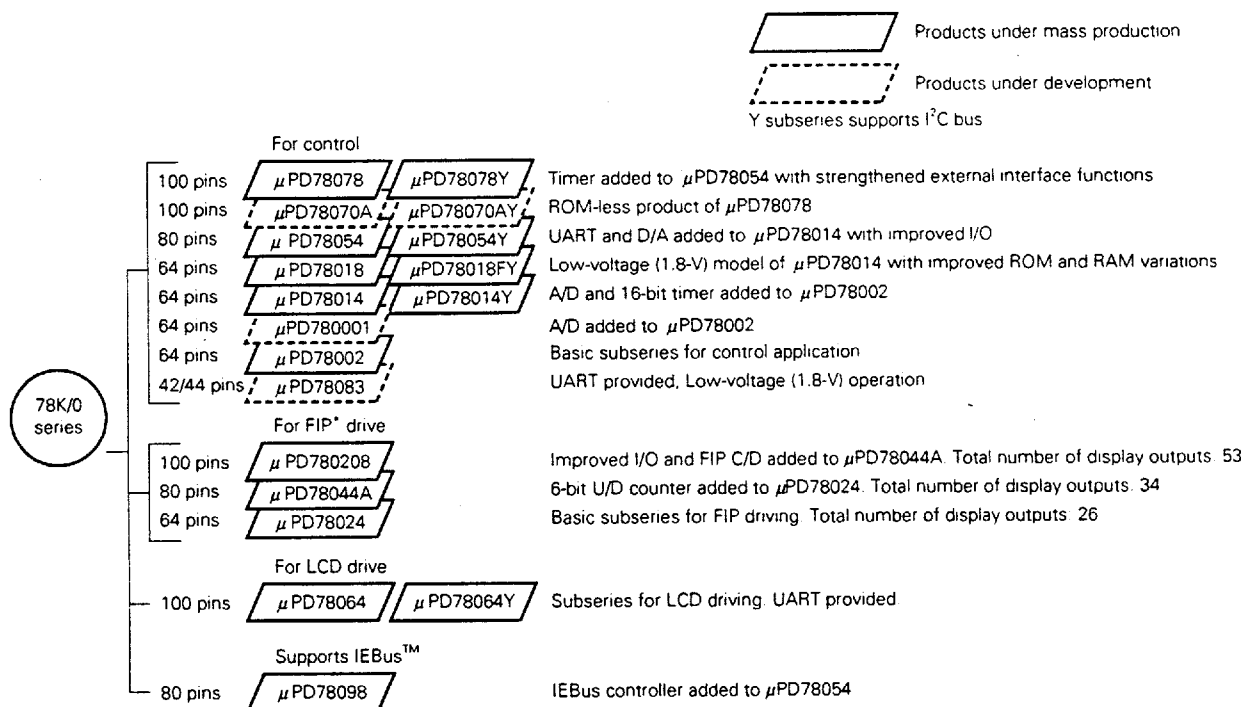
ORDERING INFORMATION

Part Number	Package	Internal ROM	Quality Grade
μ PD78P098AGC-3B9	80-pin plastic QFP (14 × 14 mm)	One-time PROM	Standard
μ PD78P098AKK-T	80-pin ceramic WQFN (14 × 14 mm)	EPROM	Not applicable

Please refer to "Quality Grades of NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Development of 78K/0 Series

The following figure shows the product development of the 78K/0 series. Enclosed in boxes are subseries names. The major functional differences among the respective subseries are as follows:



Function Subseries Name		ROM Capacity	Timer				8-Bit A/D	8-Bit D/A	Serial Interface	I/O	V _{DD} MIN.	External Expansion
			8-bit	16-bit	Watch	WDT						
For control	μPD78078	32K-60K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	88	1.8 V	○
	μPD78070A	-	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	61	2.7 V	
	μPD78054	16K-60K								69	2.0 V	
	μPD78018F	8K-48K								53	1.8 V	
	μPD78014	8K-32K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	53	2.7 V	○
	μPD780001	8K								39	1.8 V	
	μPD78002	8K-16K								53	2.7 V	
	μPD78083	-								33	1.8 V	
For FIP drive	μPD780208	32K-60K	2ch	1ch	1ch	1ch	8ch	-	2ch	74	2.7 V	-
	μPD78044A	16K-40K	2ch	1ch	1ch	1ch	8ch	-	2ch	68	2.7 V	
	μPD78024	24K-32K								54	2.7 V	
For LCD drive	μPD78064	16K-32K	2ch	1ch	1ch	1ch	8ch	-	2ch (UART:1ch)	57	2.0 V	-
Supporting IEBus	μPD78098	32K-60K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	69	2.7 V	○

Functional Outline

Item		Function
Internal memory		- PROM : 60K bytes^{Note 1} - RAM - Internal high-speed RAM : 1024 bytes - Buffer RAM : 32 bytes - Internal expansion RAM : 2048 bytes^{Note 2}
Memory space		64K bytes
General-purpose register		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)
Instruction		Variable instruction execution time
cycle	With main system clock	0.5 μ s/1.0 μ s/2.0 μ s/4.0 μ s/8.0 μ s/16.0 μ s (at 6.0 MHz)
	With subsystem clock	122 μ s (at 32.768 kHz)
Instruction set		16-bit operation - Multiplication/division (8 bits $\times$ 8 bits, 16 bits $\div$ 8 bits) - Bit manipulation (set, reset, test, Boolean operation) - BCD adjustment, etc.
I/O port		Total : 69 - CMOS input : 2 - CMOS I/O : 63 - N-ch open-drain I/O : 4
IEBus controller		Effective transmission rate: 3.9 kbps/17 kbps/26 kbps
A/D converter		8-bit resolution $\times$ 8 channels
D/A converter		8-bit resolution $\times$ 2 channels
Serial interface		3-line/SBI/2-line mode selectable : 1 channel 3-line mode (with function to automatically transfer/receive 32 bytes max.) : 1 channel 3-line/UART mode selectable : 1 channel
Timer		16-bit timer/event counter : 1 channel 8-bit timer/event counter : 2 channels - Watch timer : 1 channel - Watchdog timer : 1 channel
Timer output		3 (14-bit PWM output: 1)
Clock output		15.6 kHz, 31.3 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1.0 MHz, 2.0 MHz, 4.0 MHz (with 6.0-MHz main system clock) 32.768 kHz (with 32.768-kHz subsystem clock)
Buzzer output		977 Hz, 1.95 kHz, 3.9 kHz, 7.8 kHz (with 6.0-MHz main system clock)

Notes 1. The internal PROM capacity can be changed by using the memory size select register.

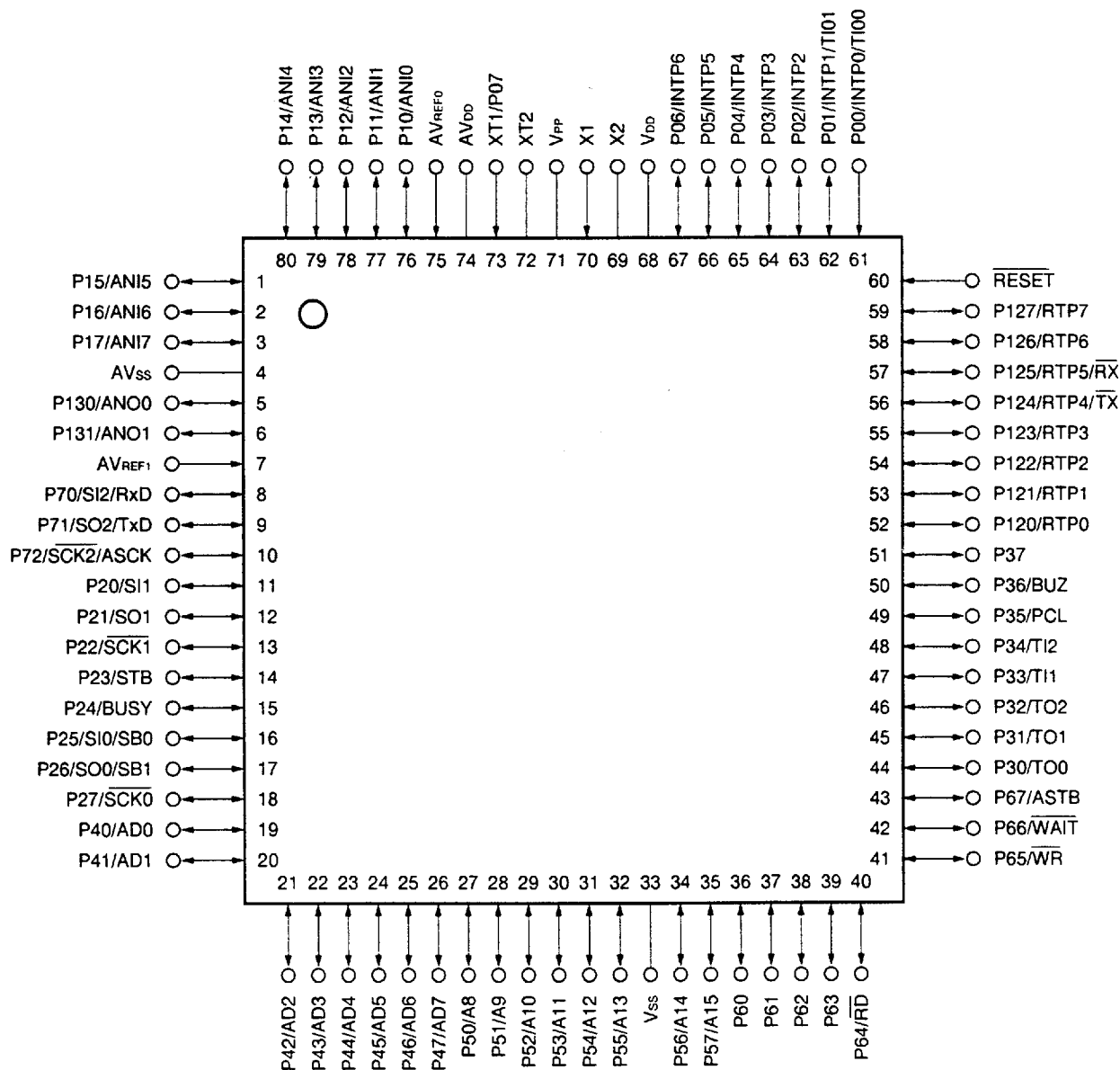
2. 0 or 2048 bytes can be selected by using the internal expansion RAM size select register.

Item		Function
Vector interrupt	Maskable interrupt	Internal: 14, external: 7
	Non-maskable interrupt	Internal: 1
	Software interrupt	Internal: 1
Test input		Internal: 1, external: 1
Operating voltage		V _{DD} = 2.7 to 5.5 V
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin ceramic WQFN (14 × 14 mm)

PIN CONFIGURATION (Top View)

(1) Normal operation mode

- 80-pin plastic QFP (14 × 14 mm)
μPD78P098AGC-3B9
- 80-pin ceramic WQFN (14 × 14 mm)
μPD78P098AKK-T



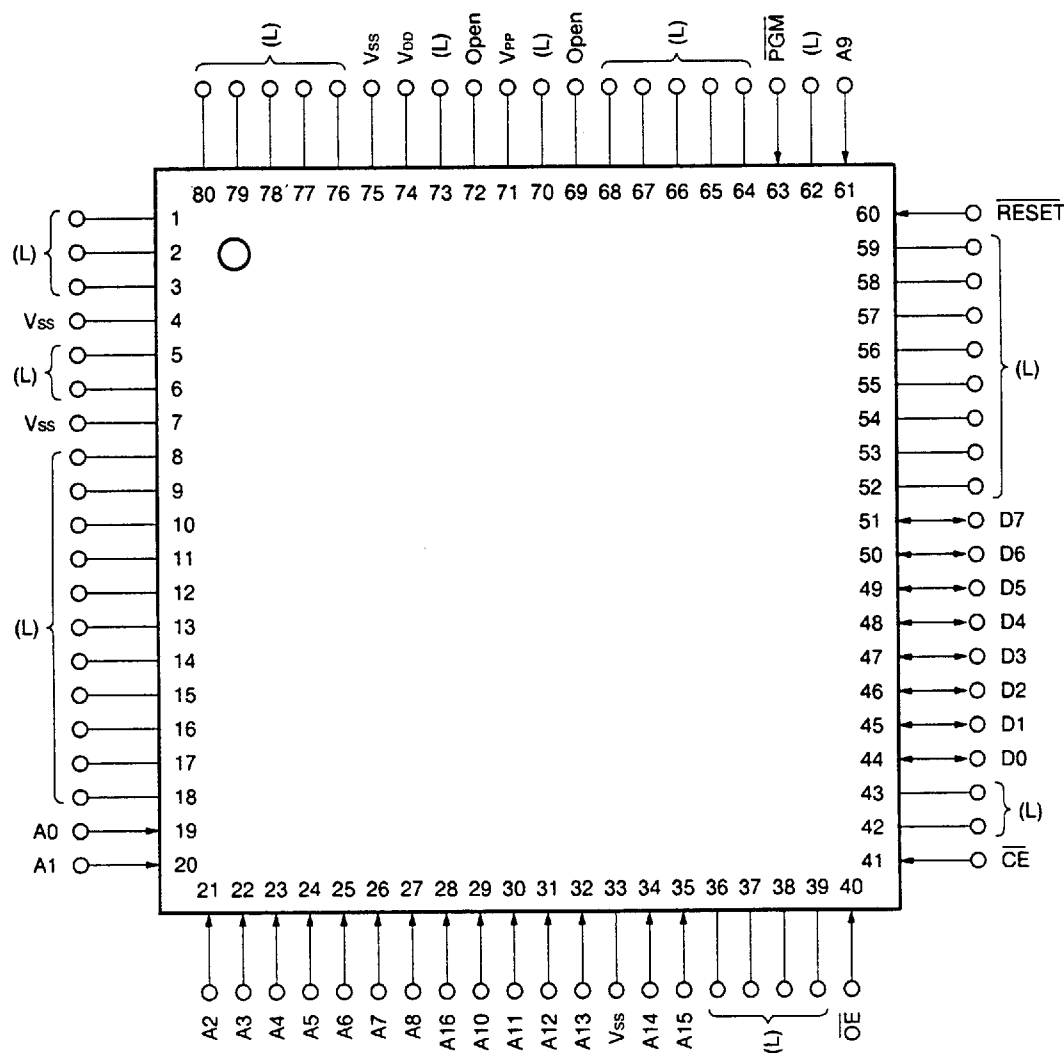
- Cautions**
1. Directly connect the VPP pin to Vss.
 2. Connect the AVDD pin to VDD.
 3. Connect the AVSS pin to Vss.

P00-P07 : Port0
 P10-P17 : Port1
 P20-P27 : Port2
 P30-P37 : Port3
 P40-P47 : Port4
 P50-P57 : Port5
 P60-P67 : Port6
 P70-P72 : Port7
 P120-P127 : Port12
 P130, P131 : Port13
 RTP0-RTP7 : Real-Time Output Port
 INTP0-INTP6 : Interrupt from Peripherals
 TI00, TI01 : Timer Input
 TI1, TI2 : Timer Input
 TO0-TO2 : Timer Output
 SB0, SB1 : Serial Bus
 SI0-SI2 : Serial Input
 SO0-SO2 : Serial Output
 SCK0-SCK2 : Serial Clock
 RxD : Receive Data (UART)
 TxD : Transmit Data (UART)
 ASCK : Asynchronous Serial Clock

$\overline{RX}$: Receive Data (IEBus Controller)
 $\overline{TX}$: Transmit Data (IEBus Controller)
 PCL : Programmable Clock
 BUZ : Buzzer Clock
 STB : Strobe
 BUSY : Busy
 AD0-AD7 : Address/Data Bus
 A8-A15 : Address Bus
 $\overline{RD}$: Read Strobe
 $\overline{WR}$: Write Strobe
 $\overline{WAIT}$: Wait
 ASTB : Address Strobe
 X1, X2 : Crystal (Main System Clock)
 XT1, XT2 : Crystal (Subsystem Clock)
 $\overline{RESET}$: Reset
 ANI0-ANI7 : Analog Input
 ANO0, ANO1 : Analog Output
 AV_{DD} : Analog Power Supply
 AV_{SS} : Analog Ground
 AV_{REF0, 1} : Analog Reference Voltage
 V_{DD} : Power Supply
 V_{PP} : Programming Power Supply
 V_{SS} : Ground

(2) PROM programming mode

- 80-pin plastic QFP (14 × 14 mm)
μPD78P098AGC-3B9
- 80-pin ceramic WQFN (14 × 14 mm)
μPD78P098AKK-T



- Cautions**
1. (L) : Individually connect these pins to Vss via a pull-down resistor.
 2. Vss : Connect this pin to ground.
 3. RESET : Keep this pin to the low level.
 4. Open : Connect nothing to these pins.

A0-A16 : Address Bus
D0-D7 : Data Bus
CE : Chip Enable
OE : Output Enable
PGM : program

RESET : Reset
VDD : Power Supply
VPP : Programming Power Supply
VSS : Ground

BLOCK DIAGRAM

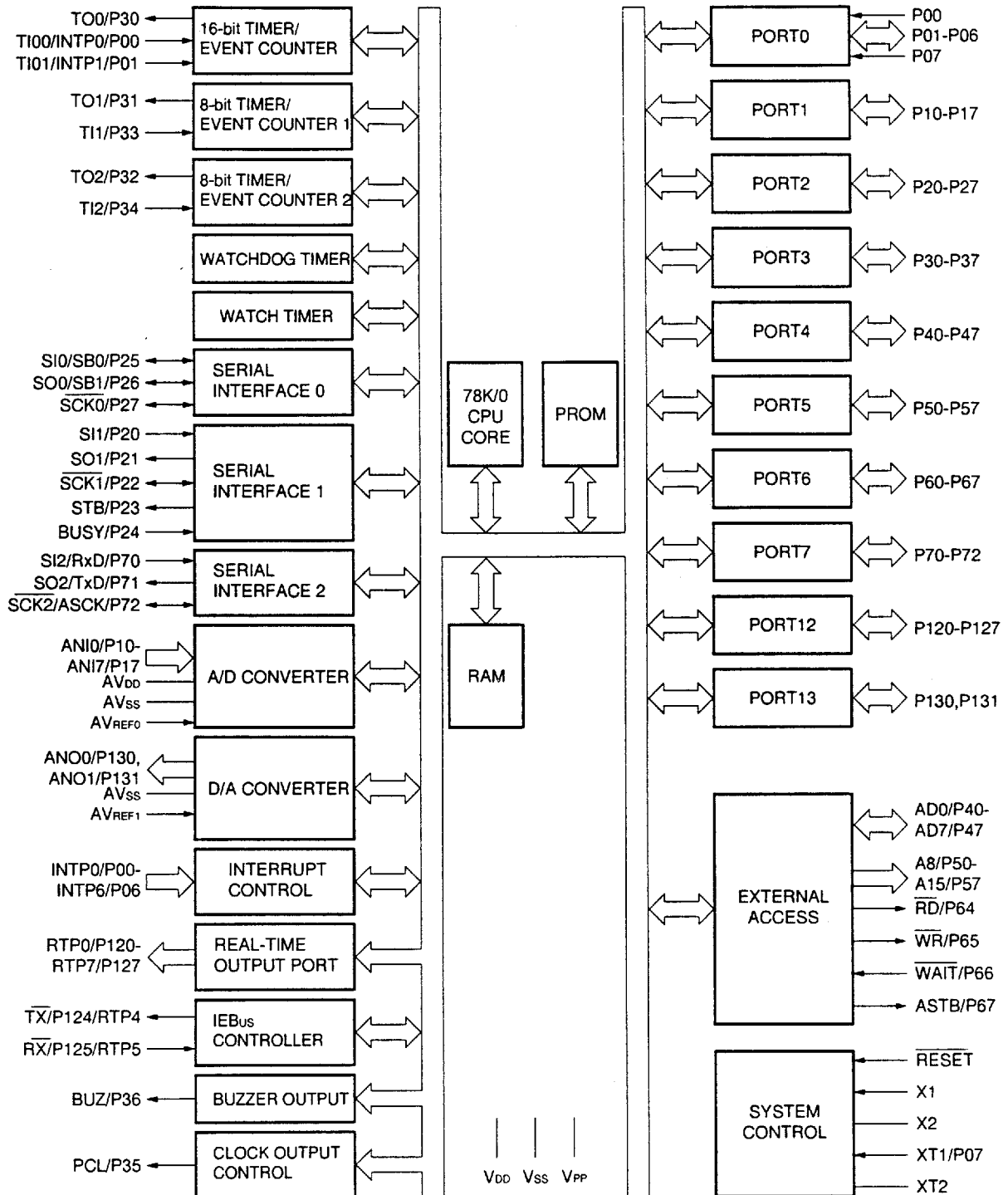


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1. DIFFERENCES BETWEEN μ PD78P098A AND MASK ROM MODEL

The μ PD78P098A is provided with a one-time PROM to which a program can be written only once, or an EPROM to which a program can be written, erased, and rewritten.

The functions of the μ PD78P098A, except the PROM specification and the mask option of P60 through P63 pins, can be set to be the same as those of the mask ROM model by using the memory size select register and internal expansion RAM size select register.

Table 1-1 shows the differences between the μ PD78P098A and mask ROM model.

Table 1-1. Differences between μ PD78P098A and Mask ROM Model

Item	μ PD78P098A	Mask ROM Model
IC pin	Not provided	Provided
V _{PP} pin	Provided	Not provided
Mask option of P60-P63 pins	Pull-up resistor not provided	Pull-up resistor can be provided by mask option

- Cautions**
1. The internal ROM capacity of the μ PD78P098A can be changed by using the memory size select register. The internal PROM capacity is set to 60K bytes at RESET.
 2. The internal expansion RAM capacity of the μ PD78P098A can be changed by using the internal expansion RAM size select register.
The internal expansion RAM capacity is set to 2K bytes at RESET.

2. PIN FUNCTIONS

2.1 Pins in Normal Operation Mode

(1) Port pins (1/2)

Pin Name	I/O	Function		At Reset	Shared with:
P00	Input	Port 0.	Input only	Input	INTP0/TI00
P01	I/O	8-bit I/O port	Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 ^{Note 1}	Input		Input only	Input	XT1
P10-P17	I/O	Port 1. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software. ^{Note 2}		Input	ANI0-ANI7
P20	I/O	Port 2. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.		Input	SI1
P21					SO1
P22					SCK1
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					SCK0
P30	I/O	Port 3. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					-

- Notes**
1. When using the P07/XT1 pin as an input port pin, set bit 6 (FRC) of the processor clock control register to 1 and do not use the feedback resistor of the subsystem clock oscillation circuit.
 2. When using the P10/ANI0 through P17/ANI7 pins as analog input pins of the A/D converter, the pull-up resistors are automatically disconnected.

(1) Port pins (2/2)

Pin Name	I/O	Function		At Reset	Shared with:
P40-P47	I/O	Port 4. 8-bit I/O port. Can be set in input or output mode in 8-bit units. When used as an input port, a pull-up resistor can be connected via software. Test input flag (KRIF) is set to 1 at falling edge of this port.		Input	AD0-AD7
P50-P57	I/O	Port 5. 8-bit I/O port. Can directly drive LED. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.		Input	A8-A15
P60	I/O	Port 6.	N-ch open-drain I/O port.	Input	-
P61		8-bit I/O port.	Can directly drive LED.		
P62		Can be set in input or output mode in 1-bit units.	When used as an input port, a pull-up Input resistor can be connected via software.	Input	$\overline{RD}$
P63					$\overline{WR}$
P64					$\overline{WAIT}$
P65					ASTB
P66					
P67					
P70	I/O	Port 7.		Input	SI2/RxD
P71		3-bit I/O port.			SO2/TxD
P72		Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.			$\overline{SCK2/ASCK}$
P120-P123	I/O	Port 12.		Input	RTP0-RTP3
P124		8-bit I/O port.			RTP4/ $\overline{TX}$
P125		Can be set in input or output mode in 1-bit units.			RTP5/ $\overline{RX}$
P126, P127		When used as an input port, a pull-up resistor can be connected via software.			RTP6, RTP7
P130, P131	I/O	Port 13. 2-bit I/O port. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.		Input	ANO0, ANO1

(2) Pins other than port pins (1/2)

Pin Name	I/O	Function	At Reset	Shared with:
INTP0	Input	External interrupt input whose valid edge can be specified (rising edge, falling edge, and both rising and falling edges).	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial data input to serial interface.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial data output from serial interface.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial data input/output of serial interface.	Input	P25/SI0
SB1				P26/SO0
SCK0	I/O	Serial clock input/output of serial interface.	Input	P27
SCK1				P22
SCK2				P72/ASCK
STB	Output	Strobe signal output for serial interface automatic transmission/reception.	Input	P23
BUSY	Input	Busy input for serial interface automatic transmission/reception.	Input	P24
RxD	Input	Serial data input to asynchronous serial interface.	Input	P70/SI2
TxD	Output	Serial data output from asynchronous serial interface.	Input	P71/SO2
ASCK	Input	Serial clock input to asynchronous serial interface.	Input	P72/SCK2
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer output (shared with 14-bit PWM output).	Input	P30
TO1		8-bit timer output (TM1).		P31
TO2		8-bit timer output (TM2)		P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0-RTP3	Output	Real-time output port outputting data in synchronization with trigger.	Input	P120-P123
RTP4				P124/TX
RTP5				P125/RX
RTP6, RTP7				P126, P127
T $\bar{X}$	Output	Data output for IEBus controller.	Input	P124/RTP4
R $\bar{X}$	Input	Data input for IEBus controller.	Input	P125/RTP5

(2) Pins other than port pins (2/2)

Pin Name	I/O	Function	At Reset	Shared with:
AD0-AD7	I/O	Low-order address/data bus when external memory is connected.	Input	P40-P47
A8-A15	Output	High-order address bus when external memory is connected.	Input	P50-P57
$\overline{RD}$	Output	Strobe signal output for read operation on external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation on external memory.	Input	P65
$\overline{WAIT}$	Input	Wait state insertion for external memory access.	Input	P66
ASTB	Output	Strobe output to externally latch address information output to ports 4 and 5 to access external memory.	Input	P67
ANI0-ANI7	Input	Analog input of A/D converter.	Input	P10-P17
ANO0, ANO1	Output	Analog output of D/A converter.	Input	P130, P131
AVREF0	Input	Reference voltage input of A/D converter.	—	—
AVREF1	Input	Reference voltage input of D/A converter.	—	—
AVDD	—	Analog power supply of A/D converter. Connected to VDD.	—	—
AVSS	—	Ground of A/D converter. Connected to Vss.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Crystal connection for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Crystal connection for subsystem clock oscillation.	Input	P07
XT2	—		—	—
VDD	—	Positive power supply.	—	—
VPP	—	High-voltage application for program write/verify. Directly connected to Vss in normal operation mode.	—	—
Vss	—	Ground.	—	—

2.2 Pins in PROM Programming Mode

Pin Name	I/O	Function
$\overline{RESET}$	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the VPP pin, and low level is applied to the $\overline{RESET}$ pin, PROM programming mode is set.
VPP	Input	PROM programming mode setting and high voltage application for program write/verify.
A0-A16	Input	Address bus.
D0-D7	I/O	Data bus.
$\overline{CE}$	Input	PROM enable input/program pulse input.
$\overline{OE}$	Input	Read strobe input to PROM.
$\overline{PGM}$	Input	Program/program inhibit input in PROM programming mode.
VDD	—	Positive power supply.
Vss	—	Ground.

2.3 Pin I/O Circuits and Handling of Unused Pins

Table 2-1 shows the types of the I/O circuits for the various pins and handling of unused pins.

For the configuration of the various I/O circuits, refer to Figure 2-1.

Table 2-1. I/O Circuit Type of Each Pin (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection When Not Used
P00/INTP0/TI00	2	Input	Connect to V _{ss} .
P01/INTP1/TI01	8-A	I/O	Individually connect to V _{ss} via resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V _{DD} or V _{ss} .
P10/ANI0-P17/ANI7	11	I/O	Individually connect to V _{DD} or V _{ss} via resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/ $\overline{\text{SCK}}1$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/ $\overline{\text{SCK}}0$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0-P47/AD7	5-E		Individually connect to V _{DD} via resistor.
P50/A8-P57/A15	5-A		Individually connect to V _{DD} or V _{ss} via resistor.
P60-P63	13-D		Individually connect to V _{DD} via resistor.
P64/ $\overline{\text{RD}}$	5-A		Individually connect to V _{DD} or V _{ss} via resistor.
P65/ $\overline{\text{WR}}$			
P66/ $\overline{\text{WAIT}}$			
P67/ASTB			

Table 2-1. I/O Circuit Type of Each Pin (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection When Not Used
P70/SI2/RxD	8-A	I/O	Individually connect to V _{DD} or V _{SS} via resistor.
P71/SO2/TxD	5-A		
P72/SCK2/ASCK	8-A		
P120/RTP0-P123/RTP3	5-A		
P124/RTP4/TX			
P125/RTP5/RX			
P126/RTP6, P127/RTP7			
P130/ANO0, P131/ANO1	12-A		
RESET	2	Input	—
XT2	16	—	Open
AV _{REF0}	—		Connect to V _{SS} .
AV _{REF1}			Connect to V _{DD} .
AV _{DD}			
AV _{SS}			Connect to V _{SS} .
V _{PP}			Directly connect to V _{SS} .

Figure 2-1. I/O Circuits of Pins (1/2)

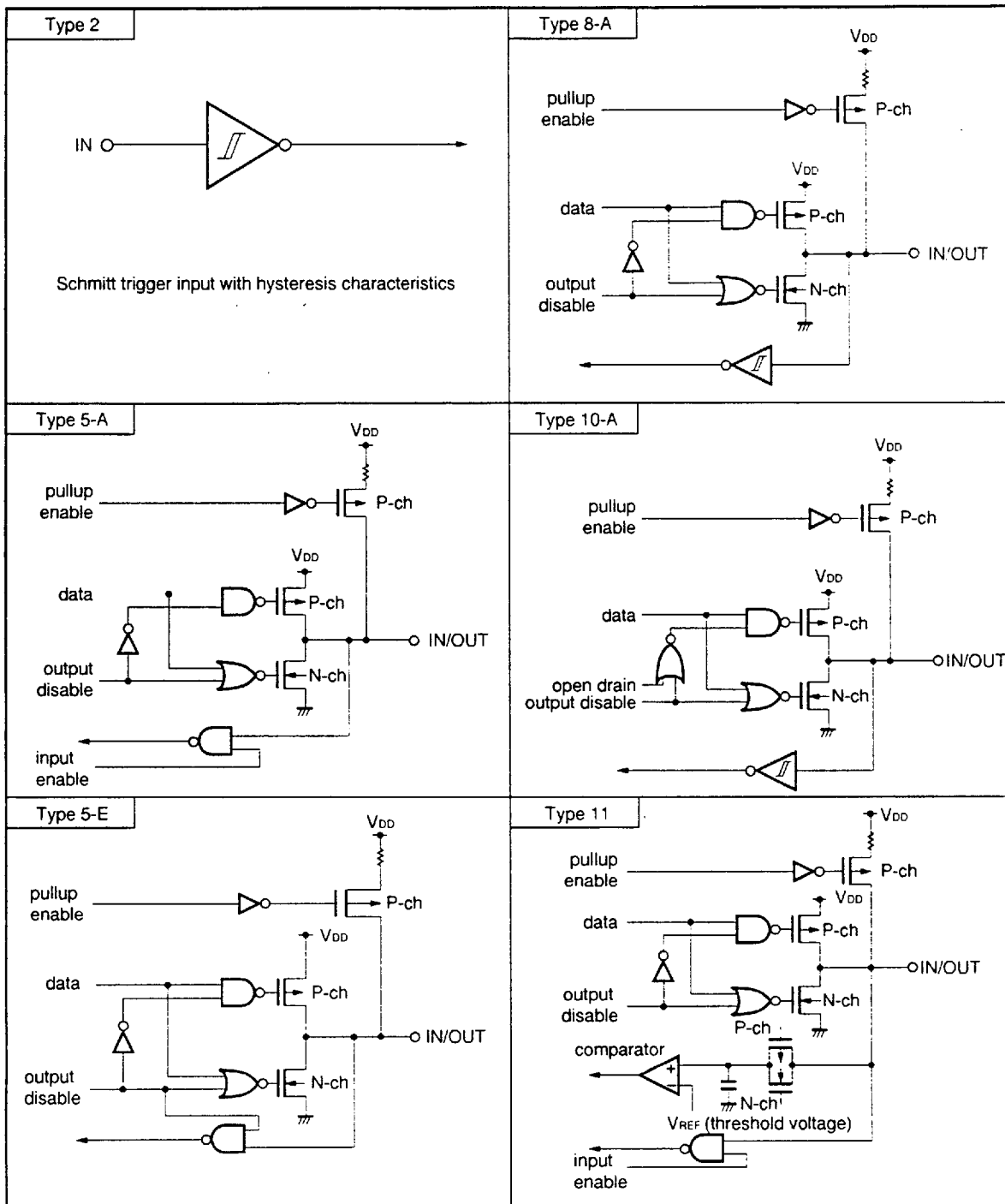
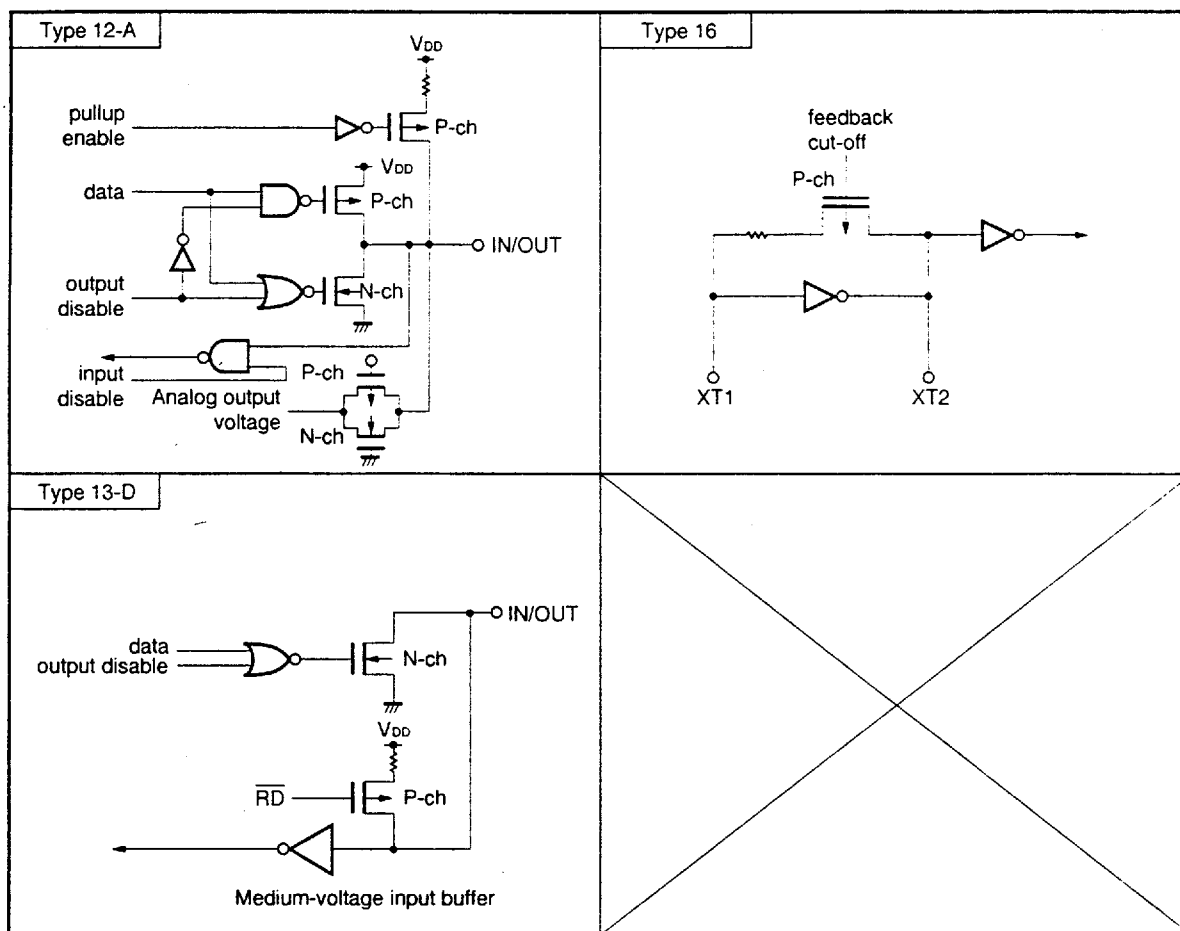


Figure 2-1. I/O Circuits of Pins (2/2)



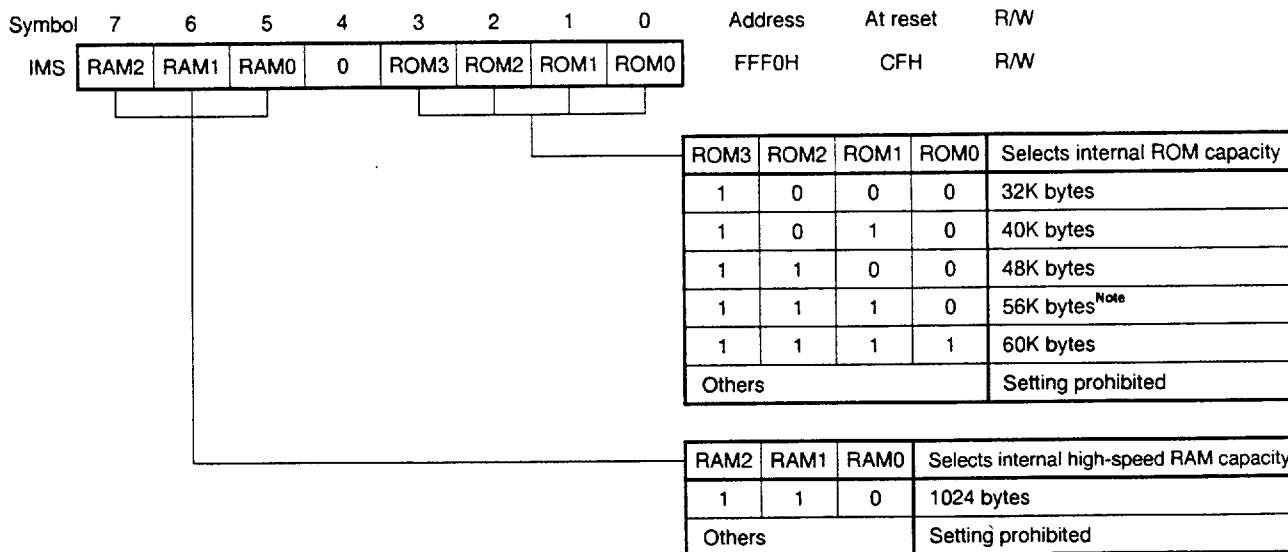
3. MEMORY SIZE SELECT REGISTER (IMS)

This register specifies via software that part of the internal memory is not used. By using this register, the internal memory (ROM) of the μPD78P098A can be mapped in the same manner as a mask ROM model.

IMS is set by an 8-bit memory manipulation instruction.

The contents of this register are set to CFH at RESET.

Figure 3-1. Format of the Memory Size Select Register



Note When using the external device expansion function, set the internal PROM capacity to 56K bytes or less.

Table 3-1 shows the value settings of IMS to map the memory of the μPD78P098A in the same manner as the respective mask ROM models.

Table 3-1. Value Settings of the Memory Size Select Register

Mask ROM Model	IMS Value Setting
μPD78094	C8H
μPD78095	CAH
μPD78096	CCH
μPD78098A	CFH

4. INTERNAL EXPANSION RAM SIZE SELECT REGISTER (IXS)

This register specifies the internal expansion RAM capacity via software. By using this register, the internal expansion RAM of the μPD78P098A can be mapped in the same manner as a mask ROM model.

IXS is set by an 8-bit memory manipulation instruction.

The contents of this register are set to 08H at RESET.

Figure 4-1. Format of Internal Expansion RAM Size Select Register

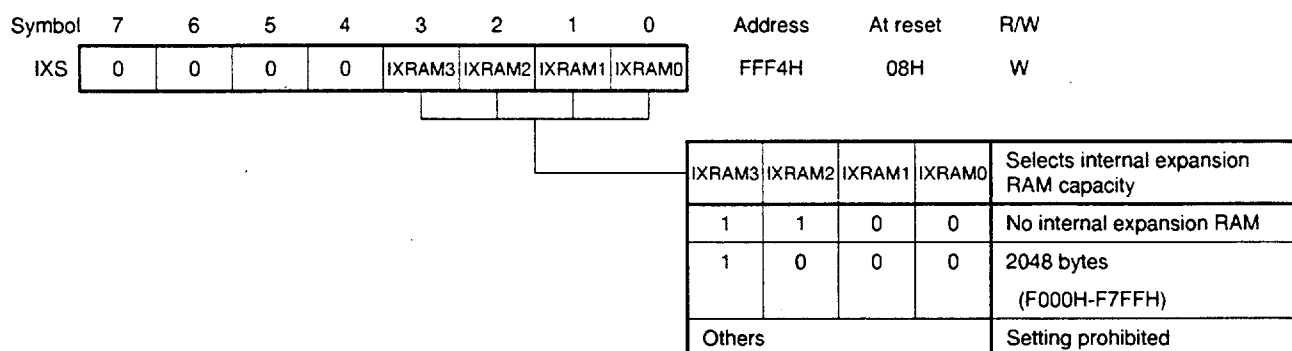


Table 4-1 shows the value settings of IXS to map the internal expansion RAM of the μPD78P098A in the same manner as the respective mask ROM models.

Table 4-1. Value Settings of Internal Expansion RAM Size Select Register

Mask ROM Model	IXS Value Setting
μPD78094	0CH ^{Note}
μPD78095	
μPD78096	
μPD78098A	08H

Note Even when a program for the μPD78P098A in which "MOV IXS, #0CH" is coded is executed on the μPD78094, 78095, or 78096, operation is unaffected.

5. PROM PROGRAMMING

The μ PD78P098A is provided with a 60K-byte PROM as a program memory. When programming this memory, it must be set in the PROM programming mode by using the V_{PP} and $\overline{RESET}$ pins. For the handling of the unused pins, refer to (2) **PROM programming mode** in **PIN CONFIGURATION (Top View)**.

Caution Write the program to addresses in the range 0000H through EFFFH (specify the last address as EFFFH). A program cannot be written with a PROM programmer that cannot specify write addresses.

5.1 Operation Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and low level is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. In this mode, the operation modes shown in Table 5-1 can be selected by using the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins.

The contents of the PROM can be read in the read mode.

Table 5-1. Operation Modes in PROM Programming Mode

Pin Operation Mode	RESET	V _{PP}	V _{DD}	CE	OE	PGM	D0-D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				x	H	H	High impedance
				x	L	L	
Read	+5 V	+5 V	L	L	H	Data output	
Output disable			L	H	x	High impedance	
Standby			H	x	x	High impedance	

Remark x: L or H

(1) Read mode

This mode is set when both the $\overline{CE}$ and $\overline{OE}$ pins are made low.

(2) Output disable mode

When the $\overline{OE}$ pin is made high, data output goes into a high-impedance state, and the output disable mode is set.

If two or more μ PD78P098As are connected to the data bus, therefore, data can be read from any one of the devices by controlling the $\overline{OE}$ pin.

(3) Standby mode

The standby mode is set when the $\overline{CE}$ pin is made high.

In this mode, data output goes into a high-impedance state regardless of the status of the $\overline{OE}$ pin.

(4) Page data latch mode

The page data latch mode is set when the $\overline{CE}$ and $\overline{PGM}$ pins are made high and the $\overline{OE}$ pin is made low at the beginning of the page write mode.

In this mode, data of 1 page and 4 bytes is latched to the internal address/data latch circuit.

(5) Page write mode

Page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with the $\overline{CE}$ and $\overline{OE}$ pins made high after addresses and data of 1 page and 4 bytes have been latched in the page data latch mode. After that, the program can be verified by making both the $\overline{CE}$ and $\overline{OE}$ pins low.

If the program cannot be written by one program pulse, writing and verifying are repeated X times ($X \leq 10$).

(6) Byte write mode

Byte write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with the $\overline{CE}$ pin made low and $\overline{OE}$ pin high. The program is verified by later making the $\overline{OE}$ pin low.

If the program cannot be written by one program pulse, writing and verifying are repeated X times ($X \leq 10$).

(7) Program verify mode

Program verify mode is set when the $\overline{CE}$ and $\overline{OE}$ pins are made low and the $\overline{PGM}$ pin is made high.

After writing the program, check in this mode whether the program has been correctly written.

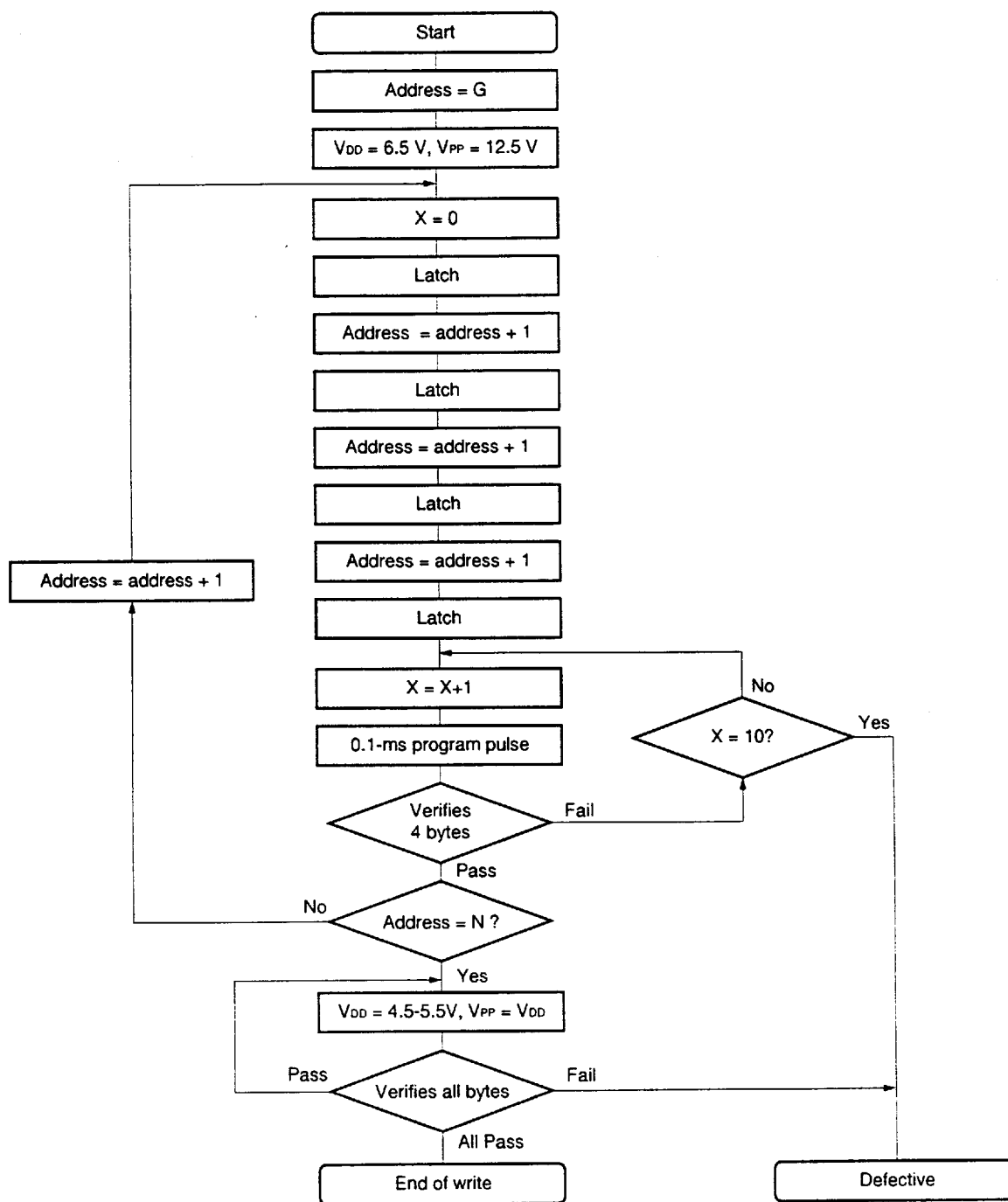
(8) Program inhibit mode

This mode is used to write a program to one of two or more μ PD78P098As with the $\overline{OE}$, V_{PP} , and D0 through D7 pins connected in parallel.

To write a program, the page write or byte write mode described above is used. At this time, the program is not written to those devices whose $\overline{PGM}$ pin is made high.

5.2 PROM Writing Procedure

Figure 5-1. Page Program Mode Flowchart



G = start address

N = end address of program

Figure 5-2. Page Program Mode Timing

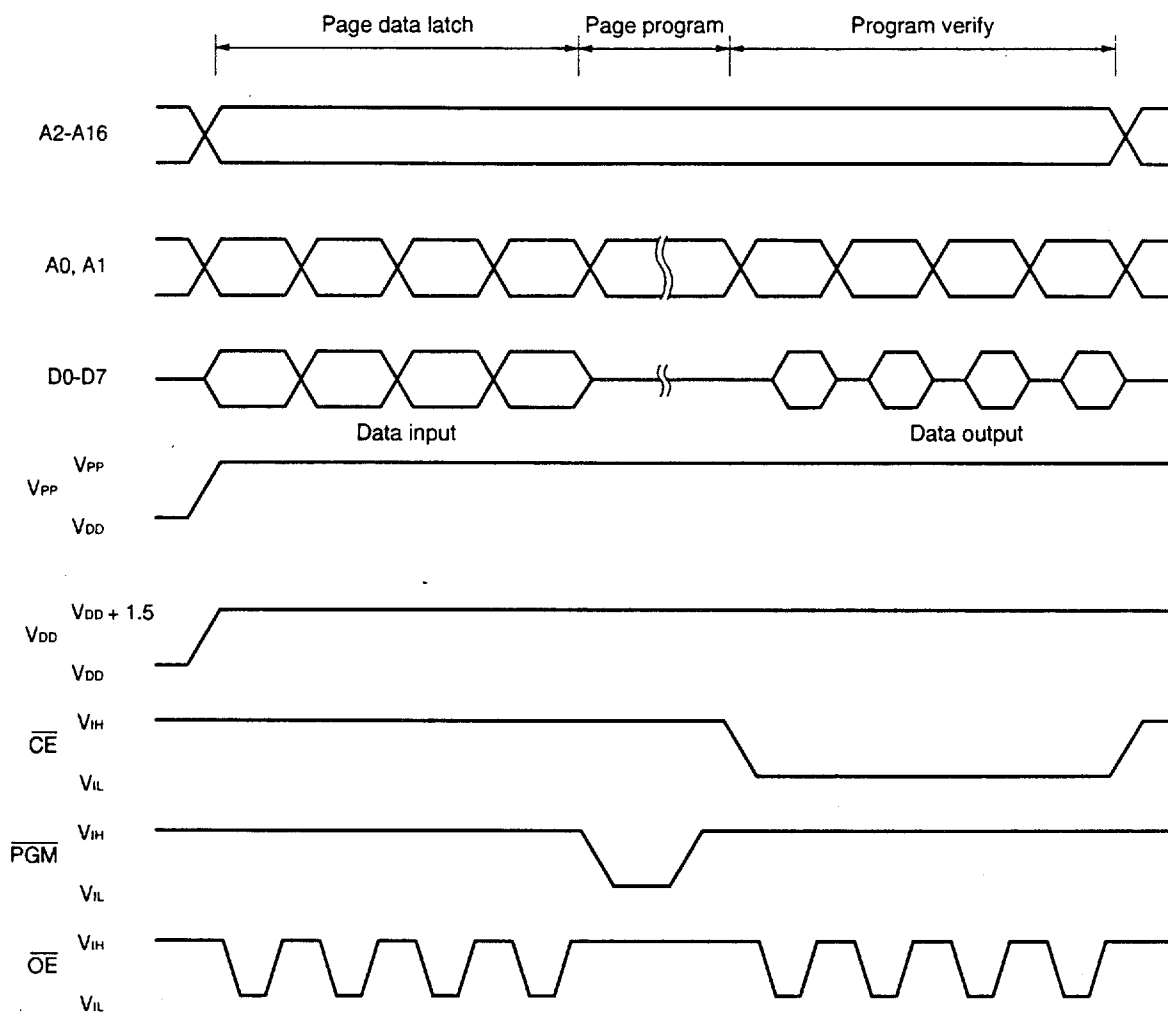
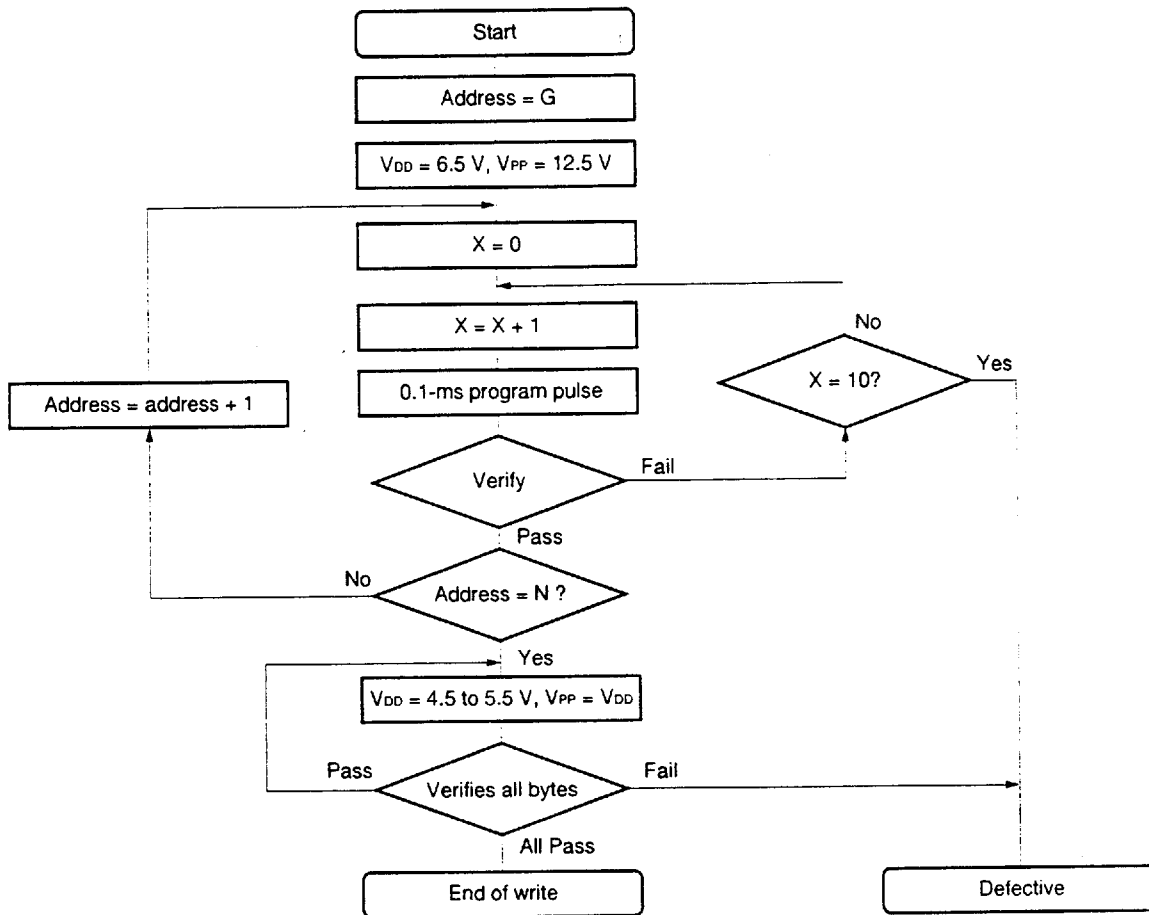


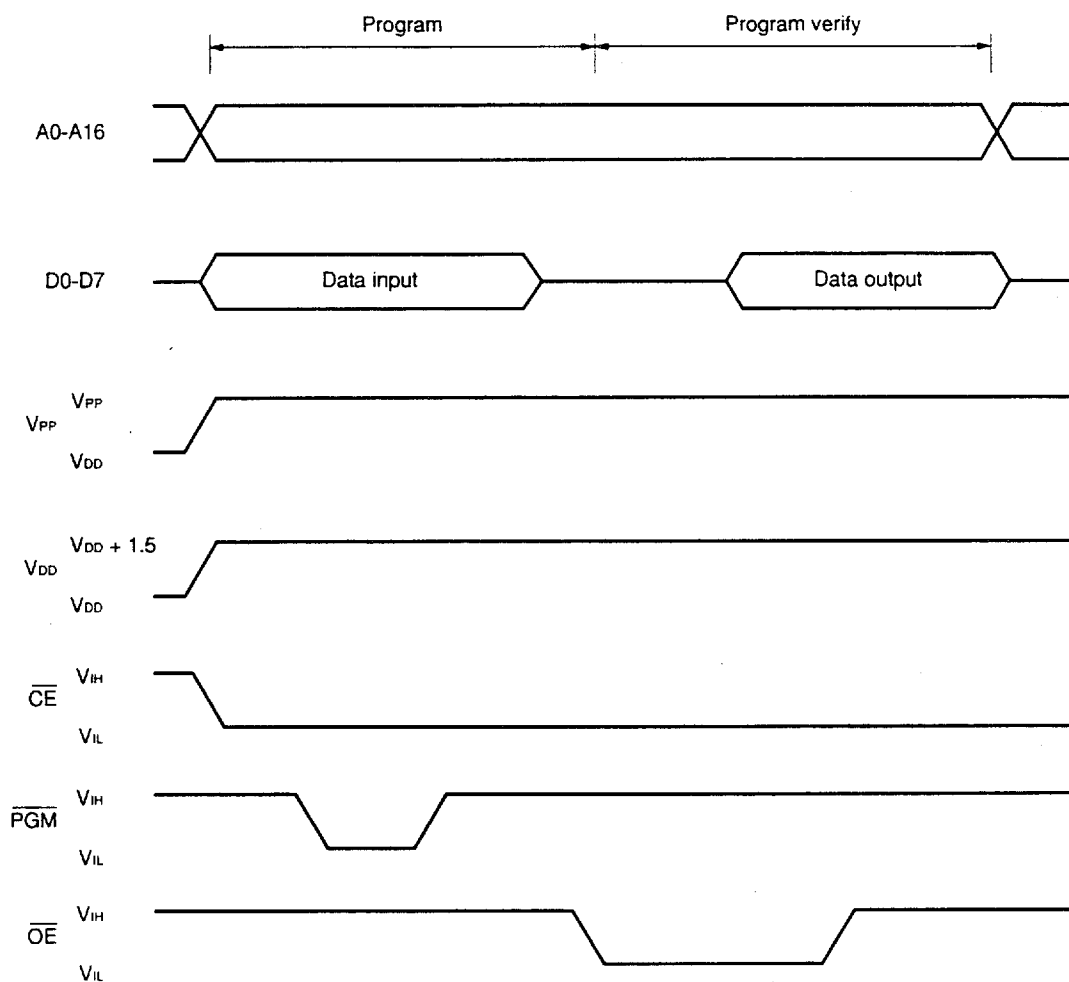
Figure 5-3. Byte Program Mode Flowchart



G = start address

N = end address of program

Figure 5-4. Byte Program Mode Timing



- Cautions**
1. Apply V_{DD} before V_{PP} and turn off V_{DD} after V_{PP}.
 2. Keep V_{PP} from going above +13.5 V, including overshoot.
 3. If the device is inserted into or pulled out of the socket while +12.5 V is applied to V_{PP}, the reliability may be adversely affected.

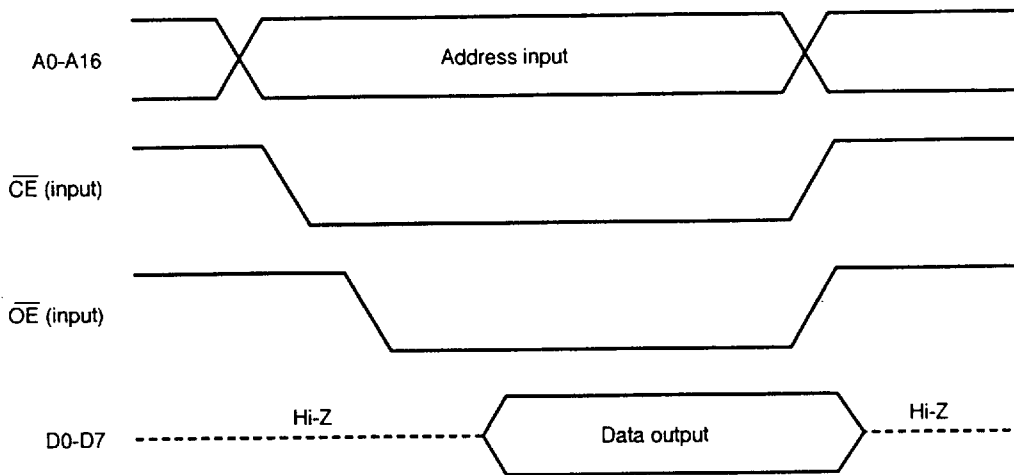
5.3 PROM Read Procedure

The contents of the PROM can be read out to the external data bus (D0 through D7) in the following procedure:

- (1) Fix the $\overline{\text{RESET}}$ pin to the low level. Supply +5 V to the V_{PP} pin. Process the unused pins as described in **(2) PROM programming mode in PIN CONFIGURATION (Top View)**.
- (2) Supply +5 V to the V_{DD} and V_{PP} pins.
- (3) Input the address of the data to be read to the A0 through A16 pins.
- (4) The read mode is set.
- (5) Data is output to the D0 through D7 pins.

Figure 5-5 shows the timing of steps (2) through (5) above.

Figure 5-5. PROM Read Timing



6. ERASURE (μ PD78P098AKK-T only)

Data written to the program memory of the μ PD78P098AKK-T can be erased (to FFH) and then new data can be written.

To erase the data, shine light with a wavelength of 400 nm or shorter in the window of the μ PD78P098AKK-T. Usually, this light is ultraviolet at 254 nm. The amount of light required to completely erase the data is as follows:

- Ultraviolet intensity x erasure time: 15 W·s/cm² min.
- Erasure time: 15 to 20 minutes (when an ultraviolet lamp of 12,000 μ W/cm² is used. However, a longer time may be required depending on degradation of the ultraviolet lamp or dirt on the window.)

Install the ultraviolet lamp at a position 2.5 cm or less from the erasure window. If a filter is attached to the lamp, remove the filter before shining the lamp.

7. STICKER ON ERASURE WINDOW (μ PD78P098AKK-T only)

Attach a protective sticker to the erasure window to protect the contents of the EPROM from being erased with light of other than erasure lamp by mistake and to prevent the internal circuits of the μ PD78P098A other than the EPROM from malfunctioning due to external disturbances caused by light.

8. SCREENING OF ONE-TIME PROM MODEL

The one-time PROM model (μ PD78P098AGC-3B9) cannot be completely tested by NEC before shipment. It is recommended that screening be implemented to verify the PROM after data has been written to the PROM and the device has been stored under the following conditions:

Storage Temperature	Storage Time
125 °C	24 hours

NEC provides a writing, marking, screening, and verifying service for one-time PROMs, called QTOP microcontroller. This service for the μ PD78P098A is in preparation. For details, consult NEC.

9. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

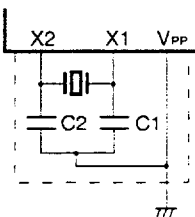
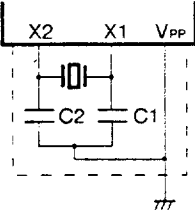
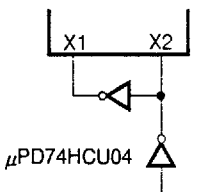
Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V _{DD}			-0.3 to +7.0	V
	V _{PP}			-0.3 to +13.5	V
	AV _{DD}			-0.3 to V _{DD} +0.3	V
	AV _{REF0}			-0.3 to V _{DD} +0.3	V
	AV _{REF1}			-0.3 to V _{DD} +0.3	V
	AV _{SS}			-0.3 to +0.3	V
Input voltage	V _{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, RESET		-0.3 to V _{DD} +0.3	V
	V _{I2}	P60 to P63	N-ch open drain	-0.3 to +16	V
	V _{I3}	A9	PROM programming mode	-0.3 to +13.5	V
Output voltage	V _O			-0.3 to V _{DD} +0.3	V
Analog input voltage	V _{AN}	P10 to P17	Analog input pins	AV _{SS} -0.3 to AV _{REF0} +0.3	V
Output current high	I _{OH}	1 pin		-10	mA
		Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P127		-15	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131		-15	mA
Output current low	I _{OL} Note	1 pin	Peak value	30	mA
			R.m.s. value	15	mA
		Total for P50 to P55	Peak value	100	mA
			R.m.s. value	70	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			R.m.s. value	70	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131	Peak value	50	mA
			R.m.s. value	20	mA
		Total for P01 to P06, P30 to P37, P64 to P67, P120 to P127	Peak value	50	mA
			R.m.s.	20	mA
Operating ambient temperature	T _A			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C
Total power dissipation	P _d			650	mW

Note The r.m.s. value should be calculated as follows: [R.m.s. value] = [Peak value] × √Duty

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (fx) ^{Note1}	VDD = Oscillation voltage range	1.0	6.0	6.29	MHz
		Oscillation stabilization time ^{Note2}	After VDD has reached MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (fx) ^{Note1}		1.0	6.0	6.29	MHz
		Oscillation stabilization time ^{Note2}	VDD = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx) ^{Note1}		1.0	6.0	6.29	MHz
		X1 input high-/low-level width (txH/txL)	When fxx = fx	85		500	ns
			Other than above	72		500	ns

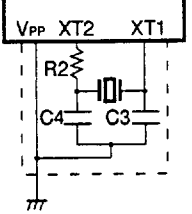
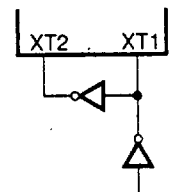
- Notes**
- Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.
 - This is the time required for oscillation to stabilize after a reset or STOP mode release.

Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- The wiring should be kept as short as possible.
- No other signal lines should be crossed.
- Keep away from lines carrying a high fluctuating current.
- The oscillator capacitor grounding point should always be at the same potential as V_{SS} .
- Do not connect to a ground pattern carrying a high current.
- A signal should not be taken from the oscillator.

- When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

SUBSYSTEM CLOCK OSILLATOR CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) ^{Note1}		32	32.768	35	MHz
		Oscillation stabilization time ^{Note2}	$V_{DD} = 4.5$ to 5.5 V		1.2	2	s
External clock		X1 input frequency (f_{XT}) ^{Note1}		32		100	kHz
		X1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

- Notes**
- Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.
 - This is the time required for oscillation to stabilize after power (V_{DD}) is turned on.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- The wiring should be kept as short as possible.
- No other signal lines should be crossed.
- Keep away from lines carrying a high fluctuating current.
- The oscillator capacitor grounding point should always be at the same potential as V_{SS} .
- Do not connect to a ground pattern carrying a high current.
- A signal should not be taken from the oscillator.

- The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

CAPACITANCE ($T_A = 25$ °C, $V_{DD} = V_{SS} = 0$ V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$f = 1$ MHz Unmeasured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	$f = 1$ MHz Unmeasured pins returned to 0	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V _{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131		0.7 V _{DD}		V _{DD}	V
	V _{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, <u>RESET</u>		0.8 V _{DD}		V _{DD}	V
	V _{IH3}	P60 to P63, N-ch open drain		0.7 V _{DD}		15	V
	V _{IH4}	X1, X2		V _{DD} −0.5		V _{DD}	V
	V _{IH5}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 5.5 V	0.8 V _{DD}		V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0.9 V _{DD}		V _{DD}	V
Input voltage low	V _{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131		0		0.3 V _{DD}	V
	V _{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, <u>RESET</u>		0		0.2 V _{DD}	V
	V _{IL3}	P60 to P63, N-ch open drain	4.5 V ≤ V _{DD} ≤ 5.5 V	0		0.3 V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.2 V _{DD}	V
	V _{IL4}	X1, X2		0		0.4	V
	V _{IL5}	XT1/P07, XT2	V _{DD} = 4.5 to 5.5 V	0		0.2 V _{DD}	V
				0		0.1 V _{DD}	V
Output voltage high	V _{OH1}	V _{DD} = 4.5 to 5.5 V, I _{OH} = −1 mA		V _{DD} −1.0			V
		I _{OH} = −100 μA		V _{DD} −0.5			V
Output voltage low	V _{OL1}	P50 to P57, P60 to P63	V _{DD} = 4.5 to 5.5 V, I _{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V _{DD} = 4.5 to 5.5 V, I _{OL} = 1.6 mA			0.4	V
	V _{OL2}	SB0, SB1, <u>SCK0</u>	V _{DD} = 4.5 to 5.5 V, Open drain, at pulled up (R = 1 kΩ)			0.2 V _{DD}	V
	V _{OL3}	I _{OL} = 400 μA				0.5	V

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, $\overline{RESET}$ P120 to P127, P130, P131, $\overline{RESET}$			3	μA
	I_{LH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LH3}	$V_{IN} = 15V$	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	$V_{IN} = 0 V$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, $\overline{RESET}$ P120 to P127, P130, P131, $\overline{RESET}$			-3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			-20	μA
	I_{LIL3}		P60 to P63			-3 ^{Note}	μA
Output leakage current high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	$V_{OUT} = 0 V$				-3	μA
Software pull-up resistor	R	$V_{IN} = 0 V$, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	$4.5 \leq V_{DD} \leq 5.5 V$	15	40	90	k Ω
			$2.7 \leq V_{DD} \leq 4.5 V$	20		500	k Ω

Note For P60-P63, a low-level input leak current of $-200 \mu A$ (MAX.) flows only during the 1.5 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 1.5 clocks following execution a read-out instruction, the current is $-3 \mu A$ (MAX.).

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I _{DD1}	5.0 MHz crystal oscillation operating mode (f _{xx} = 2.5 MHz) ^{Note2}	V _{DD} = 5.0V ± 10% ^{Note6}	5	15	mA
			V _{DD} = 3.0V ± 10% ^{Note7}	0.7	2.7	mA
		5.0 MHz crystal oscillation operating mode (f _{xx} = 5.0 MHz) ^{Note3}	V _{DD} = 5.0V ± 10% ^{Note6}	9	30	mA
			V _{DD} = 3.0V ± 10% ^{Note7}	1	3.7	mA
		6.29 MHz crystal oscillation operating mode (f _{xx} = 2.1 MHz) ^{Note4}	V _{DD} = 5.0V ± 10% ^{Note6}	4.8	17.4	mA
		6.29 MHz crystal oscillation operating mode (f _{xx} = 4.19 MHz) ^{Note5}	V _{DD} = 5.0V ± 10% ^{Note6}	8.5	28.5	mA

- Notes**
1. Currents AV_{REF0}, AV_{REF1}, AV_{DD}, and the port current (including the current flowing in the internal pull-up resistor) are not included.
 2. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.
 3. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.
 4. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.
 5. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.
 6. When in high-speed mode (when the processor clock control register has been set to 00H).
 7. When in low-speed mode (when the processor clock control register has been set to 04H).

Remark f_{xx}: Main system clock frequency

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I _{DD2}	5.0 MHz crystal oscillation HALT mode (f _{xx} = 2.5 MHz) ^{Note 2}	V _{DD} = 5.0V±10% ^{Note 7}	1.5	4.5	mA
			V _{DD} = 3.0V±10% ^{Note 8}	0.5	1.5	mA
		5.0 MHz crystal oscillation HALT mode (f _{xx} = 5.0 MHz) ^{Note 3}	V _{DD} = 5.0V±10% ^{Note 7}	1.8	5.4	mA
			V _{DD} = 3.0V±10% ^{Note 8}	0.7	2.1	mA
		6.29 MHz crystal oscillation HALT mode (f _{xx} = 2.1 MHz) ^{Note 4}	V _{DD} = 5.0V±10% ^{Note 7}	1.5	4.5	mA
		6.29 MHz crystal oscillation HALT mode (f _{xx} = 4.19 MHz) ^{Note 5}	V _{DD} = 5.0V±10% ^{Note 7}	1.8	5.4	mA
	I _{DD3}	32.768 kHz crystal oscillation operating mode ^{Note 6}	V _{DD} = 5.0V±10%	135	270	μA
			V _{DD} = 3.0V±10%	95	190	μA
	I _{DD4}	32.768 kHz crystal oscillation HALT mode ^{Note 6}	V _{DD} = 5.0V±10%	25	55	μA
			V _{DD} = 3.0V±10%	5	15	μA
	I _{DD5}	XT1 = 0 V STOP mode Feedback resistor used	V _{DD} = 5.0V±10%	1	30	μA
			V _{DD} = 3.0V±10%	0.5	10	μA
	I _{DD6}	XT1 = 0 V STOP mode Feedback resistor not used	V _{DD} = 5.0V±10%	0.1	30	μA
			V _{DD} = 3.0V±10%	0.05	10	μA

- Notes**
1. Currents AV_{REF0}, AV_{REF1}, AV_{DD}, and the port current (including the current flowing in the internal pull-up resistor) are not included.
 2. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.
 3. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.
 4. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.
 5. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.
 6. When the main system clock is stopped.
 7. When in high-speed mode (when the processor clock control register has been set to 00H).
 8. When in low-speed mode (when the processor clock control register has been set to 04H).

Remark f_{xx} : Main system clock frequency

AC CHARACTERISTICS

(1) Basic Operation ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

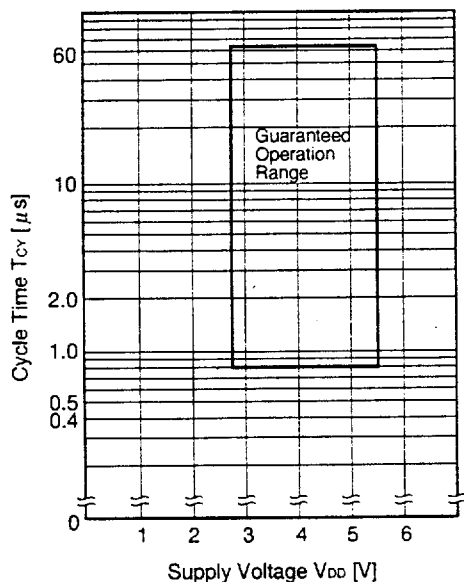
Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution timke)	T _{CY}	Operating on main system clock (MCS = 0 ^{Note 1})	f _{xx} = f _x /3	4.0 V ≤ V _{DD} ≤ 5.5 V	0.95		64	μs
			f _{xx} = f _x /6	2.7 V ≤ V _{DD} ≤ 5.5 V	1.91		64	μs
			f _{xx} = f _x /9	4.0 V ≤ V _{DD} ≤ 5.5 V	2.86		64	μs
			f _{xx} = f _x /2	2.7 V ≤ V _{DD} ≤ 5.5 V	0.8		64	μs
		Operating on main system clock (MCS = 1 ^{Note 2})	f _{xx} = 2f _x /3	4.5 V ≤ V _{DD} ≤ 5.5 V	0.48		32	μs
				4.0 V ≤ V _{DD} < 4.5 V	0.95		32	μs
			f _{xx} = f _x /3	2.7 V ≤ V _{DD} ≤ 5.5 V	0.95		32	μs
			f _{xx} = 2f _x /9	4.0 V ≤ V _{DD} ≤ 5.5 V	1.43		32	μs
			f _{xx} = f _x	4.5 V ≤ V _{DD} ≤ 5.5 V	0.4		32	μs
				2.7 V ≤ V _{DD} < 4.5 V	0.8		32	μs
Operating on subsystem clock				114	122	125	μs	
TI00 input high-/low-level width	t _{TIH00} , t _{TIL00}	3.5 V ≤ V _{DD} ≤ 5.5 V			^{Note3} 2/f _{sam} +0.1			μs
		2.7 V ≤ V _{DD} < 3.5 V			^{Note3} 2/f _{sam} +0.2			μs
TI01 input high-/low-level width	t _{TIH01} , t _{TIL01}				10			μs
TI1, TI2 input frequency	f _{TI1}	4.5 V ≤ V _{DD} ≤ 5.5 V			0		4	MHz
					0		275	kHz
TI1, TI2 input high-/low-level width	t _{TIH1} , t _{TIL1}	4.5 V ≤ V _{DD} ≤ 5.5 V			100			ns
					1.8			μs
Interrupt input high-/low-level width	t _{INTH} , t _{INTL}	INTP0	3.5 V ≤ V _{DD} ≤ 5.5 V		^{Note3} 2/f _{sam} +0.1			μs
			2.7 V ≤ V _{DD} < 3.5 V		^{Note3} 2/f _{sam} +0.2			μs
		INTP1 to INTP6			10			μs
		KR0 to KR7			10			μs
RESET low-level width	t _{RST}				10			μs

Notes 1. When oscillation mode selection register is set to 00H.

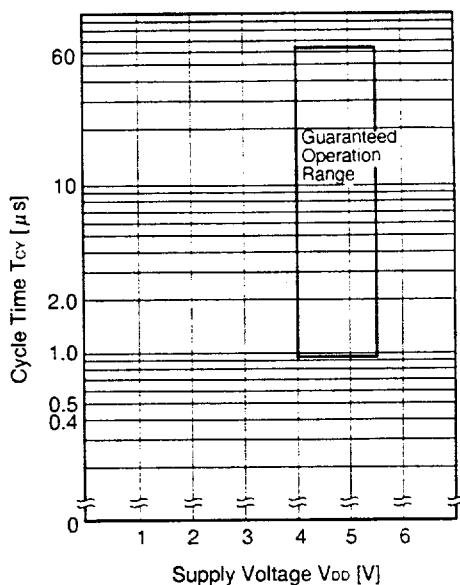
2. When oscillation mode selection register is set to 01H.

3. f_{sam} can be selected as $f_{xx}/2^N$, $f_{xx}/32$, $f_{xx}/64$, or $f_{xx}/128$ by bits 0 and 1 (SCS0 and SCS1) of the sampling clock selection register (N = 0 to 4).**Remarks** 1. f_{xx} : Main system clock frequency (f_x or $f_x/2$)2. f_x : Main system clock oscillator frequency

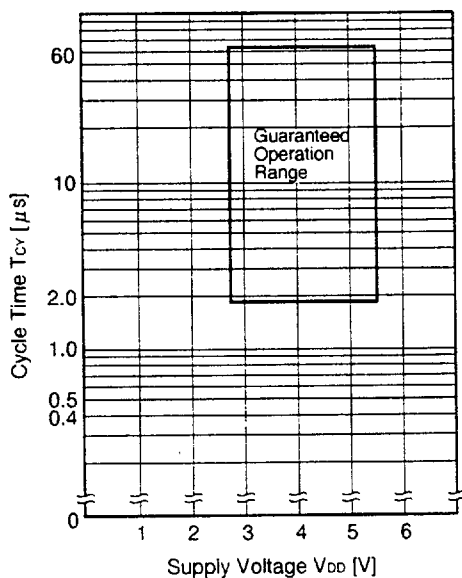
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 0, MCS = 0) Operation)



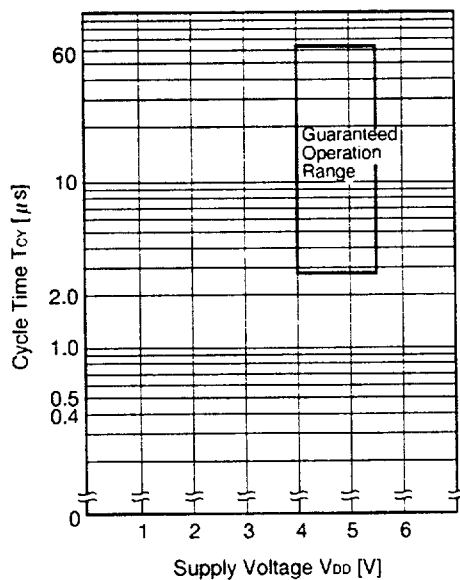
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 0, MCS = 0) Operation)



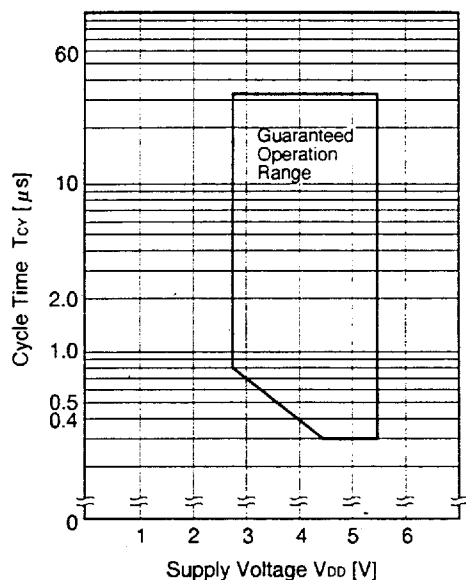
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 1, MCS = 0) Operation)



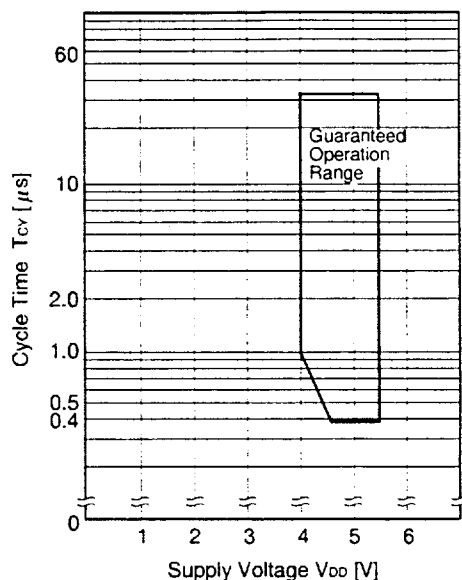
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 1, MCS = 0) Operation)



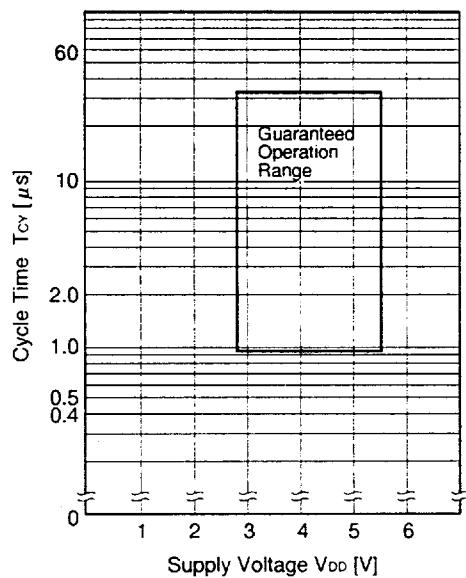
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 0, MCS = 1) Operation)



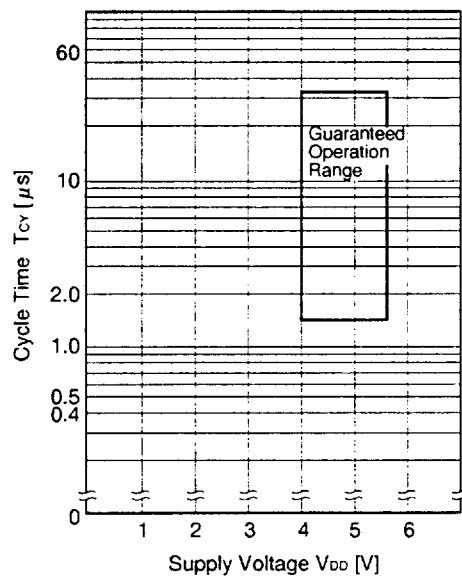
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 0, MCS = 1) Operation)



T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 1, MCS = 1) Operation)



T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 1, MCS = 1) Operation)



(2) Read/Write Operations

(a) When MCS = 1, PCC2 to PCC0 = 000B ($T_A = -40$ to $+85$ °C, $V_{DD} = 4.5$ to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}		0.85t _{cy} - 50		ns
Address setup time	t _{ADS}		0.85t _{cy} - 50		ns
Address hold time	t _{ADH}		50		ns
Data input time from address	t _{ADD1}			(2.85+2n)t _{cy} -80	ns
	t _{ADD2}			(4+2n)t _{cy} -100	ns
Data input time from $\overline{RD}\downarrow$	t _{RDD1}			(2+2n)t _{cy} -100	ns
	t _{RDD2}			(2.85+2n)t _{cy} -100	ns
Read data hold time	t _{RDH}		0		ns
$\overline{RD}$ low-level width	t _{RDL1}		(2+2n)t _{cy} -60		ns
	t _{RDL2}		(2.85+2n)t _{cy} -60		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t _{RDW1}			0.85t _{cy} - 50	ns
	t _{RDW2}			2t _{cy} - 60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t _{WRWT}			2t _{cy} - 60	ns
$\overline{WAIT}$ low-level width	t _{WTL}		(1.15+2n)t _{cy}	(2+2n)t _{cy}	ns
Write data setup time	t _{WDS}		(2.85+2n)t _{cy} -100		ns
Write data hold time	t _{WDH}		20		ns
$\overline{WR}$ low-level width	t _{WRL1}		(2.85+2n)t _{cy} -60		ns
$\overline{RD}\downarrow$ delay time from ASTB $\downarrow$	t _{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB $\downarrow$	t _{ASTWR}		0.85t _{cy} +20		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t _{RDAST}		0.85t _{cy} -10	1.15t _{cy} +20	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t _{RDADH}		0.85t _{cy} -50	1.15t _{cy} +50	ns
Write data output time from $\overline{RD}\uparrow$	t _{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t _{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t _{WRADH}		0.85t _{cy}	1.15t _{cy} +40	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t _{WTRD}		1.15t _{cy} +40	3.15t _{cy} +40	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t _{WTWR}		1.15t _{cy} +30	3.15t _{cy} +30	ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register
 2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register
 3. t_{cy} = T_{cy}/4
 4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$t_{cy} - 80$		ns
Address setup time	t_{ADS}		$t_{cy} - 80$		ns
Address hold time	t_{ADH}		$0.4t_{cy} - 10$		ns
Data input time from address	t_{ADD1}			$(3+2n)t_{cy} - 160$	ns
	t_{ADD2}			$(4+2n)t_{cy} - 200$	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(1.4+2n)t_{cy} - 70$	ns
	t_{RDD2}			$(2.4+2n)t_{cy} - 70$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.4+2n)t_{cy} - 20$		ns
	t_{RDL2}		$(2.4+2n)t_{cy} - 20$		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$t_{cy} - 100$	ns
	t_{RDWT2}			$2t_{cy} - 100$	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{cy} - 100$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1+2n)t_{cy}$	$(2+2n)t_{cy}$	ns
Write data setup time	t_{WDS}		$(2.4+2n)t_{cy} - 60$		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.4+2n)t_{cy} - 20$		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t_{ASTRD}		$0.4t_{cy} - 30$		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t_{ASTWR}		$1.4t_{cy} - 30$		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$t_{cy} - 10$	$t_{cy} + 20$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$t_{cy} - 50$	$t_{cy} + 50$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		$0.4t_{cy} - 20$		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		t_{cy}	$t_{cy} + 60$	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.6t_{cy} + 180$	$2.6t_{cy} + 180$	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.6t_{cy} + 120$	$2.6t_{cy} + 120$	ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register
 2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register
 3. $t_{cy} = T_{cy}/4$
 4. n indicates the number of waits.

(3) Serial Interface ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	$V_{DD} = 4.5$ to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}	$V_{DD} = 4.5$ to 5.5 V	$t_{KCY1}/2-50$			ns
	t_{KL1}		$t_{KCY1}/2-100$			ns
SIO setup time (vs. $\overline{SCK0}\uparrow$)	t_{SIK1}	$V_{DD} = 4.5$ to 5.5 V	100			ns
			150			ns
SIO hold time (vs. $\overline{SCK0}\uparrow$)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}\downarrow$	t_{KSO1}	$C = 100\text{pF}$ ^{Note}			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	$V_{DD} = 4.5$ to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}	$V_{DD} = 4.5$ to 5.5 V	400			ns
	t_{KL2}		800			ns
SIO setup time (vs. $\overline{SCK0}\uparrow$)	t_{SIK2}		100			ns
SIO hold time (vs. $\overline{SCK0}\uparrow$)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}\downarrow$	t_{KSO2}	$C = 100\text{pF}$ ^{Note}			300	ns
$\overline{SCK0}$ rise, fall time	t_{r2} , t_{f2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{\text{SCK0}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY3}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH3}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY3}}/2-50$			ns
	t_{KL3}		$t_{\text{KCY3}}/2-100$			ns
SB0, SB1 setup time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{SIK3}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			300			ns
SB0, SB1 hold time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{SI3}		$t_{\text{KCY3}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO3}	$R = 1\text{k}\Omega,$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	0	250	ns
		$C = 100\text{pF}$ Note		0	1000	ns
SB0, SB1 $\downarrow$ from $\overline{\text{SCK0}}\uparrow$	t_{KSB}		t_{KCY3}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1 $\downarrow$	t_{SBK}		t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY3}			ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{\text{SCK0}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY4}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH4}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	400			ns
	t_{KL4}		1600			ns
SB0, SB1 setup time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{SIK4}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			300			ns
SB0, SB1 hold time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{SI4}		$t_{\text{KCY4}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO4}	$R = 1\text{k}\Omega,$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	0	300	ns
		$C = 100\text{pF}$ Note		0	1000	ns
SB0, SB1 $\downarrow$ from $\overline{\text{SCK0}}\uparrow$	t_{KSB}		t_{KCY4}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1 $\downarrow$	t_{SBK}		t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY4}			ns
$\overline{\text{SCK0}}$ rise, fall time	$t_{\text{R4}},$ t_{F4}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY5}	$R = 1\text{k}\Omega$, $C = 100\text{pF}$ ^{Note}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	1600			ns
				3200			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH5}			$t_{\text{KCY5}}/2 - 160$			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL5}			$t_{\text{KCY5}}/2 - 50$			ns
SB0, SB1 setup time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{SIK5}		$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	300			ns
				350			ns
SB0, SB1 hold time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{HSI5}			600			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSOS}			0		300	ns

Note R and C are the $\overline{\text{SCK0}}$, SB0 and SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY6}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH6}		650			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL6}		800			ns
SB0, SB1 setup time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{SIK6}		100			ns
SB0, SB1 hold time (vs. $\overline{\text{SCK0}}\uparrow$)	t_{HSI6}		$t_{\text{KCY6}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSOS6}	$R = 1\text{k}\Omega$, $C = 100\text{pF}$ ^{Note}	0		300	ns
$\overline{\text{SCK0}}$ rise, fall time	t_{R6} , t_{F6}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the $\overline{\text{SCK0}}$, SB0 and SB1 output line load resistance and load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY7}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH7}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY7}}/2-50$			ns
	t_{KL7}		$t_{\text{KCY7}}/2-100$			ns
SI1 setup time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{SIK7}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI1 hold time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO7}	$C = 100\text{pF}$ Note			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY8}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH8}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	400			ns
	t_{KL8}		800			ns
SI1 setup time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{SIK8}		100			ns
SI1 hold time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{KSI8}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO8}	$C = 100\text{pF}$ Note			300	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{r8}},$ t_{f8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(iii) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{\text{SCK1}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY9}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH9}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY9}}/2-50$			ns
	t_{KL9}		$t_{\text{KCY9}}/2-100$			ns
SI1 setup time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{SIK9}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI1 hold time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{KS19}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO9}	$C = 100 \text{ pF}^{\text{Note}}$ $V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$			300	ns
$\text{STB}\uparrow$ from $\overline{\text{SCK1}}\uparrow$	t_{SBD}		$t_{\text{KCY9}}/2-100$		$t_{\text{KCY9}}/2+100$	ns
Strobe signal high-level width	t_{SBW}		$t_{\text{KCY9}}-30$		$t_{\text{KCY9}}+30$	ns
Busy signal setup time (vs. busy signal detection timing)	t_{BVS}		100			ns
Busy signal hold time (vs. busy signal detection timing)	t_{BYH}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
$\overline{\text{SCK1}}\downarrow$ from busy inactivation	t_{SPS}				$2t_{\text{KCY9}}$	ns

Note C is the SO1 output line load capacitance.

(iv) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{\text{SCK1}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY10}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH10}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	400			ns
	t_{KL10}		800			ns
SI1 setup time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{SIK10}		100			ns
SI1 hold time (vs. $\overline{\text{SCK1}}\uparrow$)	t_{KS110}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO10}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{R10}},$ t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{\text{SCK2}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY11}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK2}}$ high-/low-level width	$t_{\text{KH11}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY11}}/2-50$			ns
	t_{KL11}		$t_{\text{KCY11}}/2-100$			ns
SI2 setup time (vs. $\overline{\text{SCK2}}\uparrow$)	t_{SIK11}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI2 hold time (vs. $\overline{\text{SCK2}}\uparrow$)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO11}	$C = 100\text{pF}$ Note			300	ns

Note C is the SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK2}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY12}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK2}}$ high-/low-level width	$t_{\text{KH12}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	400			ns
	t_{KL12}		800			ns
SI2 setup time (vs. $\overline{\text{SCK2}}\uparrow$)	t_{SIK12}		100			ns
SI2 hold time (vs. $\overline{\text{SCK2}}\uparrow$)	t_{KSI12}		400			ns
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO12}	$C = 100\text{pF}$ Note			300	ns
$\overline{\text{SCK2}}$ rise, fall time	$t_{\text{R12}},$ t_{F12}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO2 output line load capacitance.

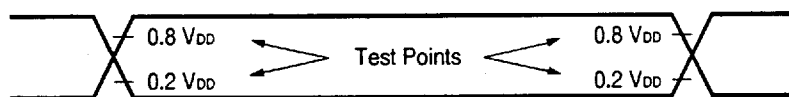
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V _{DD} = 4.5 to 5.5 V			78125	bps
					39063	bps

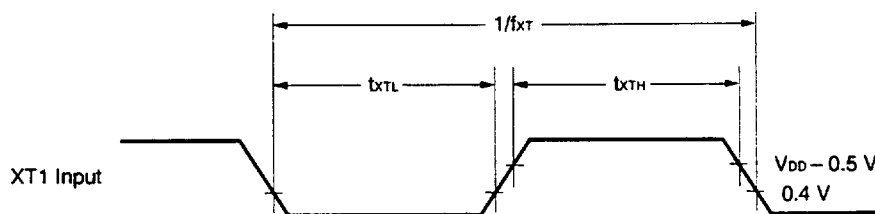
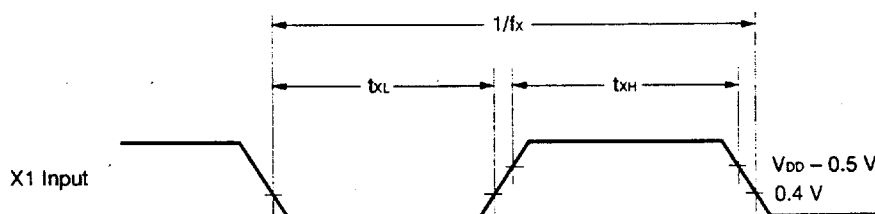
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t _{KCY13}	V _{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK high-/low-level width	t _{KH13} , t _{KL13}	V _{DD} = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V _{DD} = 4.5 to 5.5 V			39063	bps
					19531	bps
SCK rise, fall time	t _{R13} , t _{F13}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

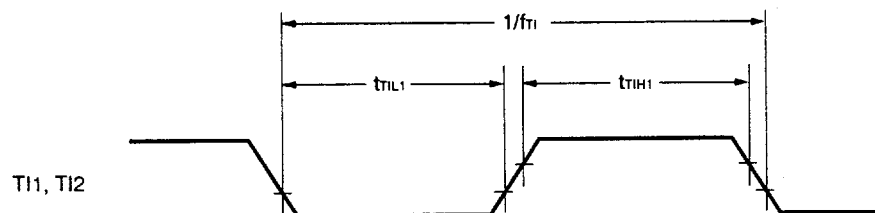
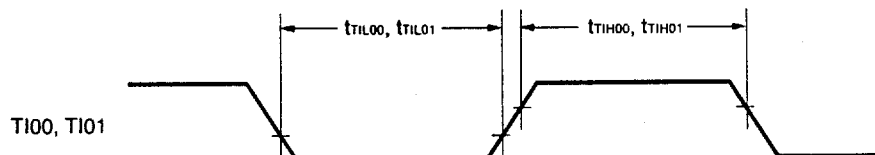
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

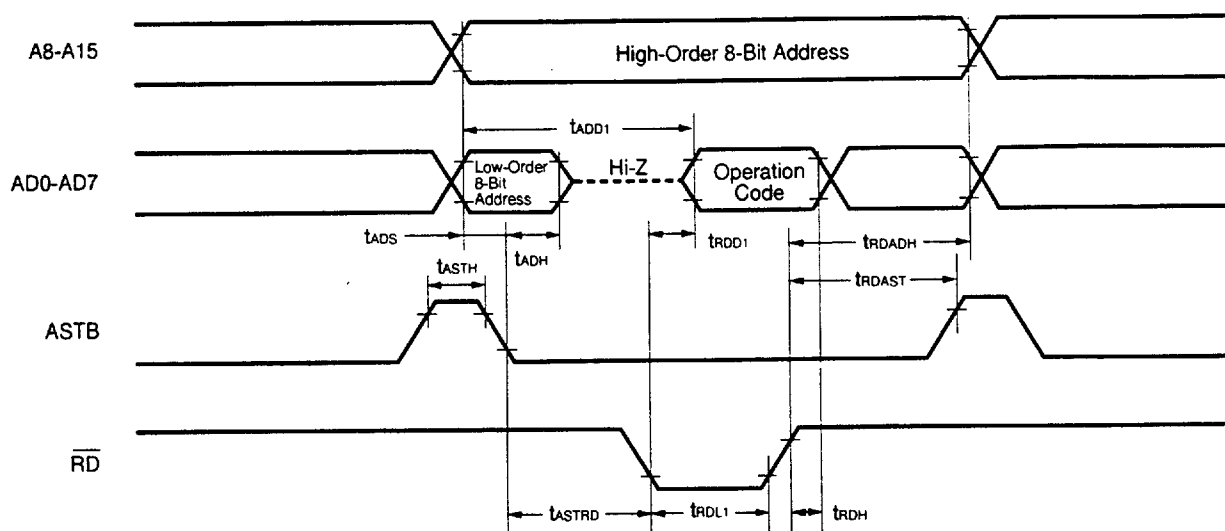


T1 Timing

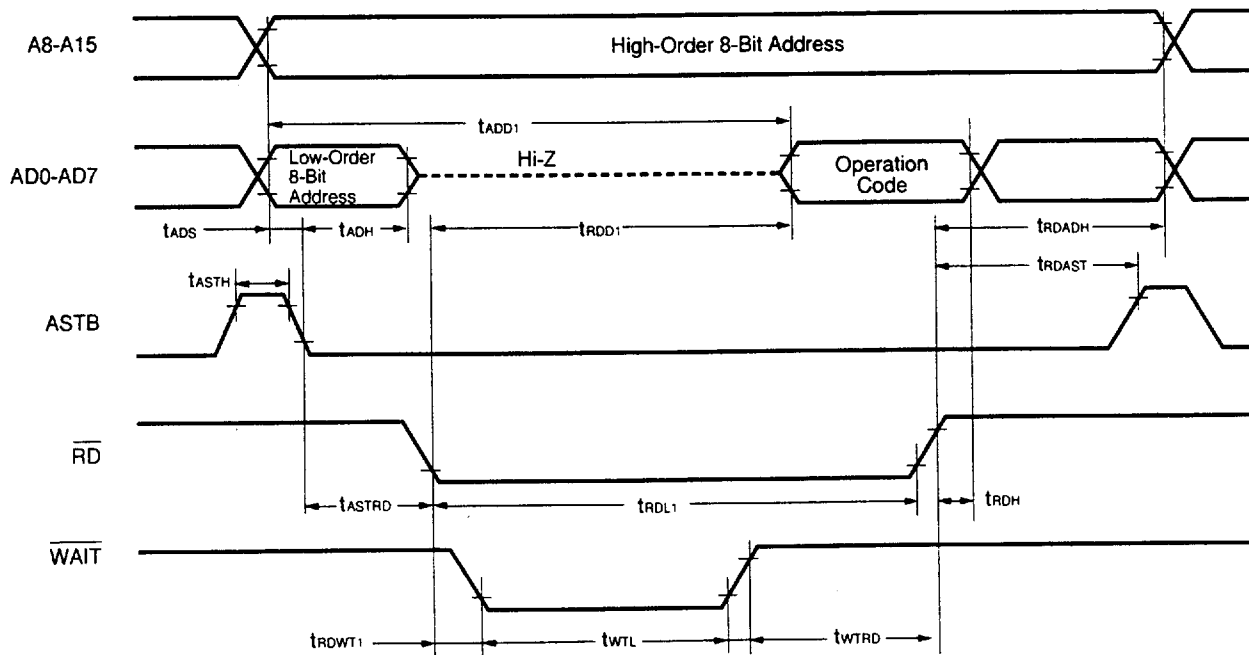


Read/Write Operations

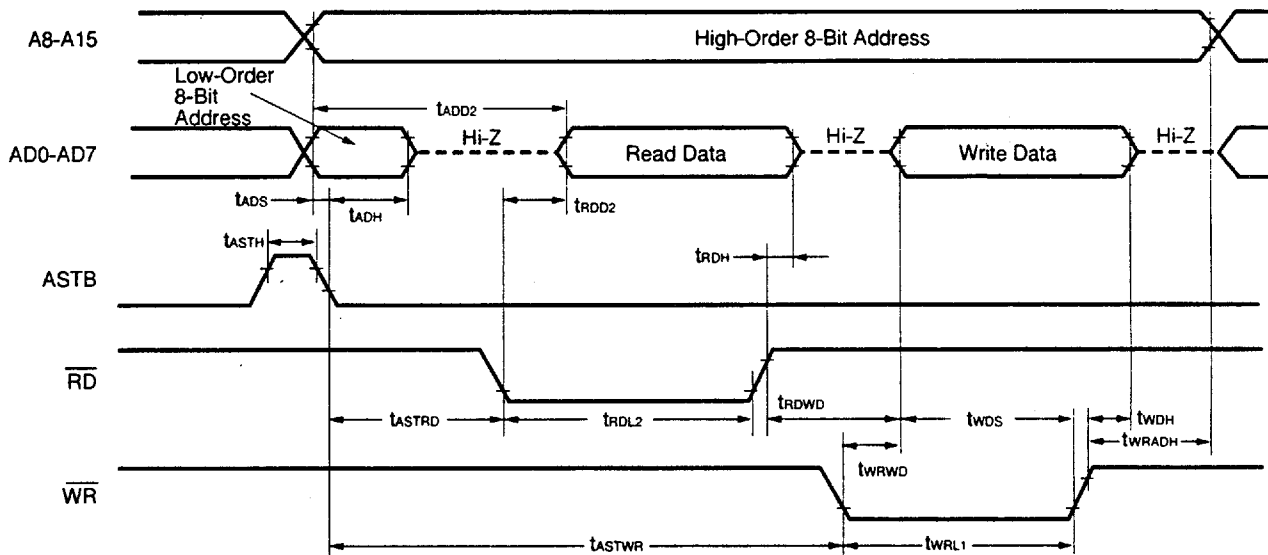
External fetch (no wait):



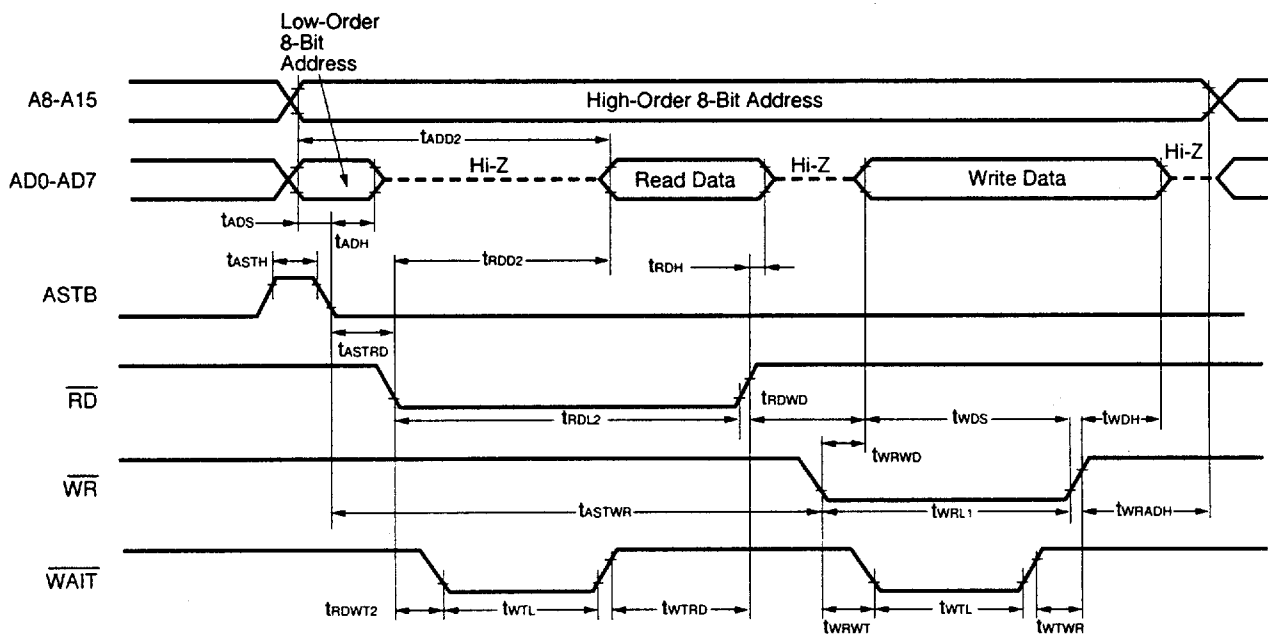
External fetch (wait insertion):



External data access (no wait):

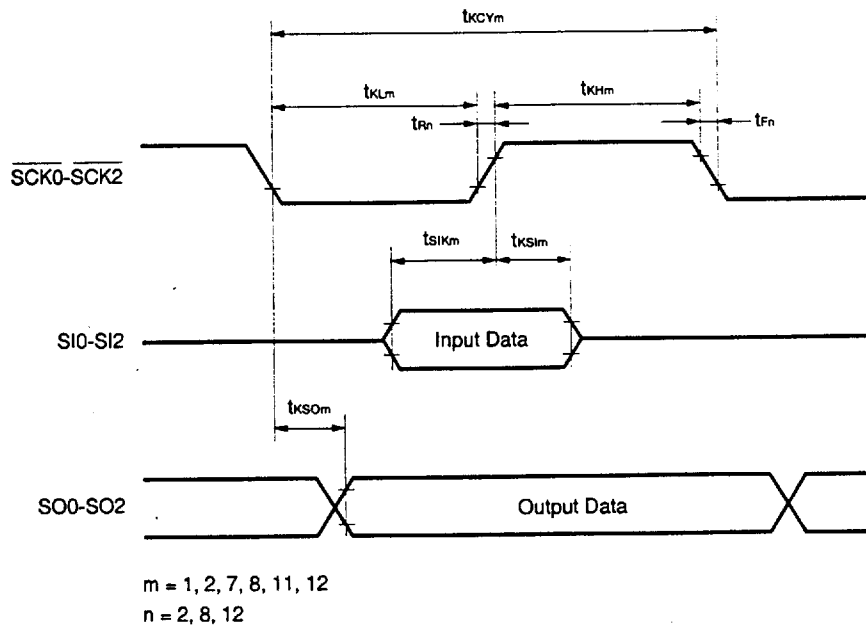


External data access (wait insertion):

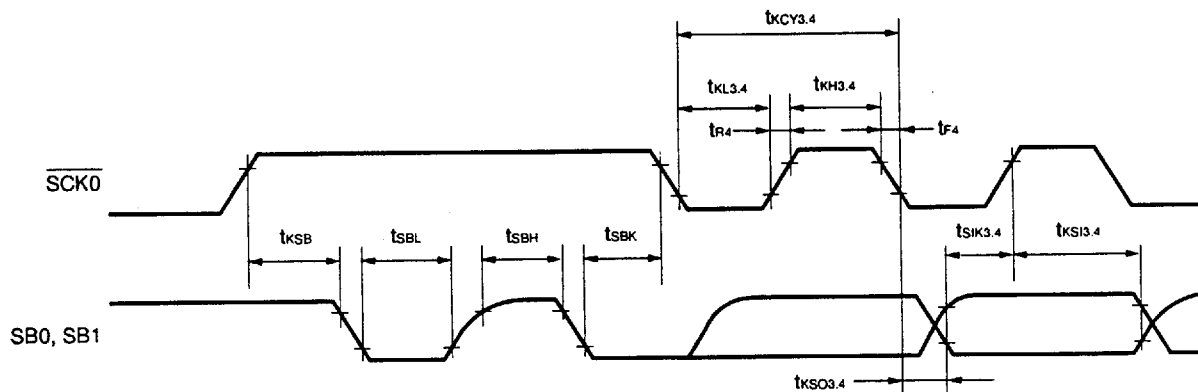


Serial Transfer Timing

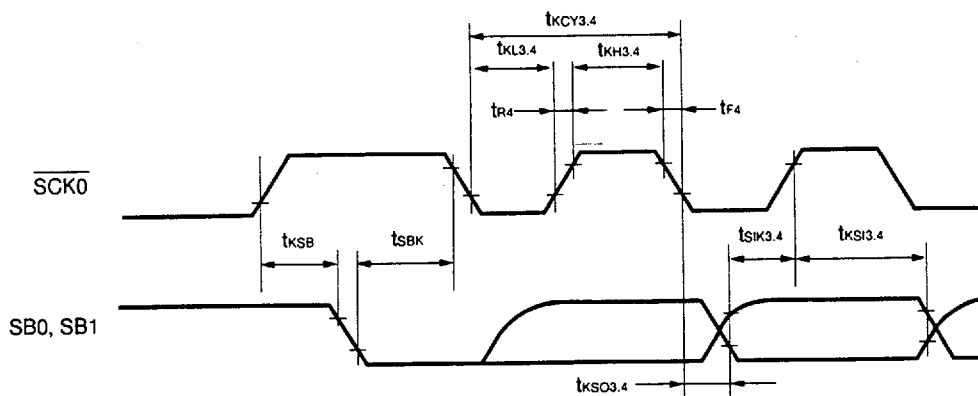
3-wire serial I/O mode:



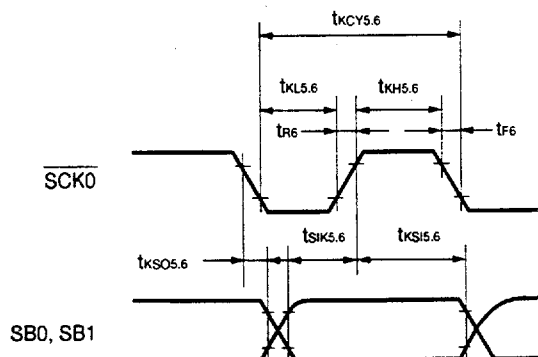
SBI mode (bus release signal transfer):



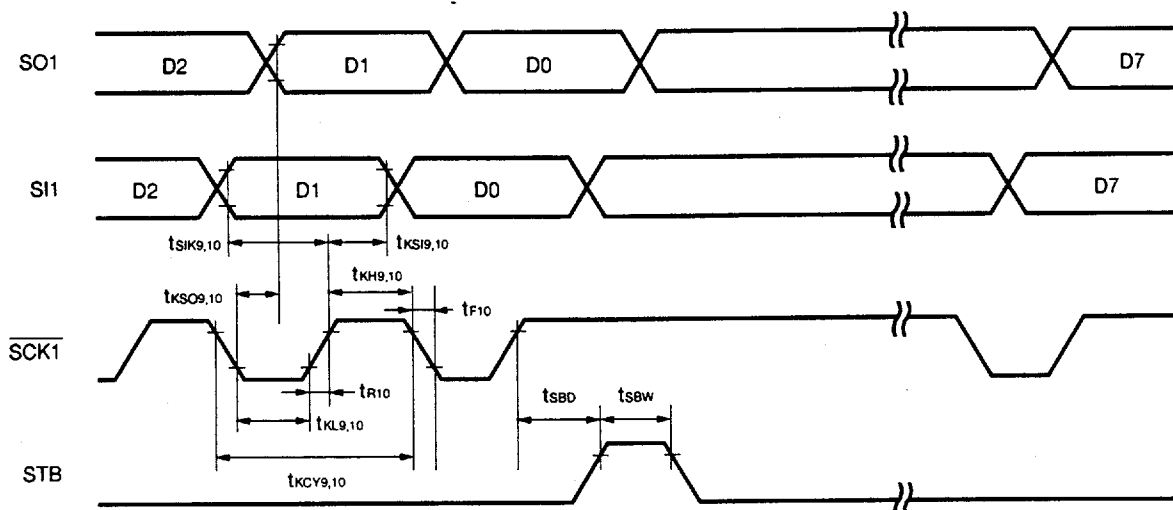
SBI mode (command signal transfer):



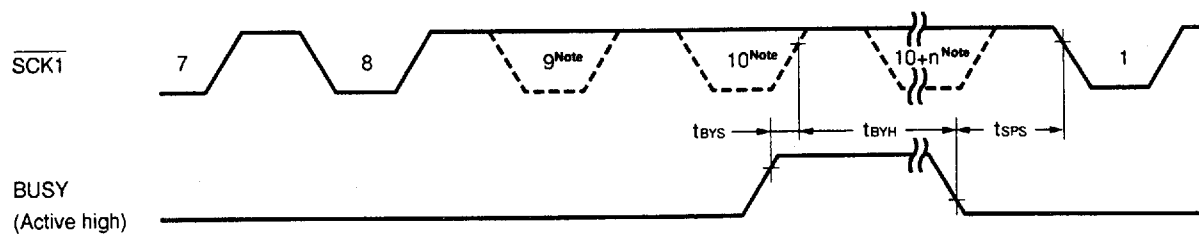
2-wire serial I/O mode:



Automatic transmission/reception function 3-wire serial I/O mode:

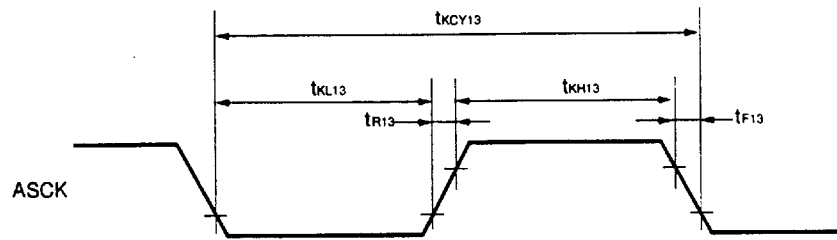


Automatic transmission/reception function 3-wire serial I/O mode (busy processing):



Note The signal is not actually low here, but is represented in this way to show the timing.

UART mode (external Clock Input):



A/D Converter Characteristics ($T_A = -40$ to $+85$ °C, $AV_{DD} = V_{DD} = 2.7$ to 5.5 V, $AV_{SS} = V_{SS} = 0$ V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error ^{Note}		IEAD = 00H				1.8	%
		IEAD = 01H	$V_{DD} = 4.5$ to 5.5 V		2.2	3.4	%
					2.6	3.8	%
Conversion time	t_{CONV}			19.1		200	μ s
Sampling time	t_{SAMP}			$12/f_{xx}$			μ s
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}			2.7		AV_{DD}	V
AV_{REF0} - AV_{SS} resistance	R_{AIREF0}			4	14		k Ω

Note Excluding quantization error ($\pm 1/2$ LSB). Shown as a percentage of the full scale value.

Remarks 1. f_{xx} : Main system clock frequency (f_x or $f_x/2$)
 2. f_x : Main system clock oscillator frequency

D/A Converter Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V, $AV_{SS} = V_{SS} = 0$ V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		$R = 2\text{ M}\Omega$ ^{Note1}				1.2	%
		$R = 4\text{ M}\Omega$ ^{Note1}				0.8	%
		$R = 10\text{ M}\Omega$ ^{Note1}				0.6	%
Setting time		$C = 30\text{ pF}$ ^{Note 1}	$AV_{REF} = 4.5$ to 5.5 V			10	μ s
						15	μ s
Output resistor	R_{O0}	DACS0 = 55H			10		k Ω
	R_{O1}	DACS1 = 55H			10		k Ω
Analog reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF1} current	I_{AREF1}	Note2				1.5	mA

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance.
 2. Value for one D/A converter channel.

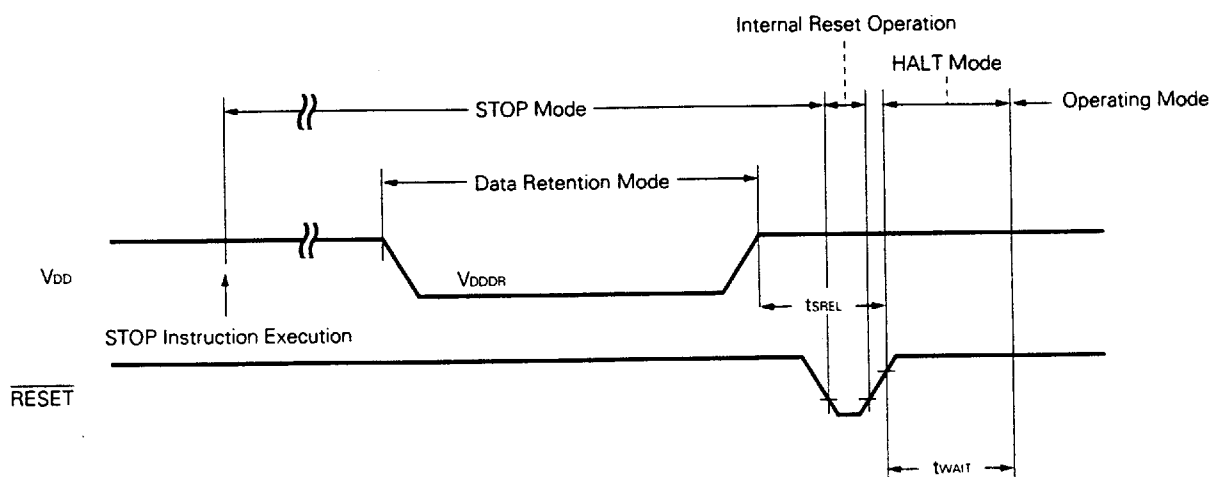
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS ($T_A = -40$ to $+85$ °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	$V_{DDDR} = 2.0$ V Subsystem clock stopped, feedback resistor disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		Note		ms

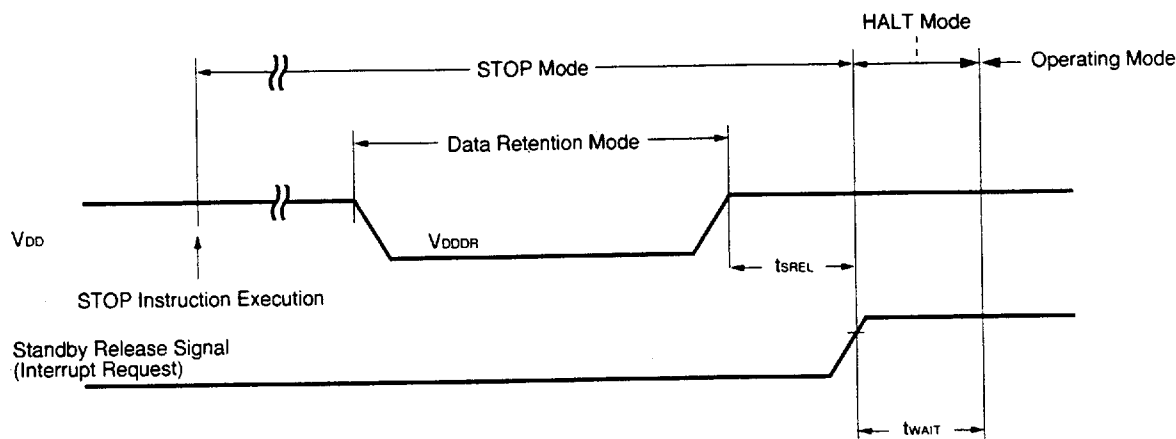
Note $2^{12}/f_{xx}$, or $2^{14}/f_{xx}$ through $2^{17}/f_{xx}$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register.

Remark f_{xx} : Main system clock frequency
 f_x : Main system clock oscillation frequency

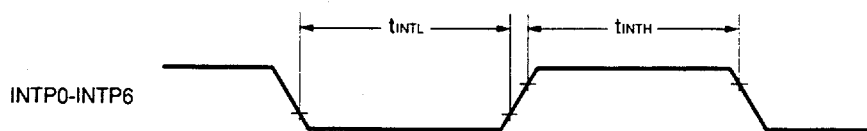
Data Retention Timing (STOP mode release by $\overline{RESET}$)



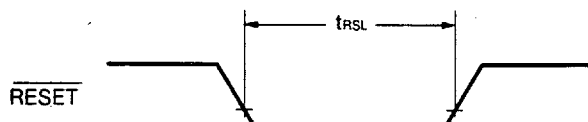
Data Retention Timing (STOP mode release by standby release signal: interrupt signal)



Interrupt Input Timing



RESET Input Timing



IEBus Controller Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
IEBus controller system clock frequency	f_s	When using mode 0, †Note 1		5.91	6.00	6.09	MHz
				6.20	6.29	6.39	MHz
		When using mode 2		5.97	6.00	6.03	MHz
				6.26	6.29	6.32	MHz
Driver delay time (TX output → bus line)		$C = 50\text{ pF}$ †Note 2	$f_s = 6.00\text{ MHz}$			1.6	μs
			$f_s = 6.29\text{ MHz}$			1.5	μs
Receiver delay time (Bus line → RX input)		$f_s = 6.00\text{ MHz}$				0.75	μs
		$f_s = 6.29\text{ MHz}$				0.7	μs
Propagation delay time on the bus		$f_s = 6.00\text{ MHz}$				0.9	μs
		$f_s = 6.29\text{ MHz}$				0.85	μs

Notes 1. For the values in the second row, the IEBus standards are not satisfied.

2. C is the TX output line load capacitance.

PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM Write Mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		$0.7 V_{DD}$		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		$0.3 V_{DD}$	V
Output voltage high	V_{OH}	V_{OH}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
Output voltage low	V_{OL}	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	PGM = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 5.0 \pm 0.5\text{ V}$, $V_{PP} = V_{DD} \pm 0.6\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		$0.7 V_{DD}$		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		$0.3 V_{DD}$	V
Output voltage high	V_{OH1}	V_{OH1}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
	V_{OH2}	V_{OH2}	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$			V
Output voltage low	V_{OL}	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
Output leakage current	I_{LO}	I_{LO}	$0 \leq V_{OUT} \leq V_{DD}$, $\overline{OE} = V_{IH}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		$V_{DD} - 0.6$	V_{DD}	$V_{DD} + 0.6$	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	$V_{PP} = V_{DD}$			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$			50	mA

Note Corresponding μ PD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (vs. $\overline{\text{OE}}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{\text{OE}}$ setup time	t_{OES}	t_{OES}		2			μs
CE setup time (vs. $\overline{\text{OE}}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (vs. $\overline{\text{OE}}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (vs. $\overline{\text{OE}}\uparrow$)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (vs. $\overline{\text{OE}}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{\text{OE}}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (vs. $\overline{\text{OE}}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (vs. $\overline{\text{OE}}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{\text{OE}}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{\text{OE}}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
PGM setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{\text{CE}}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{\text{OE}}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (vs. $\overline{\text{PGM}}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{\text{OE}}$ setup time	t_{OES}	t_{OES}		2			μs
CE setup time (vs. $\overline{\text{PGM}}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (vs. $\overline{\text{PGM}}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (vs. $\overline{\text{OE}}\uparrow$)	t_{AH}	t_{AH}		2			μs
Input data hold time (vs. $\overline{\text{PGM}}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{\text{OE}}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (vs. $\overline{\text{PGM}}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (vs. $\overline{\text{PGM}}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{\text{OE}}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{\text{OE}}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol

(2) PROM Read Mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 5.0 \pm 0.5\text{ V}$, $V_{PP} = V_{DD} \pm 0.6\text{ V}$)

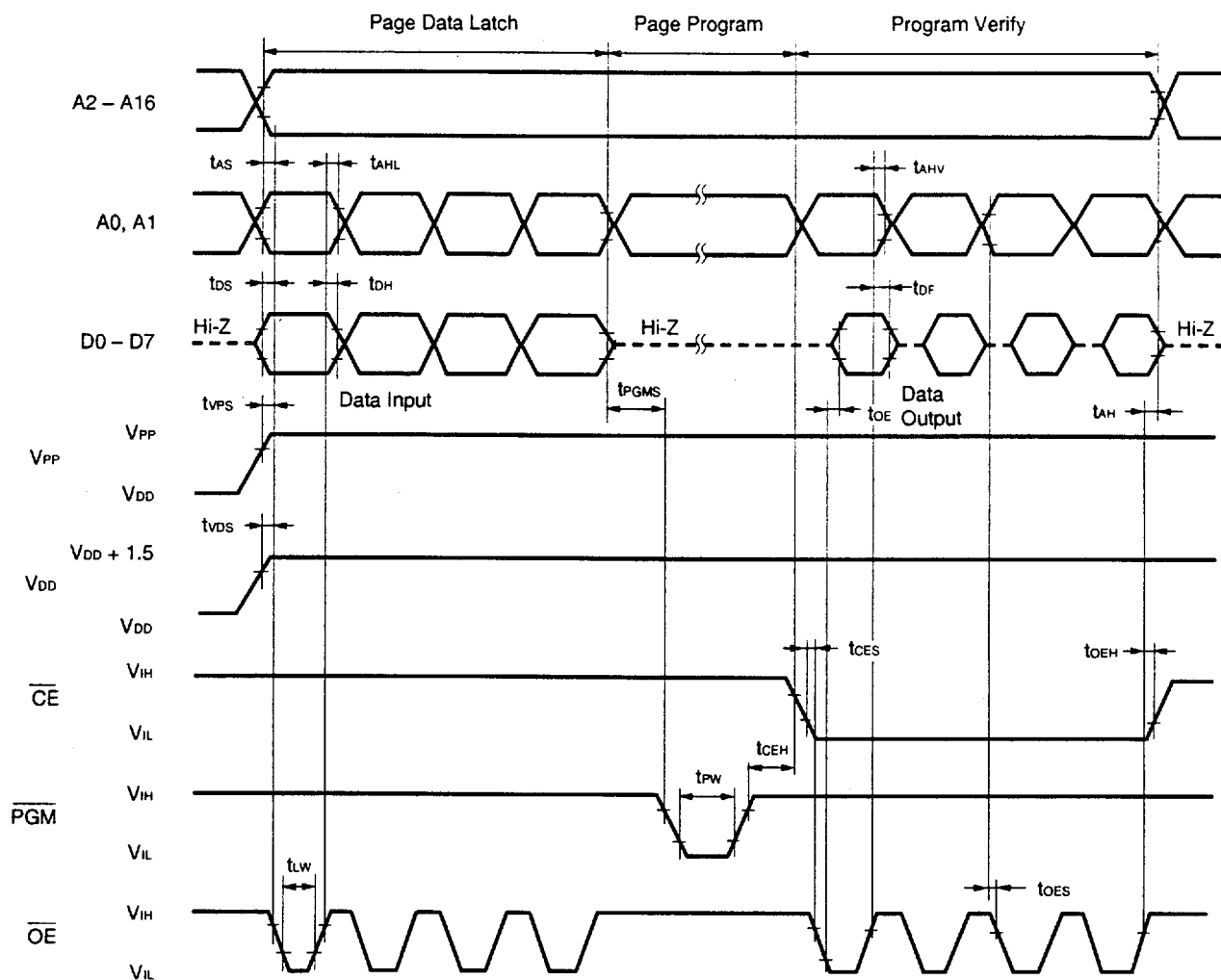
Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			800	ns
Data output delay time from $\overline{CE}\downarrow$	t_{CE}	t_{CE}	$\overline{OE} = V_{IL}$			800	ns
Data output delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}	$\overline{CE} = V_{IL}$			200	ns
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}	$\overline{CE} = V_{IL}$	0		60	ns
Data hold time from address	t_{OH}	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note Corresponding μ PD27C1001A symbol

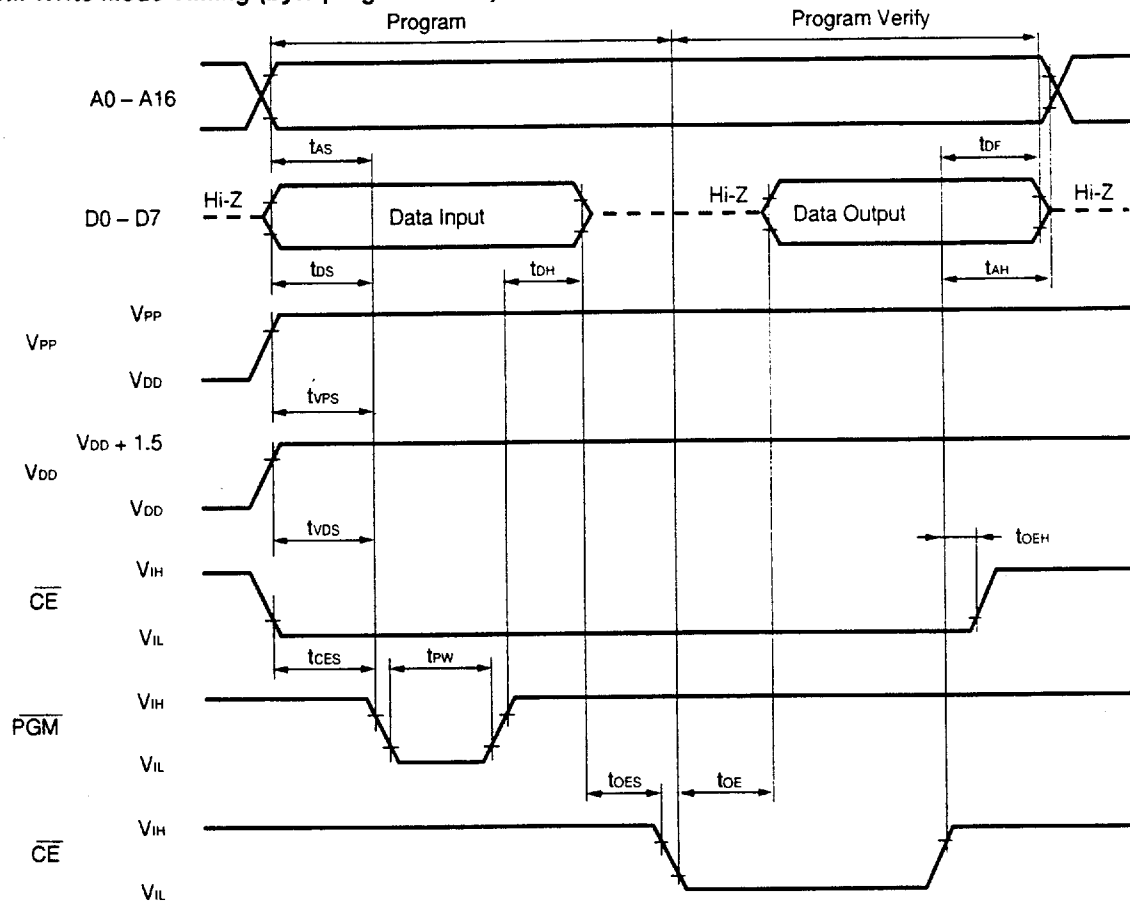
(3) PROM Programming Mode Setting ($T_A = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programing mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)

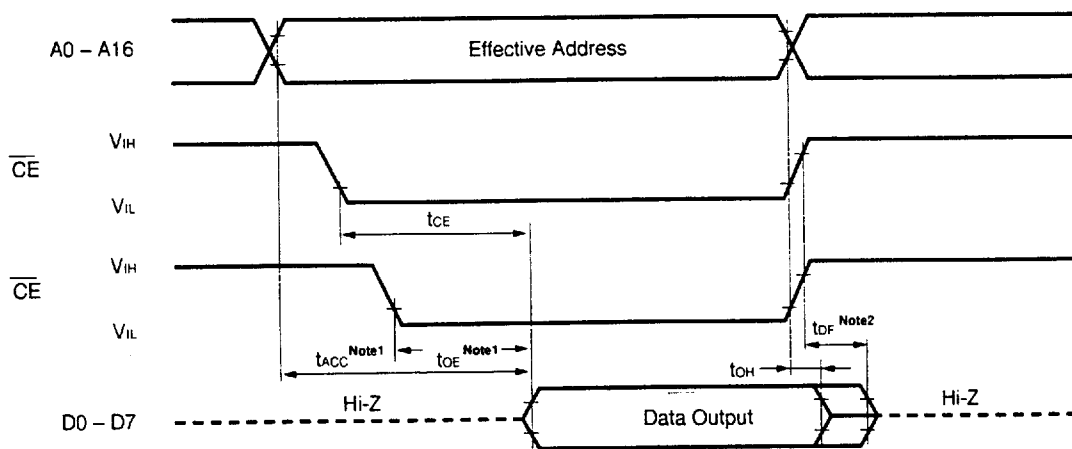


PROM Write Mode Timing (byte program mode)



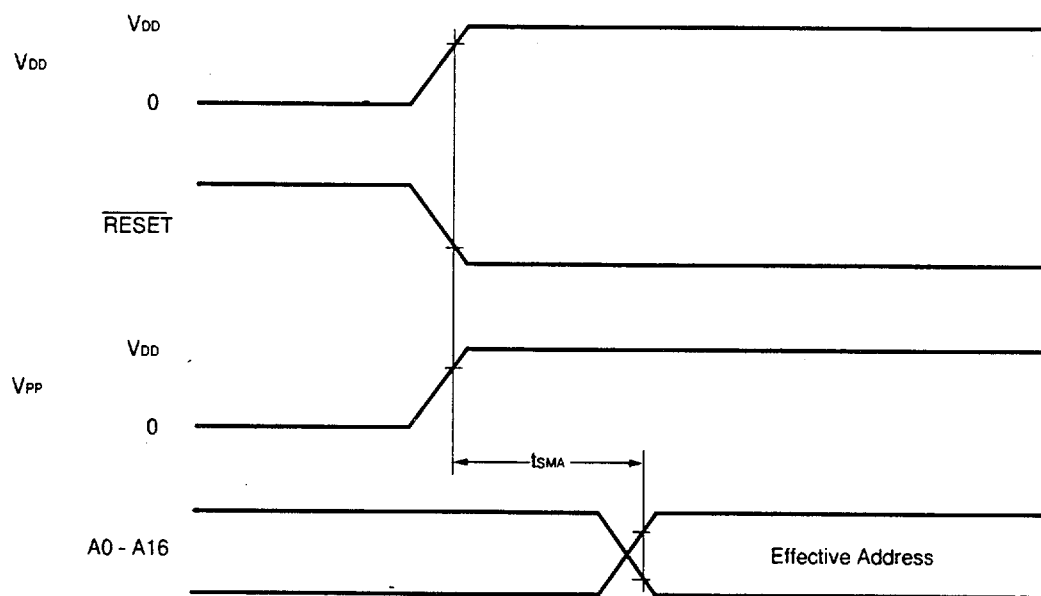
- Cautions**
1. V_{DD} should be applied before V_{PP} , and cut after V_{PP} .
 2. V_{PP} should not exceed +13.5 V including overshoot.
 3. Disconnection during application of $\pm 12.5V$ to V_{PP} may have an adverse effect on reliability.

PROM Read Mode Timing



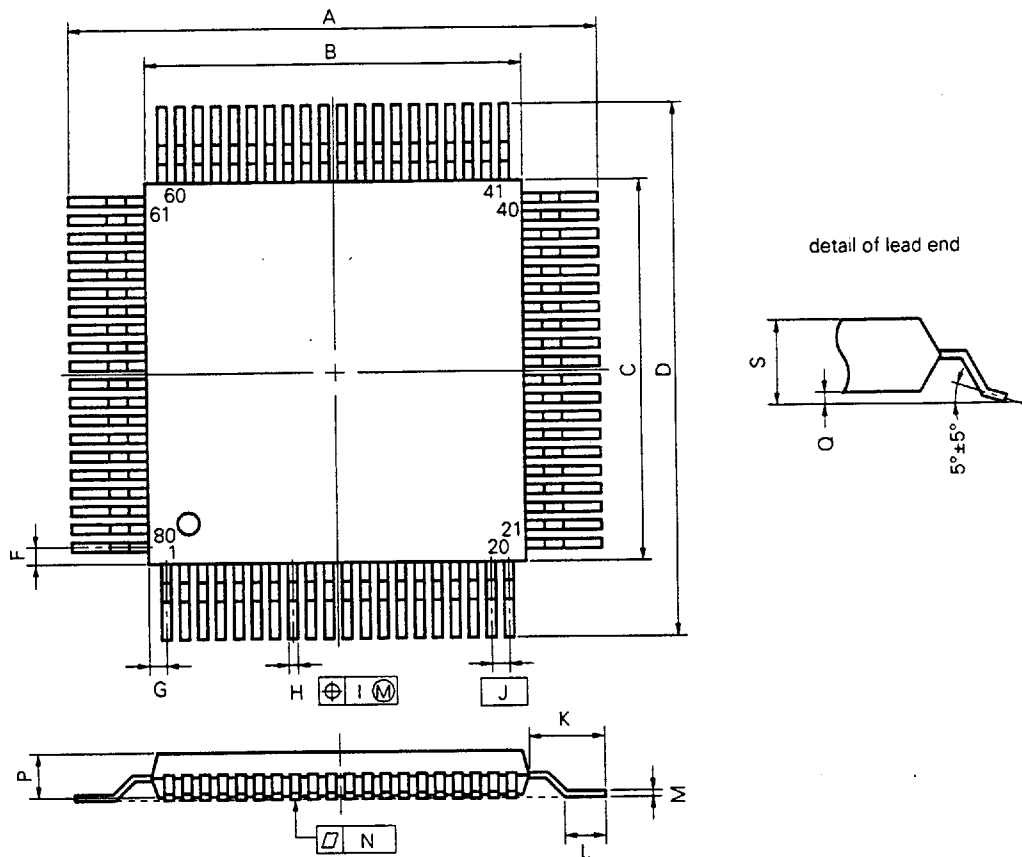
- Notes**
1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of $t_{ACC} - t_{OE}$.
 2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH} .

PROM Programming Mode Setting Timing



10. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (□14)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

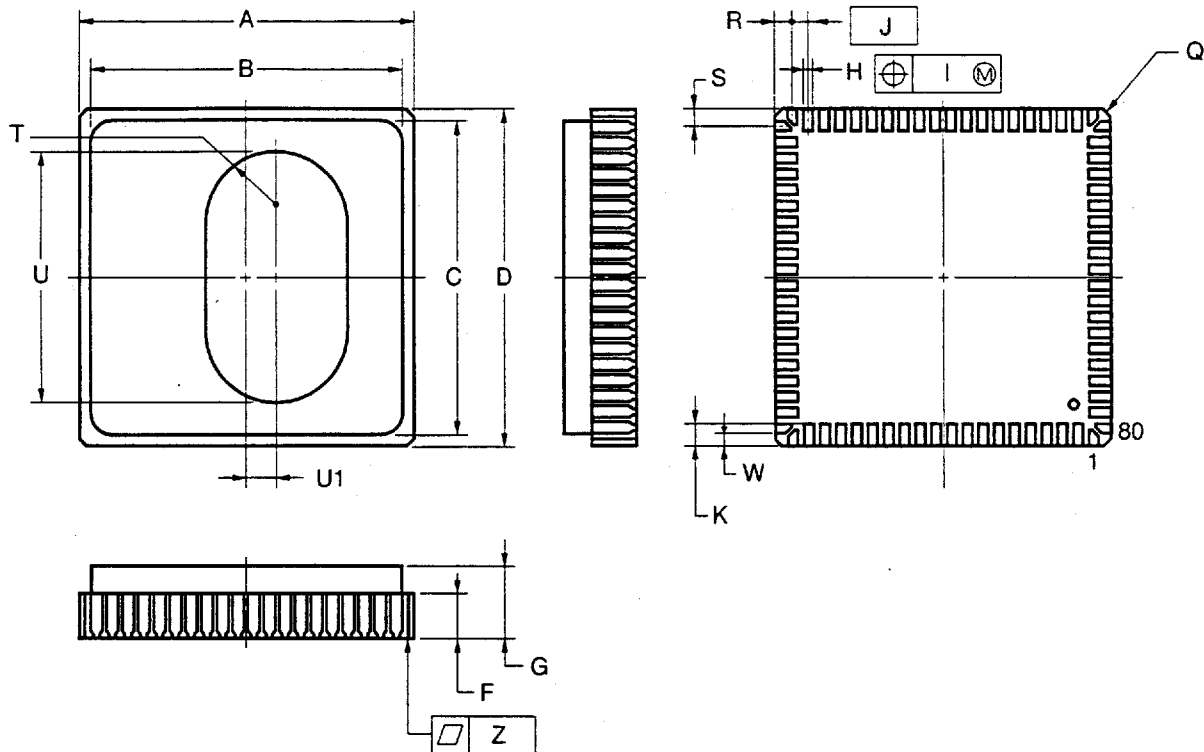
Remark

Dimensions and materials of ES products are different from those of mass-production products.

S80GC-65-3B9-3

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN CERAMIC WQFN



NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.18	0.551 ^{+0.008} _{-0.007}
B	13.0	0.512
C	13.0	0.512
D	14.0±0.18	0.551 ^{+0.008} _{-0.007}
F	1.84	0.072
G	3.56 MAX.	0.141 MAX.
H	0.40±0.10	0.018 ^{+0.004} _{-0.005}
I	0.06	0.003
J	0.65 (T.P.)	0.026 (T.P.)
K	1.0±0.15	0.039 ^{+0.007} _{-0.006}
Q	C0.3	C0.012
R	0.825	0.032
S	0.825	0.032
T	R3.0	R0.118
U	10.4	0.409
U1	1.4	0.055
W	0.75±0.15	0.030 ^{+0.006} _{-0.007}
Z	0.10	0.004

X80KK-65A

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μ PD78P098A.

Language processor software

RA78K/0 ^{Notes 1, 2, 3}	Common assembler package for 78K/0 series products
CC78K/0 ^{Notes 1, 2, 3}	Common C compiler package for 78K/0 series products
DF78098 ^{Notes 1, 2, 3}	Device file for μ PD78098 subseries
CC78K/0-L ^{Notes 1, 2, 3}	Common C compiler library source file for 78K/0 series products

PROM writing tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054KK-T	Programmer adapter connected to PG-1500
PG-1500 controller ^{Notes 1, 2}	Control program for PG-1500

Debugging tools

IE-78000-R	Common in-circuit emulator for 78K/0 series products
IE-78000-R-BK	Common break board for 78K/0 series products
IE-78098-R-EM	Emulation board for evaluation of μ PD78098 subseries
EP-78230GC-R	Common emulation probe for μ PD78234 subseries
EV-9200GC-80	Socket mounted on board of user system designed for 80-pin plastic QFP
EV-9900	Jig used to remove μ PD78P098AKK-T from EV-9200GC-80
SD78K/0 ^{Notes 1, 2}	Screen debugger for IE-78000-R
SM78K0 ^{Notes 4, 5}	Common system simulator for 78K/0 series products
DF8098 ^{Notes 1, 2, 4, 5}	Device file for μ PD78098 subseries

Real-time OS

RX78K/0 ^{Notes 1, 2, 3}	Real-time OS for 78K/0 series
MX78K0 ^{Notes 1, 2, 3}	OS for 78K/0 series

Notes 1. PC-9800 series (MS-DOS™) base

2. IBM PC/AT™ (PC DOS™) base

3. HP9000 series 300™, HP9000 series 700™ (HP-UX™) base, SPARCstation™ (SunOS™) base, EWS-4800 series (EWS-UX/V) base

4. PC-9800 series (MS-DOS+Windows™) base

5. IBM PC/AT (PC DOS+Windows) base

Remark The RA78K/0, CC78K/0, SD78K/0, and SM78K0 are used with the DF78098.

Fuzzy inference development support systems

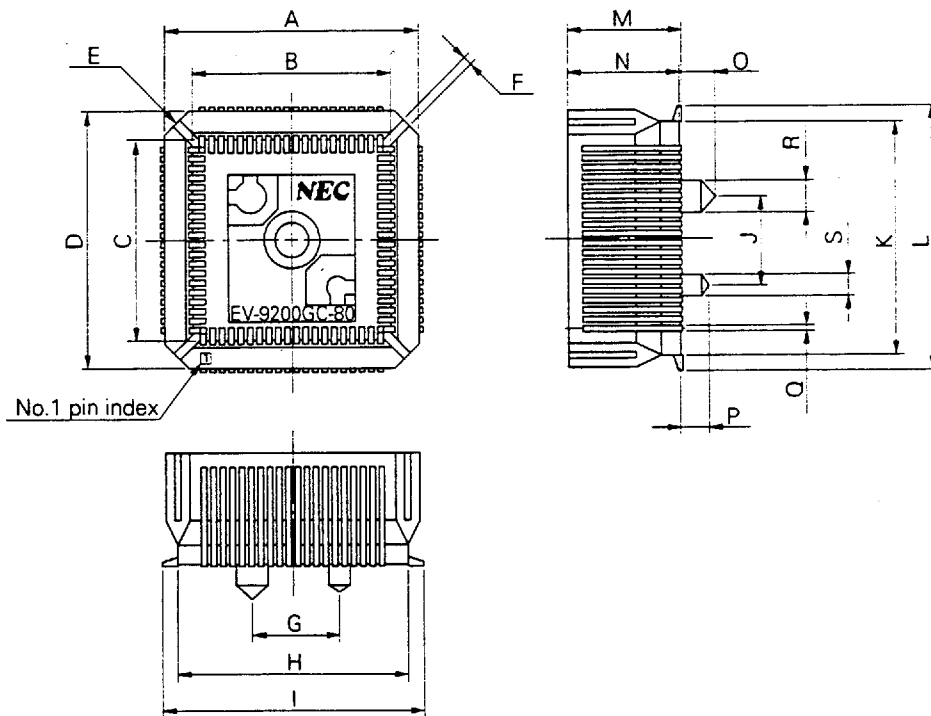
FE9000 ^{Note 1} /FE9200 ^{Note 2}	Fuzzy knowledge data creation tool
FT9080 ^{Note 1} /FT9085 ^{Note 3}	Translator
FI78K0 ^{Notes 1, 3}	Fuzzy inference module
FD78K0 ^{Notes 1, 3}	Fuzzy inference debugger

- Notes**
1. PC-9800 series (MS-DOS) base
 2. IBM PC/AT (PC DOS+Windows) base
 3. IBM PC/AT (PC DOS) base

Remark For development tools by the third parties, refer to 78K/0 Series Selection Guide (IF-1185).

DIMENSIONS AND RECOMMENDED MOUNTING PATTERN OF CONVERSION SOCKET

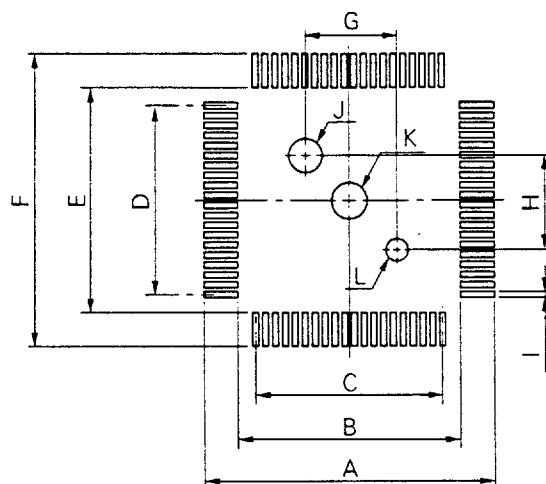
Figure A-1. Dimensions of EV-9200GC-80 (reference)



EV-9200GC-80-G0

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. Recommended Mounting Pattern of EV-9200GC-80 (reference)



EV-9200GC-80-P0

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.3$	$\phi 0.091$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

APPENDIX B. RELATED DOCUMENTS

Device-related documents

Document Name	Document Number	
	Japanese	English
μPD78098 Subseries User's Manual	IEU-854	IEU-1381
μPD78094, 78095, 78096, 78098A Data Sheet	U10146J	To be released soon
78K/0 Series User's Manual - Instruction	IEU-849	IEU-1372
78K/0 Series Instruction List	IEM-5522	-
78K/0 Series Instruction Set	IEM-5521	-
μPD78098 Subseries Special Function Register List	IEM-5591	-
78K/0 Series Application Note - Fundamental (III)	IEA-767	U10182E
78K/0 Series Application Note - Floating-point operation program	IEA-718	IEA-1289

Development tool-related documents (User's Manuals)

Document Name		Document Number	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	-
CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	-
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 series (MS-DOS) base		EEU-704	To be prepared
PG-1500 Controller IBM PC series (PC DOS) base		EEU-5008	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78098-R-EM		EEU-933	EEU-1473
EP-78230		EEU-985	EEU-1515
SM78K/0 System Simulator	Reference	EEU-5002	To be released soon
SD78K/0 Screen Debugger PC-9800 series (MS-DOS) base	Introduction	EEU-852	-
	Reference	EEU-816	-
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) base	Introduction	EEU-5024	EEU-1414
	Reference	EEU-993	EEU-1413

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition for designing.

Embedded software-related documents (User's Manuals)

Document Name		Document Number	
		Japanese	English
78K/0 Series Real-Time OS	Fundamental	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
78K/0 Series OS MX78K0	Fundamental	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Debugger		EEU-912	EEU-1458

Others

Document Name		Document Number	
		Japanese	English
Package Manual		IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual		IEI-616	IEI-1207
Quality Grade on NEC Semiconductor Devices		IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System		IEM-5068	—
Electrostatic Discharge (ESD) Test		MEM-539	—
Semiconductor Device Quality Guarantee Guide		MEI-603	MEI-1202
Microcontroller Related Product Guide - Other Manufacturers		MEI-604	—

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition for designing.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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* As of September 3, 1996

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