NEC

MOS INTEGRATED CIRCUIT

μPD464618AL, 464636AL

4M-BIT Bi-CMOS SYNCHRONOUS FAST STATIC RAM 256K-WORD BY 18-BIT / 128K-WORD BY 36-BIT LVTTL INTERFACE/REGISTER-REGISTER/LATE WRITE

Description

The μPD464618AL is a 262,144 words by 18 bits, and the μPD464636AL is a 131,072 words by 36 bits synchronous static RAM fabricated with advanced Bi-CMOS technology using N-channel memory cell.

This technology and unique peripheral circuits make the μPD464618AL and μPD464636AL a high-speed device. The μPD464618AL and μPD464636AL are suitable for applications which require high-speed, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

These are packaged in a 119-pin plastic BGA (Ball Grid Array).

Features

- Register to register synchronous operation
- LVTTL 3.3 V Input / Output levels
- Fast clock access time : 2.5 ns / 200 MHz, 3.0 ns / 166 MHz, 3.5 ns / 143 MHz
- Asynchronous output enable control : /G
- Single differential clock inputs
- Byte write control : /SBa (DQa1-9), /SBb (DQb1-9), /SBc (DQc1-9), /SBd (DQd1-9)
- Common I/O using three-state outputs
- Internally self-timed write cycle
- Late write with 1 dead cycle between Read-Write
- Boundary scan (JTAG) IEEE 1149.1 compatible
- Single +3.3 V power supply
- Sleep mode : ZZ(Enables sleep mode, active high)

Ordering Information

Part number	Access time	Clock frequency	Package
μPD464618ALS1-A5	2.5 ns	200 MHz	119-pin plastic BGA
μPD464618ALS1-A6	3.0 ns	166 MHz	
μPD464618ALS1-A7	3.5 ns	143 MHz	
μPD464636ALS1-A5	2.5 ns	200 MHz	
μPD464636ALS1-A6	3.0 ns	166 MHz	
μPD464636ALS1-A7	3.5 ns	143 MHz	

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The mark ★ shows major revised points.

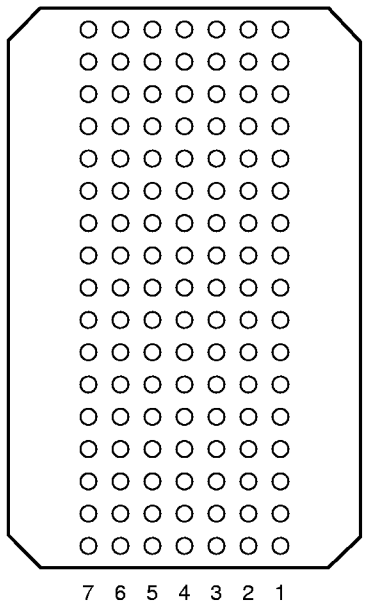
Pin Configurations

/xxx indicates active low signal.

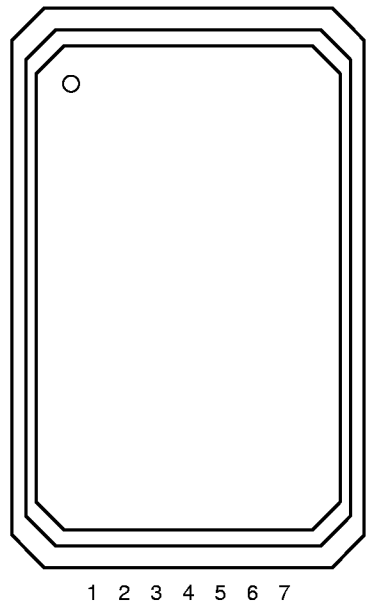
119-pin Plastic BGA (256K Words by 18 Bits Pin Assignment)

[μPD464618ALS1]

Bottom View



Top View



7	6	5	4	3	2	1		1	2	3	4	5	6	7
V_{DDQ}	SA2	SA6	NC	SA9	SA12	V_{DDQ}	A	V_{DDQ}	SA12	SA9	NC	SA6	SA2	V_{DDQ}
NC	NC	SA16	NC	SA17	NC	NC	B	NC	NC	SA17	NC	SA16	NC	NC
NC	SA3	SA7	V_{DD}	SA10	SA13	NC	C	NC	SA13	SA10	V_{DD}	SA7	SA3	NC
NC	DQa9	V_{SS}	NC	V_{SS}	NC	DQb1	D	DQb1	NC	V_{SS}	NC	V_{SS}	DQa9	NC
DQa8	NC	V_{SS}	/SS	V_{SS}	DQb2	NC	E	NC	DQb2	V_{SS}	/SS	V_{SS}	NC	DQa8
V_{DDQ}	DQa7	V_{SS}	/G	V_{SS}	NC	V_{DDQ}	F	V_{DDQ}	NC	V_{SS}	/G	V_{SS}	DQa7	V_{DDQ}
DQa6	NC	V_{SS}	NC	/SBb	DQb3	NC	G	NC	DQb3	/SBb	NC	V_{SS}	NC	DQa6
NC	DQa5	V_{SS}	NC	V_{SS}	NC	DQb4	H	DQb4	NC	V_{SS}	NC	V_{SS}	DQa5	NC
V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}	J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
DQa4	NC	V_{SS}	K	V_{SS}	DQb5	NC	K	NC	DQb5	V_{SS}	K	V_{SS}	NC	DQa4
NC	DQa3	/SBa	/K	V_{SS}	NC	DQb6	L	DQb6	NC	V_{SS}	/K	/SBa	DQa3	NC
V_{DDQ}	NC	V_{SS}	/SW	V_{SS}	DQb7	V_{DDQ}	M	V_{DDQ}	DQb7	V_{SS}	/SW	V_{SS}	NC	V_{DDQ}
NC	DQa2	V_{SS}	SA1	V_{SS}	NC	DQb8	N	DQb8	NC	V_{SS}	SA1	V_{SS}	DQa2	NC
DQa1	NC	V_{SS}	SA0	V_{SS}	DQb9	NC	P	NC	DQb9	V_{SS}	SA0	V_{SS}	NC	DQa1
★ NC	SA4	V_{DD}	V_{DD}	V_{SS}	SA14	NC	R	NC	SA14	V_{SS}	V_{DD}	V_{DD}	SA4	NC
ZZ	SA5	SA8	NC	SA11	SA15	NC	T	NC	SA15	SA11	NC	SA8	SA5	ZZ
V_{DDQ}	NC	TDO	TCK	TDI	TMS	V_{DDQ}	U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

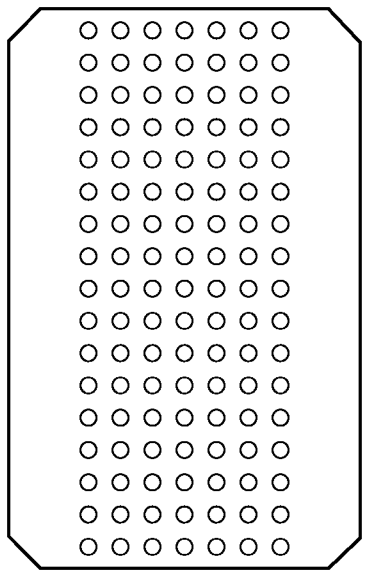
Pin Name and Functions [μPD464618ALS1]

Pin name	Description	Function
V_{DD}	Core Power Supply	Supplies power for RAM core
V_{SS}	Ground	
$V_{DD}Q$	Output Power Supply	Supplies power for output buffers
K, /K	Main Clock Input	
SA0 to SA17	Synchronous Address Input	
DQa1 to DQb9	Synchronous Data Input / Output	
/SS	Synchronous Chip Select	Logically selects SRAM
/SW	Synchronous Byte Write Enable	Write command
/SBa	Synchronous Byte "a" Write Enable	Write DQa1 to DQa9
/SBb	Synchronous Byte "b" Write Enable	Write DQb1 to DQb9
/G	Asynchronous Output Enable	Asynchronous input
ZZ	Sleep Mode Enable	Enables sleep mode, active high
NC	No Connection	
TMS	Test Mode Select (JTAG)	
TDI	Test Data Input (JTAG)	
TCK	Test Clock Input (JTAG)	
TDO	Test Data Output (JTAG)	

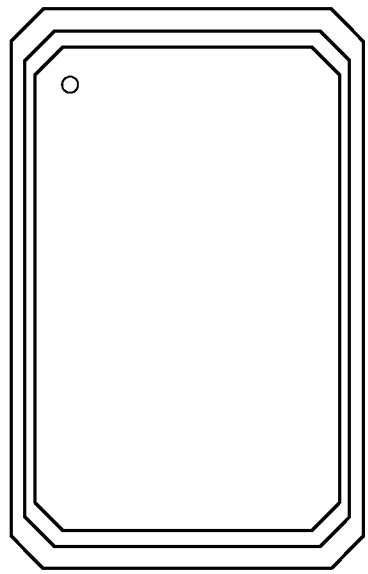
119-pin plastic BGA (128K Words by 36 Bits Pin Assignment)

[μPD464636ALS1]

Bottom View



Top View



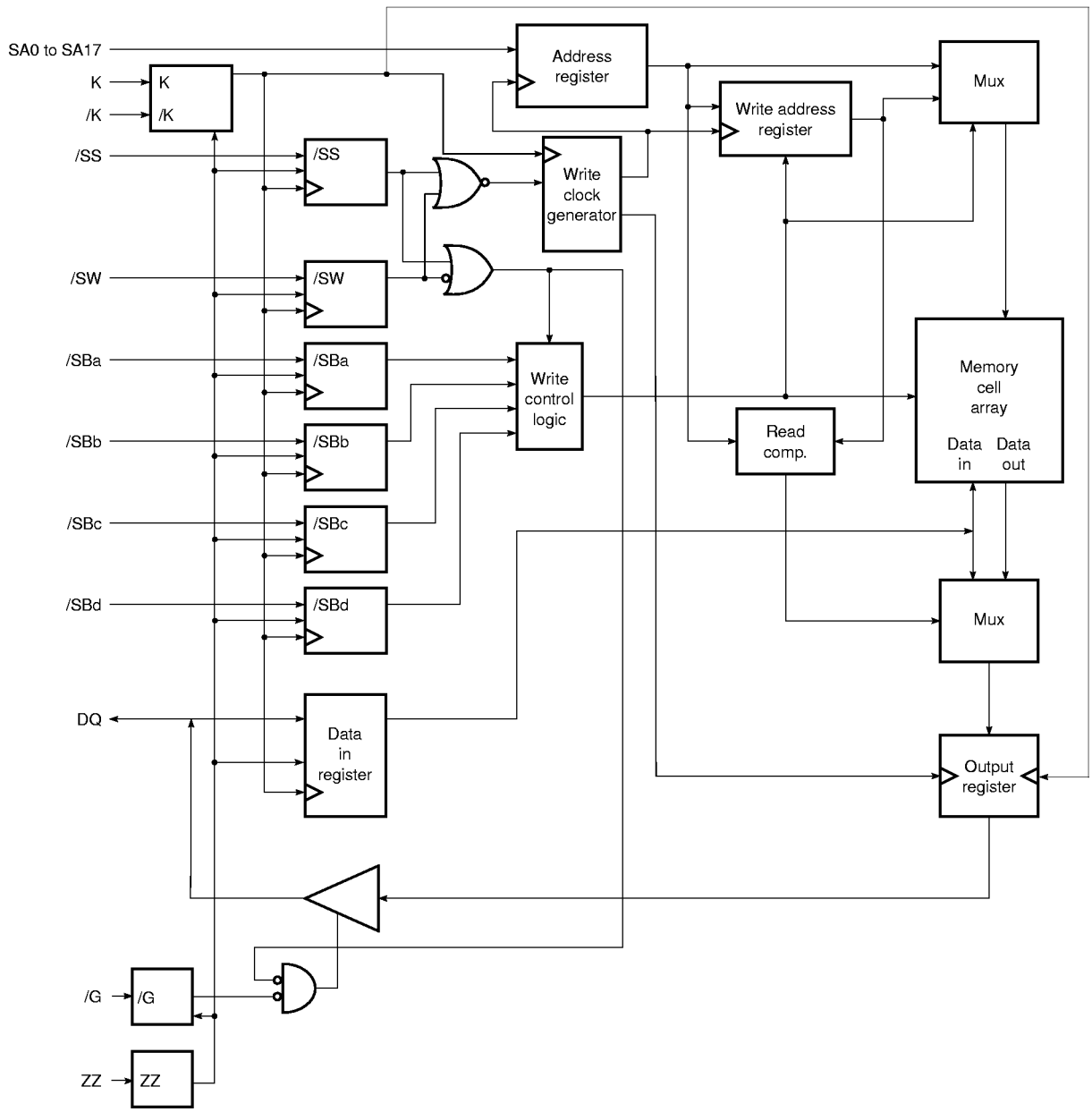
A B C D E F G H J K L M N P R T U

	7	6	5	4	3	2	1		1	2	3	4	5	6	7
	V_{DDQ}	SA2	SA5	NC	SA9	SA12	V_{DDQ}	A	V_{DDQ}	SA12	SA9	NC	SA5	SA2	V_{DDQ}
	NC	NC	SA15	NC	SA16	NC	NC	B	NC	NC	SA16	NC	SA15	NC	NC
	NC	SA3	SA6	V_{DD}	SA10	SA13	NC	C	NC	SA13	SA10	V_{DD}	SA6	SA3	NC
	DQb8	DQb9	V_{SS}	NC	V_{SS}	DQc9	DQc8	D	DQc8	DQc9	V_{SS}	NC	V_{SS}	DQb9	DQb8
	DQb6	DQb7	V_{SS}	/SS	V_{SS}	DQc7	DQc6	E	DQc6	DQc7	V_{SS}	/SS	V_{SS}	DQb7	DQb6
	V_{DDQ}	DQb5	V_{SS}	/G	V_{SS}	DQc5	V_{DDQ}	F	V_{DDQ}	DQc5	V_{SS}	/G	V_{SS}	DQb5	V_{DDQ}
	DQb3	DQb4	/SBb	NC	/SBc	DQc4	DQc3	G	DQc3	DQc4	/SBc	NC	/SBb	DQb4	DQb3
	DQb1	DQb2	V_{SS}	NC	V_{SS}	DQc2	DQc1	H	DQc1	DQc2	V_{SS}	NC	V_{SS}	DQb2	DQb1
	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}	J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
	DQa1	DQa2	V_{SS}	K	V_{SS}	DQd2	DQd1	K	DQd1	DQd2	V_{SS}	K	V_{SS}	DQa2	DQa1
	DQa3	DQa4	/SBa	/K	/SBd	DQd4	DQd3	L	DQd3	DQd4	/SBd	/K	/SBa	DQa4	DQa3
	V_{DDQ}	DQa5	V_{SS}	/SW	V_{SS}	DQd5	V_{DDQ}	M	V_{DDQ}	DQd5	V_{SS}	/SW	V_{SS}	DQa5	V_{DDQ}
	DQa6	DQa7	V_{SS}	SA1	V_{SS}	DQd7	DQd6	N	DQd6	DQd7	V_{SS}	SA1	V_{SS}	DQa7	DQa6
	DQa8	DQa9	V_{SS}	SA0	V_{SS}	DQd9	DQd8	P	DQd8	DQd9	V_{SS}	SA0	V_{SS}	DQa9	DQa8
★	NC	SA4	V_{DD}	V_{DD}	V_{SS}	SA14	NC	R	NC	SA14	V_{SS}	V_{DD}	V_{DD}	SA4	NC
	ZZ	NC	SA7	SA8	SA11	NC	NC	T	NC	NC	SA11	SA8	SA7	NC	ZZ
	V_{DDQ}	NC	TDO	TCK	TDI	TMS	V_{DDQ}	U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Name and Functions [μPD464636ALS1]

Pin name	Description	Function
V_{DD}	Core Power Supply	Supplies power for RAM core
V_{SS}	Ground	
$V_{DD}Q$	Output Power Supply	Supplies power for output buffers
K, /K	Main Clock	
SA0 to SA16	Synchronous Address Input	
DQa1 to DQd9	Synchronous Data Input / Output	
/SS	Synchronous Chip Select	Logically selects SRAM
/SW	Synchronous Byte Write Enable	Write command
/SBa	Synchronous Byte "a" Write Enable	Write DQa1 to DQa9
/SBb	Synchronous Byte "b" Write Enable	Write DQb1 to DQb9
/SBc	Synchronous Byte "c" Write Enable	Write DQc1 to DQc9
/SBd	Synchronous Byte "d" Write Enable	Write DQd1 to DQd9
/G	Asynchronous Output Enable	Asynchronous input
ZZ	Sleep Mode Enable	Enables sleep mode, active high
NC	No Connection	
TMS	Test Mode Select (JTAG)	
TDI	Test Data Input (JTAG)	
TCK	Test Clock Input (JTAG)	
TDO	Test Data Output (JTAG)	

★ Late Write Block Diagram



Synchronous Truth Table

ZZ	/SS	/SW	/SBa	/SBb	/SBc	/SBd	Mode	DQa1–9	DQb1–9	DQc1–9	DQd1–9	Power
L	H	x	x	x	x	x	Not selected	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Active
L	L	H	x	x	x	x	Read	Dout	Dout	Dout	Dout	Active
L	L	L	L	L	L	L	Write	Din	Din	Din	Din	Active
L	L	L	L	H	H	H	Write	Din	Hi-Z	Hi-Z	Hi-Z	Active
L	L	L	H	L	L	L	Write	Hi-Z	Din	Din	Din	Active
H	x	x	x	x	x	x	Sleep Mode	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Standby

Remark × : Don't care

Output Enable Truth Table

Mode	/G	DQ
Read	L	Dout
Read	H	Hi-Z
Sleep (ZZ=H)	x	Hi-Z
Write (/SW=L)	x	Hi-Z
Deselect (/SS=H)	x	Hi-Z

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		–0.5		+4	V	1
Output supply voltage	V_{DDQ}		–0.5		+4	V	1
Input voltage	V_{IN}		–0.5		V_{DD} + 0.5	V	1
Input / Output voltage	$V_{I/O}$		–0.5		V_{DD} + 0.5	V	1
Operating temperature	T_j		5		110	°C	2
Storage temperature	T_{stg}		–55		+125	°C	

Notes 1. –1.0 V MIN. (Pulse width 10% Tcyc)

2. T_j = Junction temperature

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_j = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Core supply voltage	V_{DD}		3.15	3.3	3.45	V
Output buffer supply voltage	V_{DDQ}		3.15	3.3	3.45	V
Low level input voltage	V_{IL}		–0.3 Note		+0.8	V
High level input voltage	V_{IH}		2.0		V_{DD}+0.3	V
PECL clock input high voltage	$V_{IH-PECL}$		2.135		2.420	V
PECL clock input low voltage	$V_{IL-PECL}$		1.490		1.825	V

Note –1.0 V MIN. (Pulse width 10% Tcyc)

Capacitance (T_A = 25 °C, f = 1 MHz)

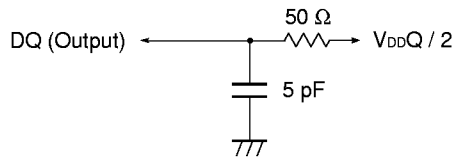
Parameter Note	Symbol	Test conditions	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V	6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	7	pF

Note These parameters are sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
	Input leakage current	I_{LI}	V_{IN} = 0 to V_{DD}		–5		+5	μA	
	DQ leakage current	I_{LO}	$V_{I/O}$ = 0 to $V_{DD}Q$, /SS = V_{IH} or /G = V_{IH}		–5		+5	μA	
★	Operating supply current	I_{CC}	/SS = V_{IL}, IDQ = 0 mA	μPD464618AL			470	mA	
			Cycle = 200 MHz	μPD464636AL			670		
	Sleep mode power supply current	I_{SBZZ}	ZZ = V_{IH}, All other inputs = V_{IH} or V_{IL}, Cycle = DC, IDQ = 0 mA				45	mA	
★	Power supply standby current	I_{SBSS}	/SS = V_{IH}, ZZ = V_{IL}, V_{IN} = V_{IH} or V_{IL}	μPD464618AL			450	mA	
			IDQ = 0 mA, Cycle = 200 MHz	μPD464636AL			650		
	Low level output voltage	V_{OL}	I_{OL} = 8 mA				0.4	V	1
	High level output voltage	V_{OH}	I_{OH} = –5 mA		2.4			V	1

Note 1. See figure.

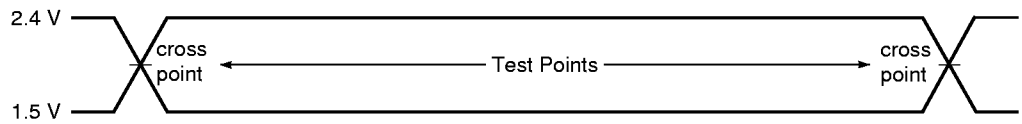


AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

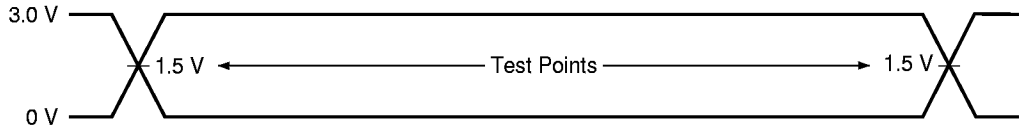
AC Characteristics Test Conditions

Input waveform (rise / fall time = 0.5 ns (20 to 80%))

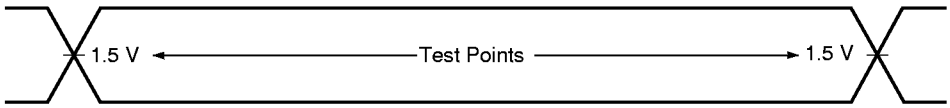
K,/K signals



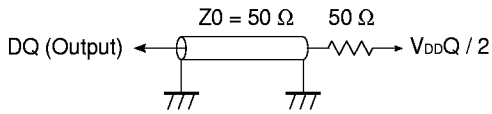
Other signals

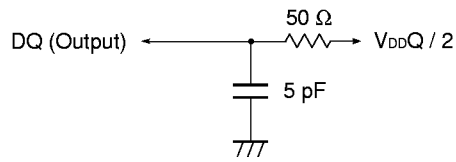


Output waveform



Output load

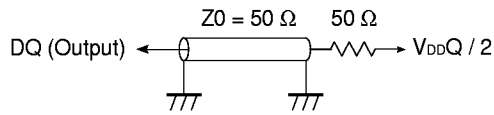




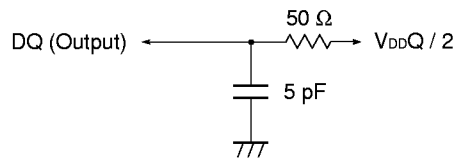
Single Differential Clock, Registered Input / Registered Output Mode

Parameter		Symbol	-A5 (200 MHz)		-A6 (166 MHz)		-A7 (143 MHz)		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time		t_{KHKH}	5.0	–	6.0	–	7.0	–	ns	
Clock phase time		t_{KHKL} /t_{KLKH}	1.5	–	2.0	–	2.5	–	ns	
Setup times	Address	t_{AVKH}	0.5	–	0.5	–	0.5	–	ns	
	Write data	t_{DVKH}								
	Write enable	t_{WVKH}								
	Chip select	t_{SVKH}								
Hold times	Address	t_{KHAX}	1.0	–	1.0	–	1.0	–	ns	
	Write data	t_{KHDX}								
	Write enable	t_{KHWX}								
	Chip select	t_{KHSX}								
Clock access time		t_{KHQV}	–	2.5	–	3.0	–	3.5	ns	1
★ K high to Q change		t_{KHQX}	0.7	–	0.7	–	0.7	–	ns	1
/G low to Q valid		t_{GLQV}	–	2.5	–	3.0	–	3.5	ns	1
/G low to Q change		t_{GLQX}	0.7	–	0.7	–	0.7	–	ns	1
/G high to Q Hi-Z		t_{GHQZ}	0.7	2.5	0.7	3.0	0.7	3.5	ns	2
K high to Q Hi-Z (/SW)		t_{KHQZ}	0.7	2.5	0.7	3.0	0.7	3.5	ns	2
★ K high to Q Hi-Z (/SS)		t_{KHQZ2}	0.7	2.5	0.7	3.0	0.7	3.5	ns	2
★ K high to Q Lo-Z		t_{KHQX2}	0.7	–	0.7	–	0.7	–	ns	2
Sleep mode recovery		t_{ZZR}	5.0	–	6.0	–	7.0	–	ns	
Sleep mode enable		t_{ZZE}	–	5.0	–	6.0	–	7.0	ns	

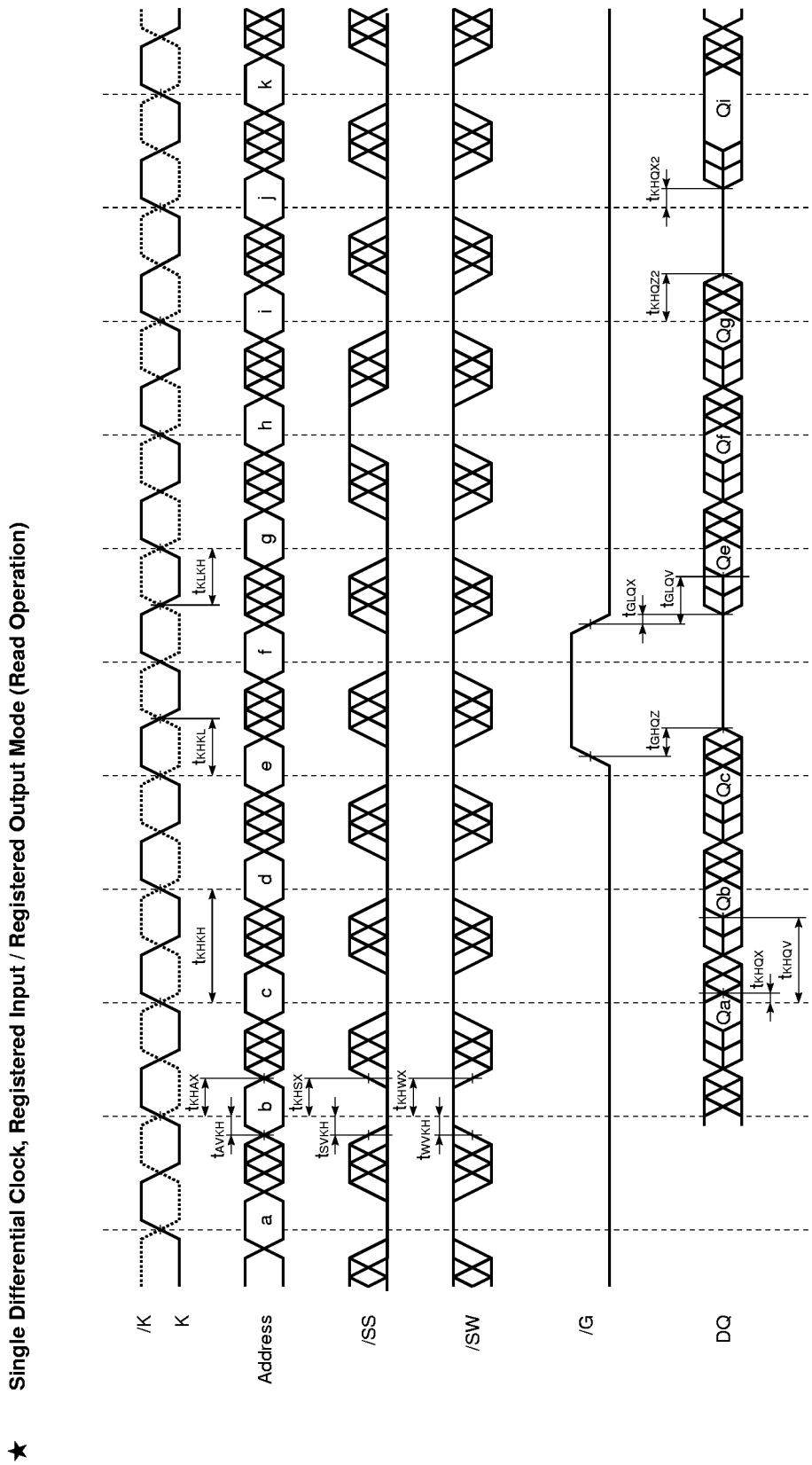
Notes 1. See figure.



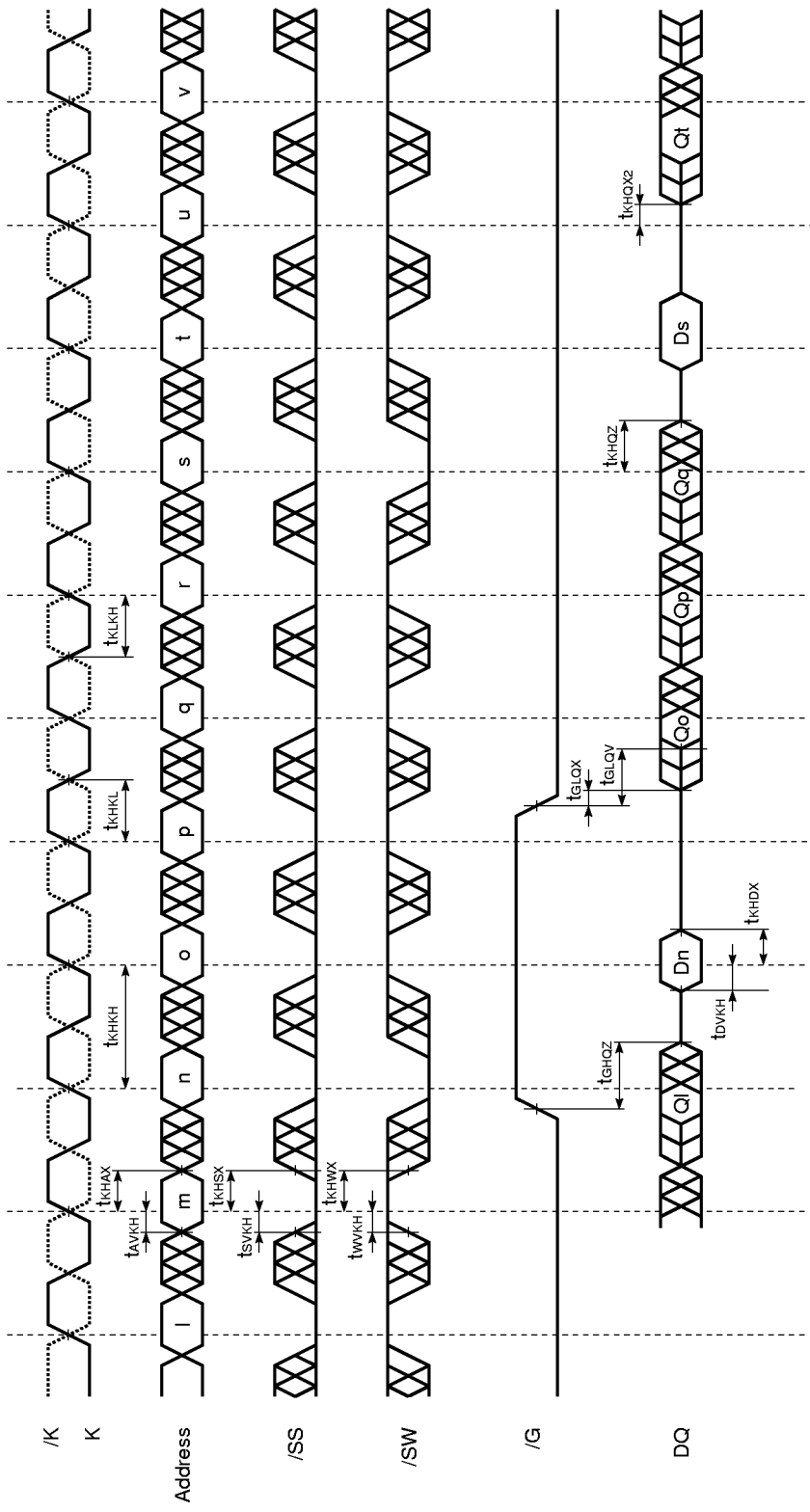
2. See figure.



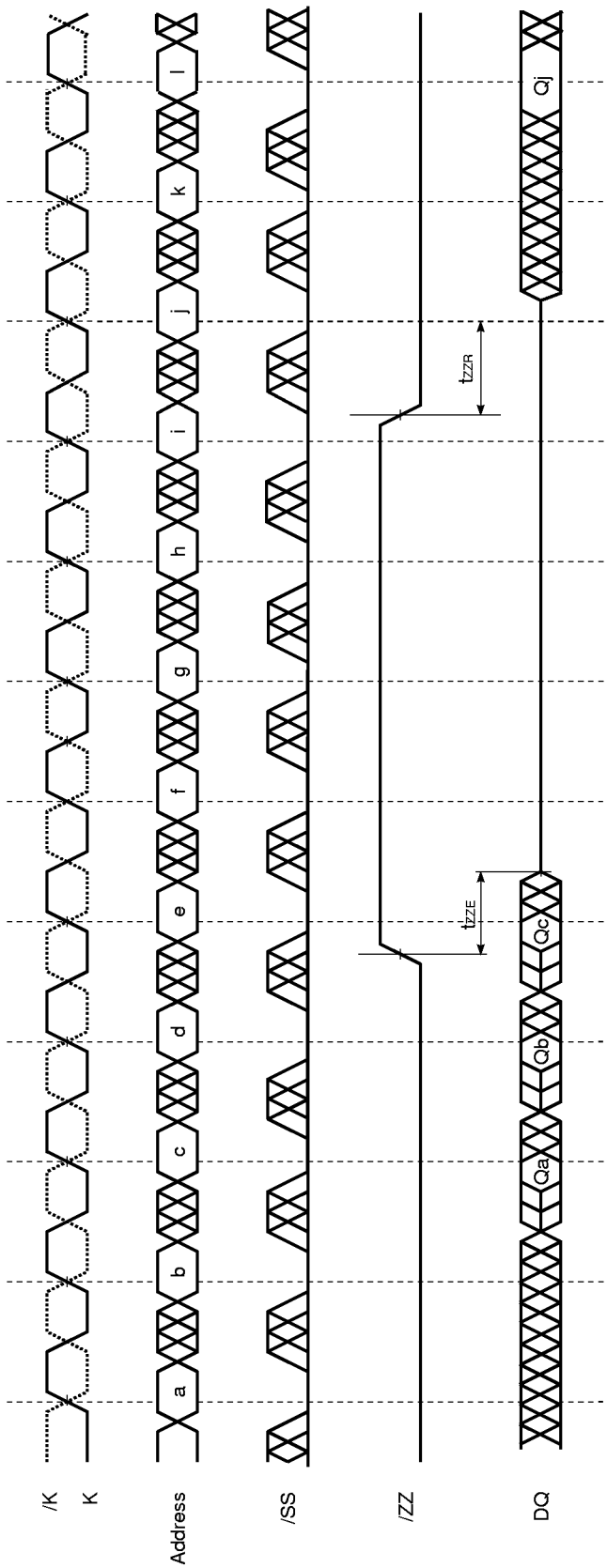
★ **Single Differential Clock, Registered Input / Registered Output Mode (Read Operation)**



★ **Single Differential Clock, Registered Input / Registered Output Mode (Write Operation)**



Sleep Mode



JTAG Specification

The μPD464618AL and μPD464636AL support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	4 U	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	2 U	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	3 U	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is deter-mined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	5 U	Test Data Output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

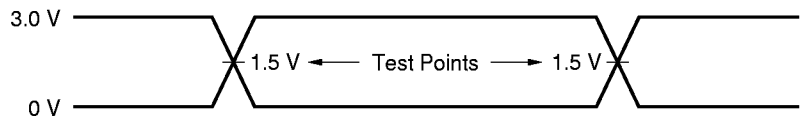
Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (T_j = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
JTAG input high voltage	V_{IH}		2.2		V_{DD}+0.3	V	
JTAG input low voltage	V_{IL}		–0.3		+0.8	V	
JTAG output high voltage	V_{OH}	I_{OH} = –8 mA	2.4		–	V	
JTAG output low voltage	V_{OL}	I_{OL} = 8 mA	–		0.4	V	

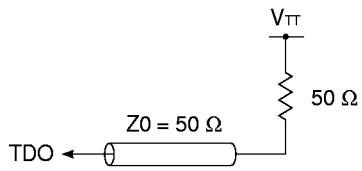
JTAG AC Test Conditions (T_j = 5 to 110 °C)

Input waveform (rise / fall time = 1 ns (20 to 80 %))



Output waveform

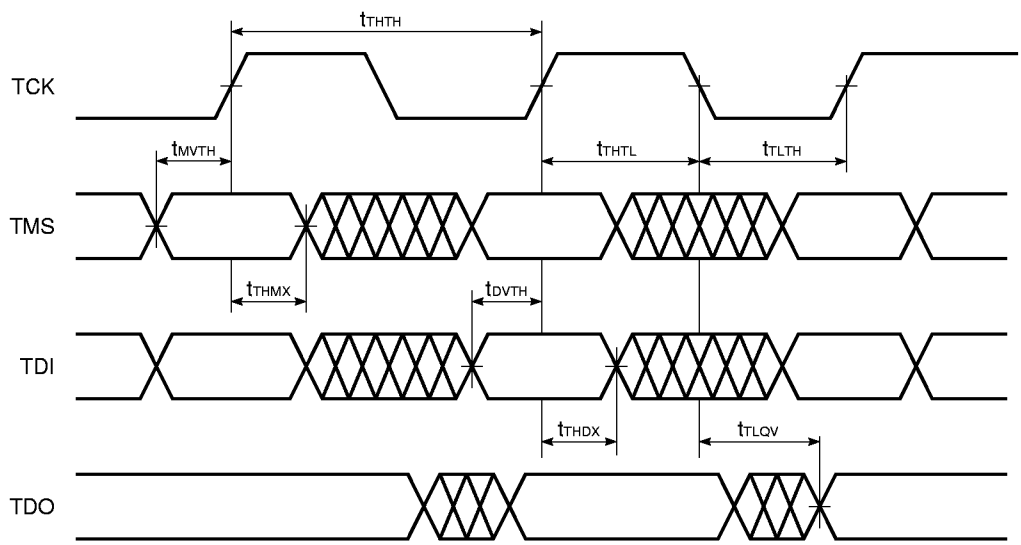
Output load (V_{TT}=1.5 V)



JTAG AC Characteristics (Tj = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock cycle time (TCK)	t_{THTH}		100		–	ns	
Clock phase time (TCK)	t_{THTL} / t_{TLTH}		40		–	ns	
Setup time (TMS / TDI)	t_{MVTH} / t_{DVTH}		10		–	ns	
Hold time (TMS / TDI)	t_{THMX} / t_{THDX}		10		–	ns	
TCK low to TDO valid (TDO)	t_{TLQV}		–		20	ns	

JTAG Timing Diagram



Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Scan Register Definition (2)

Register name	μPD464618AL	μPD464636AL	Unit
Instruction register	3	3	bit
Bypass register	1	1	bit
ID register	32	32	bit
Boundary register	51	70	bit

ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD464618AL	256K x 18	XXXX	0110001011 101000	00010010000	1
μPD464636AL	128K x 36	XXXX	0110101100 101000	00010010000	1

SCAN Exit Order

[μPD464618AL (256K words by 18 bits)]

Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID
1	M2	5R	26	SA17	3B
2	SA5	6T	27	NC	2B
3	SA0	4P	28	SA9	3A
			29	SA10	3C
4	SA4	6R	30	SA13	2C
5	SA8	5T	31	SA12	2A
6	ZZ	7T			
			32	DQb1	1D
7	DQa1	7P	33	DQb2	2E
8	DQa2	6N			
			34	DQb3	2G
9	DQa3	6L			
			35	DQb4	1H
10	DQa4	7K	36	/SBb	3G
11	/SBa	5L	37	NC	4D
12	/K	4L	38	/SS	4E
13	K	4K	39	NC	4G
14	/G	4F	40	NC	4H
			41	/SW	4M
15	DQa5	6H			
16	DQa6	7G	42	DQb5	2K
			43	DQb6	1L
17	DQa7	6F			
18	DQa8	7E	44	DQb7	2M
			45	DQb8	1N
19	DQa9	6D			
20	SA2	6A	46	DQb9	2P
21	SA3	6C	47	SA11	3T
22	SA7	5C	48	SA14	2R
23	SA6	5A	49	SA1	4N
24	NC	6B	50	SA15	2T
25	SA16	5B	51	M1	3R

[μPD464636AL (128K words by 36 bits)]

Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID
1	M2	5R	36	SA16	3B
			37	NC	2B
2	SA0	4P	38	SA9	3A
3	SA8	4T	39	SA10	3C
4	SA4	6R	40	SA13	2C
5	SA7	5T	41	SA12	2A
6	ZZ	7T	42	DQc9	2D
7	DQa9	6P	43	DQc8	1D
8	DQa8	7P	44	DQc7	2E
9	DQa7	6N	45	DQc6	1E
10	DQa6	7N	46	DQc5	2F
11	DQa5	6M	47	DQc4	2G
12	DQa4	6L	48	DQc3	1G
13	DQa3	7L	49	DQc2	2H
14	DQa2	6K	50	DQc1	1H
15	DQa1	7K	51	/SBc	3G
16	/SBa	5L	52	NC	4D
17	/K	4L	53	/SS	4E
18	K	4K	54	NC	4G
19	/G	4F	55	NC	4H
20	/SBb	5G	56	/SW	4M
21	DQb1	7H	57	/SBd	3L
22	DQb2	6H	58	DQd1	1K
23	DQb3	7G	59	DQd2	2K
24	DQb4	6G	60	DQd3	1L
25	DQb5	6F	61	DQd4	2L
26	DQb6	7E	62	DQd5	2M
27	DQb7	6E	63	DQd6	1N
28	DQb8	7D	64	DQd7	2N
29	DQb9	6D	65	DQd8	1P
30	SA2	6A	66	DQd9	2P
31	SA3	6C	67	SA11	3T
32	SA6	5C	68	SA14	2R
33	SA5	5A	69	SA1	4N
34	NC	6B			
35	SA15	5B	70	M1	3R

JTAG Instructions

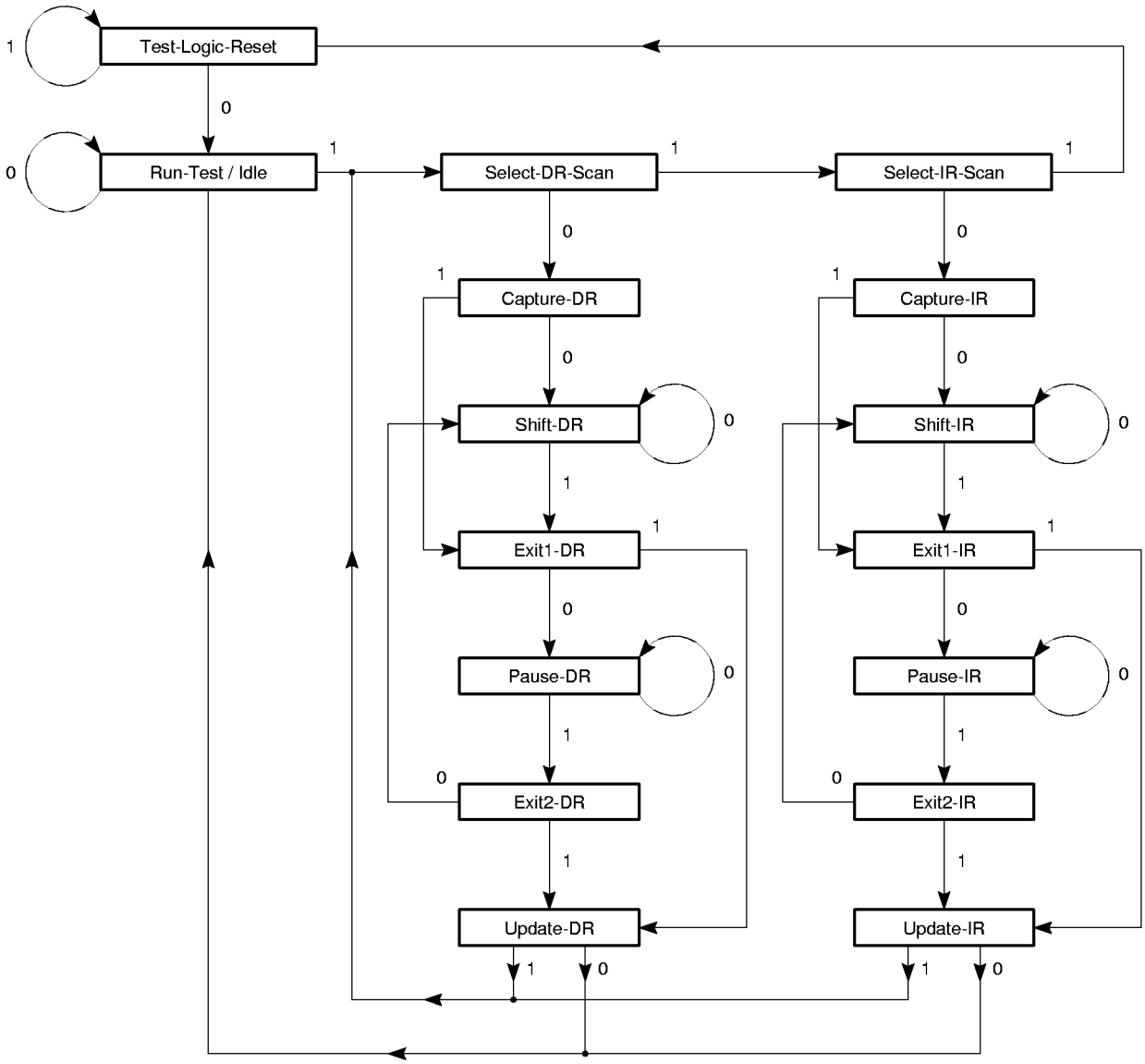
Instructions	Description
EXTEST	EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE instruction, except the RAM output are forced to Hi-Z any time the instruction is loaded.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE	SAMPLE is a Standard 1149.1 mandatory public instruction. When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins. This functionality is not Standard 1149.1 compliant.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (Hi-Z) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

JTAG Instruction Cording

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	1
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note 1. TRISTATE all data drivers and CAPTURE the pad values into a SERIAL SCAN LATCH.

TAP Controller State Diagram



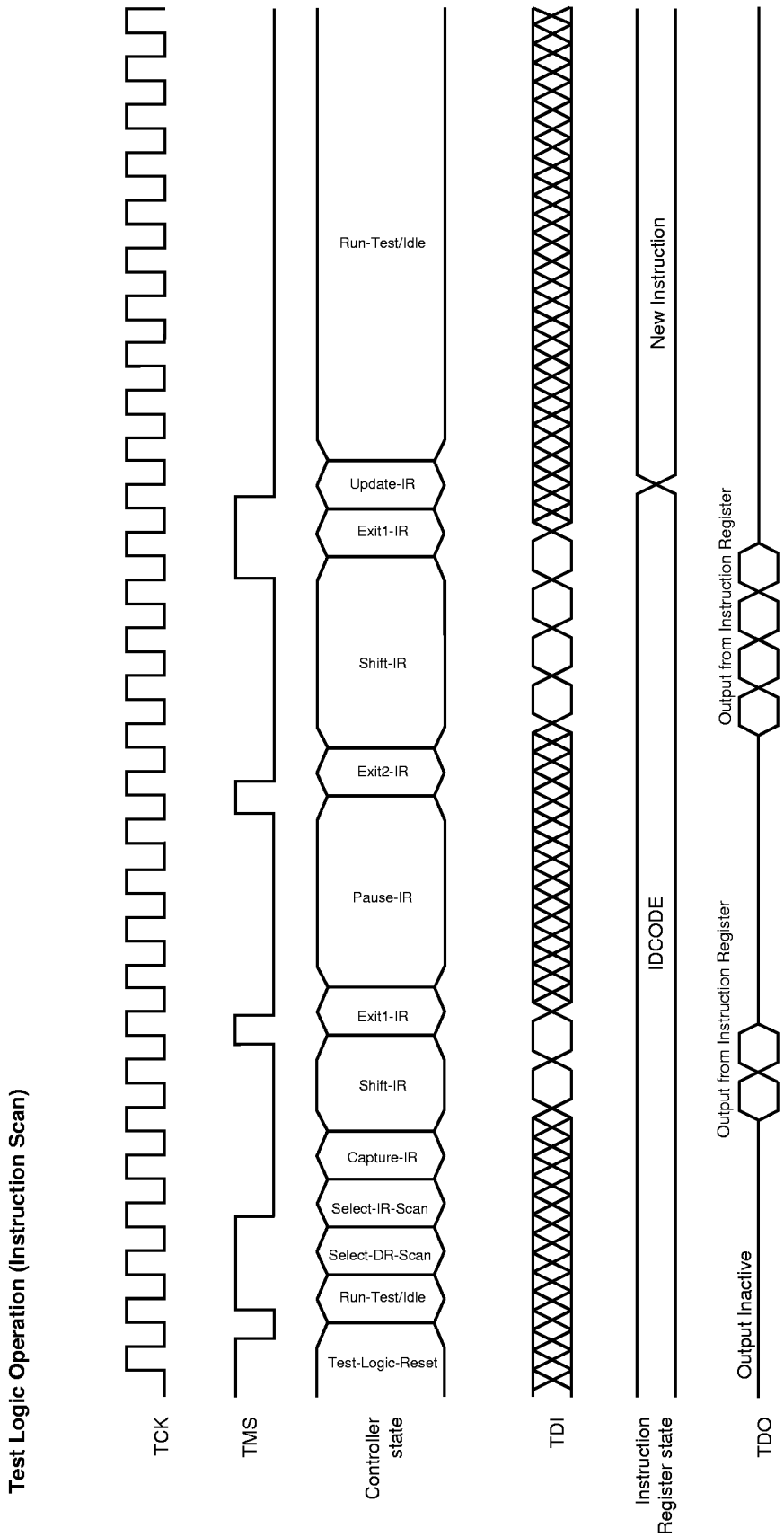
Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs.

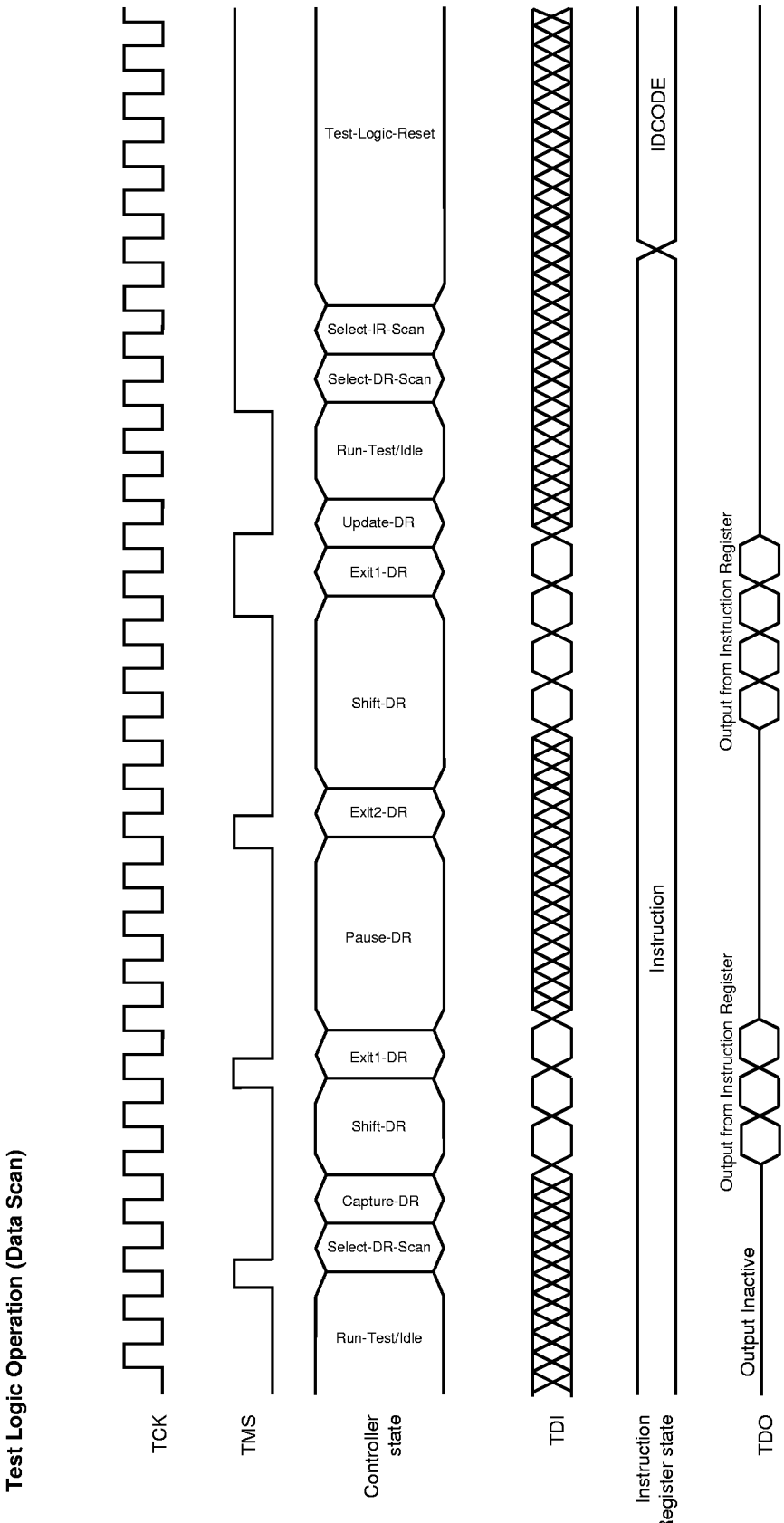
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1k resistor.

TDO should be left unconnected.

Test Logic Operation (Instruction Scan)

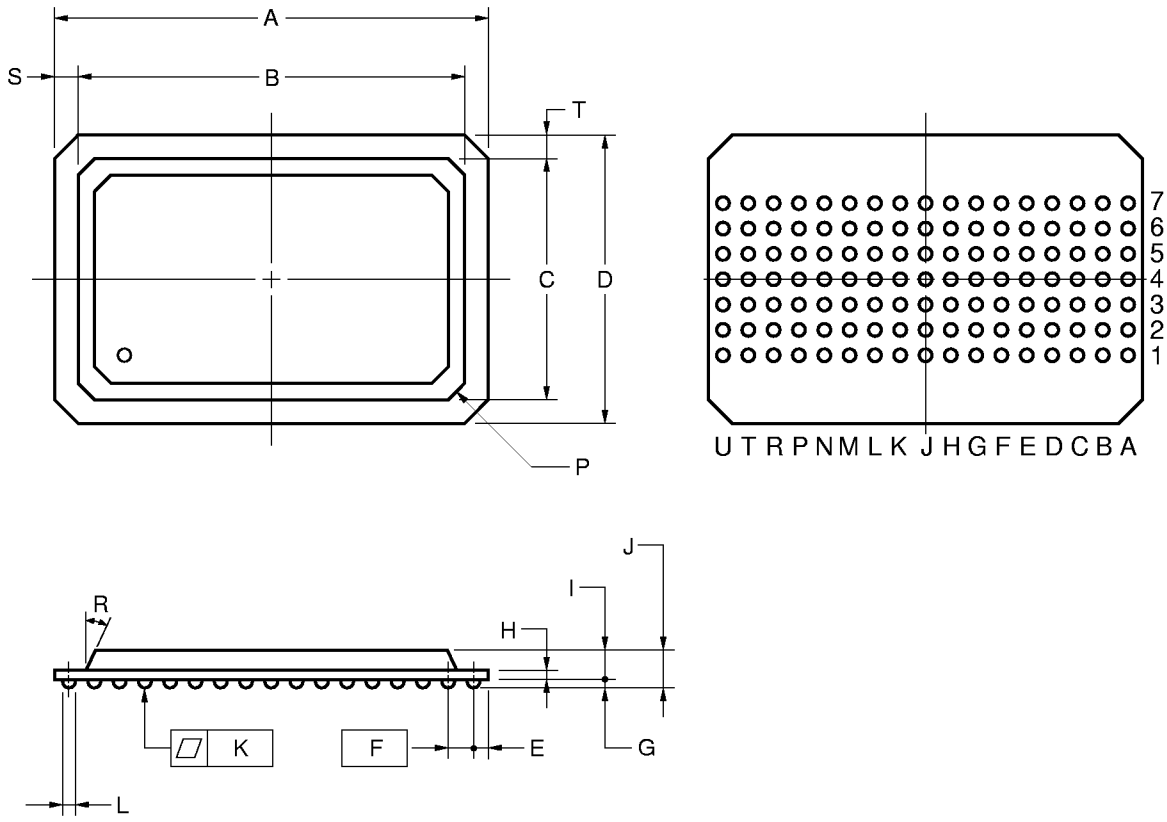


Test Logic Operation (Data Scan)



Package Drawing

119 PIN PLASTIC BGA



ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	19.5	0.768
C	12.0	0.472
D	14.0±0.2	0.551±0.008
E	0.84	0.033
F	1.27 (T.P.)	0.05 (T.P.)
G	0.6±0.1	$0.024^{+0.004}_{-0.005}$
H	0.56	0.022
I	1.46±0.1	$0.057^{+0.005}_{-0.004}$
J	2.30 MAX.	0.091
K	0.15	0.006
L	ϕ0.78±0.1	$\phi 0.031^{+0.004}_{-0.005}$
P	C0.7	C0.028
R	25°	25°
S	1.25	0.049
T	1.0	0.039

P119S1-R4

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD464618AL and μPD464636AL.

Type of Surface Mount Device

μPD464618ALS1: 119-pin plastic BGA
μPD464636ALS1: 119-pin plastic BGA