CMOS 16-Bit Microcontrollers

# TMP91CY22F

## 1. Outline and Features

TMP91CY22F is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91CY22F comes in a 100-pin flat package.

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4-channels (1.0 μs/2 bytes at 16 MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: 16 Kbytes
Built-in ROM: 256 Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus
  ··· Dynamic data bus sizing

(5) 8-bit timers: 8 channels

(6) 16-bit timer/event counter: 2 channels

(7) General-purpose serial interface: 2 channels
UART/ Synchronous mode: 2 channels
IrDA ver1.0 (115.2 kbps) supported

(8) Serial bus interface: 1 channel
- $I^2C$ bus mode/clock synchronous Select mode

(9) 10-bit AD converter: 8 channels

(10) Watchdog timer

(11) Timer for real-time clock (RTC)

(12) Chip Select/Wait controller: 4 channels

(13) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 26 internal interrupts: ┐
- 10 external interrupts: ┘ Seven selectable priority levels

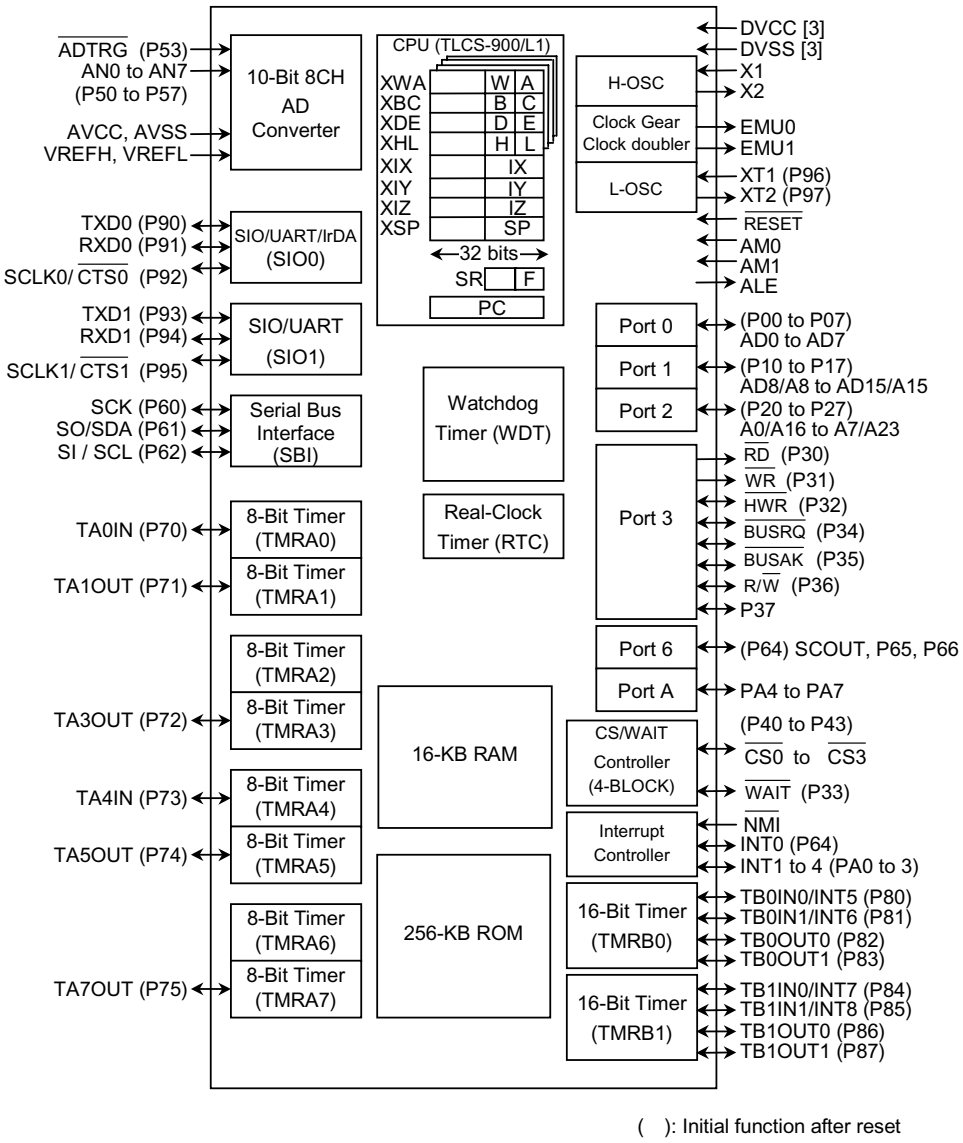
(14) Input/Output ports: 81 pins

(15) Standby function
Three HALT modes: IDLE2 (programmable), IDLE1, STOP

(16) Triple-clock controller
- Clock Doubler (DFM)
- Clock Gear (fc to fc/16)
- SLOW mode (fs = 32.768 kHz)

(17) Operating voltage
- $V_{CC}$ = 2.7 V to 3.6 V (fc max = 27 MHz)
- $V_{CC}$ = 1.8 V to 3.6 V (fc max = 10 MHz)

(18) Package
- 100-pin QFP: P-LQFP100-1414-0.50D




( ): Initial function after reset

Figure 1.1 TMP91CY22F Block Diagram

# 2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91CY22F, their names and functions are as follows:

## 2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91CY22F.

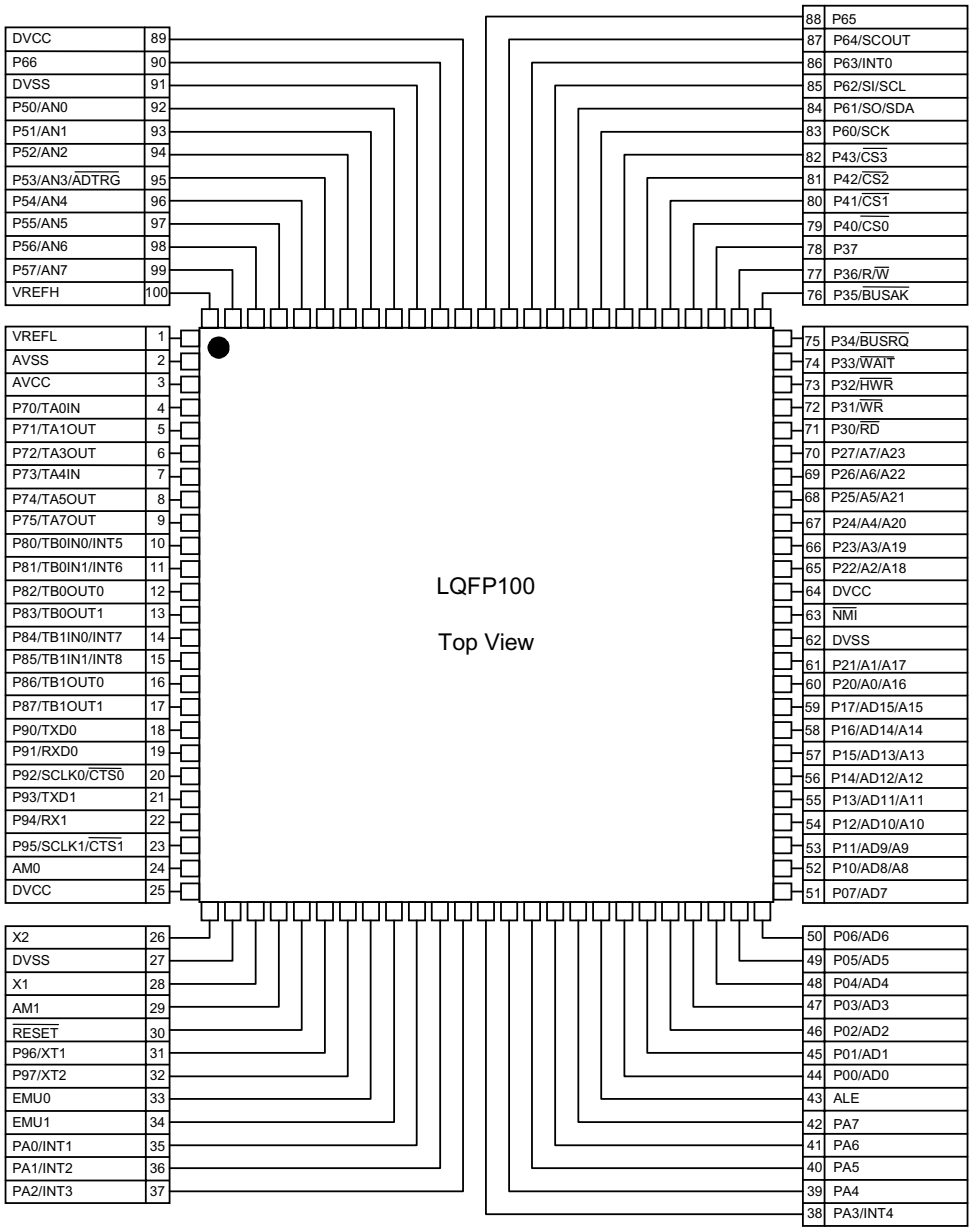



Figure 2.1.1 Pin assignment diagram (100-pin LQFP)

## 2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin names and functions.

Table 2.2.1 Pin names and functions (1/3)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P00 to P07 | 8 | I/O | Port 0: I/O port that allows I/O to be selected at the bit level |
| AD0 to AD7 | | Tri-state | Address and data (lower): Bits 0 to 7 of address and data bus |
| P10 to P17 | 8 | I/O | Port 1: I/O port that allows I/O to be selected at the bit level |
| AD8 to AD15 | | Tri-state | Address and data (upper): Bits 8 to 15 for address and data bus |
| A8 to A15 | | Output | Address: Bits 8 to 15 of address bus |
| P20 to P27 | 8 | I/O | Port 2: I/O port that allows I/O to be selected at the bit level (with pull-down resistor) |
| A0 to A7 | | Output | Address: Bits 0 to 7 of address bus |
| A16 to A23 | | Output | Address: Bits 16 to 23 of address bus |
| P30 | 1 | Output | Port 30: Output port |
| $\overline{RD}$ | | Output | Read: Strobe signal for reading external memory |
| P31 | 1 | Output | Port 31: Output port |
| $\overline{WR}$ | | Output | Write: Strobe signal for writing data to pins AD0 to AD7 |
| P32 | 1 | I/O | Port 32: I/O port (with pull-up resistor) |
| $\overline{HWR}$ | | Output | High Write: Strobe signal for writing data to pins AD8 to AD15 |
| P33 | 1 | I/O | Port 33: I/O port (with pull-up resistor) |
| $\overline{WAIT}$ | | Input | Wait: Pin used to request CPU bus wait |
| P34 | 1 | I/O | Port 34: I/O port (with pull-up resistor) |
| $\overline{BUSRQ}$ | | Input | Bus Request: Signal used to request Bus Release |
| P35 | 1 | I/O | Port 35: I/O port (with pull-up resistor) |
| $\overline{BUSAK}$ | | Output | Bus Acknowledge: Signal used to acknowledge Bus Release |
| P36 | 1 | I/O | Port 36: I/O port (with pull-up resistor) |
| R / $\overline{W}$ | | Output | Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle. |
| P37 | 1 | I/O | Port 37: I/O port (with pull-up resistor) |
| P40 | 1 | I/O | Port 40: I/O port (with pull-up resistor) |
| $\overline{CS0}$ | | Output | Chip Select 0: Outputs 0 when address is within specified address area |
| P41 | 1 | I/O | Port 41: I/O port (with pull-up resistor) |
| $\overline{CS1}$ | | Output | Chip Select 1: Outputs 0 if address is within specified address area |
| P42 | 1 | I/O | Port 42: I/O port (with pull-up resistor) |
| $\overline{CS2}$ | | Output | Chip Select 2: Outputs 0 if address is within specified address area |
| P43 | 1 | I/O | Port 43: I/O port (with pull-up resistor) |
| $\overline{CS3}$ | | Output | Chip Select 3: Outputs 0 if address is within specified address area |
| P50 to P57 | 8 | Input | Port 5: Pin used to input port |
| AN0 to AN7 | | Input | Analog input: Pin used to input to AD converter |
| $\overline{ADTRG}$ | | Input | AD Trigger: Signal used to request start of AD converter |
| P60 | 1 | I/O | Port 60: I/O port |
| SCK | | I/O | Serial bus interface clock in SIO Mode |
| P61 | 1 | I/O | Port 61: I/O port |
| SO | | Output | Serial bus interface output data in SIO Mode |
| SDA | | I/O | Serial bus interface data in $I^2C$ bus Mode |
| P62 | 1 | I/O | Port 62: I/O port |
| SI | | Input | Serial bus interface input data in SIO Mode |
| SCL | | I/O | Serial bus interface clock in $I^2C$ bus Mode |
| P63 | 1 | I/O | Port 63: I/O port |
| INT0 | | Input | Interrupt Request Pin 0: Interrupt request pin with programmable level / rising edge / falling edge |
| P64 | 1 | I/O | Port 64: I/O port |
| SCOUT | | Output | System Clock Output: Outputs $f_{FPH}$ or fs clock. |

Table 2.2.1 Pin names and functions (2/3)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P65 | 1 | I/O | Port 65: I/O port |
| P66 | 1 | I/O | Port 66: I/O port |
| P70<br>TA0IN | 1 | I/O<br>Input | Port 70: I/O port<br>Timer A0 Input |
| P71<br>TA1OUT | 1 | I/O<br>Output | Port 71: I/O port<br>Timer A1 Output |
| P72<br>TA3OUT | 1 | I/O<br>Output | Port 72: I/O port<br>Timer A3 Output |
| P73<br>TA4IN | 1 | I/O<br>Input | Port 73: I/O port<br>Timer A4 Input |
| P74<br>TA5OUT | 1 | I/O<br>Output | Port 74: I/O port<br>Timer A5 Output |
| P75<br>TA7OUT | 1 | I/O<br>Output | Port 75: I/O port<br>Timer A7 Output |
| P80<br>TB0IN0<br>INT5 | 1 | I/O<br>Input<br>Input | Port 80: I/O port<br>Timer B0 Input 0<br>Interrupt Request Pin 5: Interrupt request pin with programmable rising edge / falling edge. |
| P81<br>TB0IN1<br>INT6 | 1 | I/O<br>Input<br>Input | Port 81: I/O port<br>Timer B0 Input 1<br>Interrupt Request Pin 6: Interrupt request on rising edge |
| P82<br>TB0OUT0 | 1 | I/O<br>Output | Port 82: I/O port<br>Timer B0 Output 0 |
| P83<br>TB0OUT1 | 1 | I/O<br>Output | Port 83: I/O port<br>Timer B0 Output 1 |
| P84<br>TB1IN0<br>INT7 | 1 | I/O<br>Input<br>Input | Port 84: I/O port<br>Timer B1 Input 0<br>Interrupt Request Pin 7: Interrupt request pin with programmable rising edge / falling edge. |
| P85<br>TB1IN1<br>INT8 | 1 | I/O<br>Input<br>Input | Port 85: I/O port<br>Timer B1 Input 1<br>Interrupt Request Pin 8: Interrupt request on rising edge |
| P86<br>TB1OUT0 | 1 | I/O<br>Output | Port 86: I/O port<br>Timer B1 Output 0 |
| P87<br>TB1OUT1 | 1 | I/O<br>Output | Port 87: I/O port<br>Timer B1 Output 1 |
| P90<br>TXD0 | 1 | I/O<br>Output | Port 90: I/O port<br>Serial Send Data 0 (programmable open-drain) |
| P91<br>RXD0 | 1 | I/O<br>Input | Port 91: I/O port<br>Serial Receive Data 0 |
| P92<br>SCLK0<br>$\overline{\text{CTS0}}$ | 1 | I/O<br>I/O<br>Input | Port 92: I/O port<br>Serial Clock I/O 0<br>Serial Data Send Enable 0 (Clear to Send) |
| P93<br>TXD1 | 1 | I/O<br>Output | Port 93: I/O port<br>Serial Send Data 1 (programmable open-drain) |
| P94<br>RXD1 | 1 | I/O<br>Input | Port 94: I/O port (with pull-up resistor)<br>Serial Receive Data 1 |
| P95<br>SCLK1<br>$\overline{\text{CTS1}}$ | 1 | I/O<br>I/O<br>Input | Port 95: I/O port (with pull-up resistor)<br>Serial Clock I/O 1<br>Serial Data Send Enable 1 (Clear to Send) |
| P96<br>XT1 | 1 | I/O<br>Input | Port 96: I/O port (open-drain output)<br>Low-frequency oscillator connection pin |

Table 2.2.1 Pin names and functions (3/3)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P97<br>XT2 | 1 | I/O<br>Output | Port 97: I/O port (open-drain output)<br>Low-frequency oscillator connection pin |
| PA0 to PA3<br>INT1 to INT4 | 4 | I/O<br>Input | Ports A0 to A3: I/O ports<br>Interrupt Request Pins 1 to 4: Interrupt request pins with programmable rising edge / falling edge. |
| PA4 to PA7 | 4 | I/O | Ports A4 to A7: I/O ports |
| ALE | 1 | Output | Address Latch Enable<br>Can be disabled to reduce noise. |
| $\overline{\text{NMI}}$ | 1 | Input | Non-Maskable Interrupt Request Pin: Interrupt request pin with programmable falling edge or both edge. |
| AM0 to 1 | 2 | Input | Address Mode: The Vcc pin should be connected. |
| EMU0/EMU1 | 1 | Output | Test Pins: Open pins |
| $\overline{\text{RESET}}$ | 1 | Input | Reset: initializes TMP91CY22. (with pull-up resistor) |
| VREFH | 1 | Input | Pin for reference voltage input to AD converter (H) |
| VREFL | 1 | Input | Pin for reference voltage input to AD converter (L) |
| AVCC | 1 | I/O | High-frequency oscillator connection pins |
| AVSS | 1 | | Power supply pin for AD converter |
| X1/X2 | 2 | | GND pin for AD converter (0 V) |
| DVCC | 3 | | Power supply pins (All VCC pins should be connected with the power supply pin.) |
| DVSS | 3 | | GND pins (0 V) (All VSS pins should be connected with the power supply pin.) |

Note: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signal.

# 3. Operation

This device is a version of expanding its internal mask ROM size to 256 Kbytes and RAM size to 16 Kbytes. The configuration and the functionality of this device are the same as those of the TMP91CW12A. For the functions of this device that are not described here, refer to the TMP91CW12A data sheet.

## 3.1 Memory Map

Figure 3.1.1 is a memory map of the TMP91CY22F.

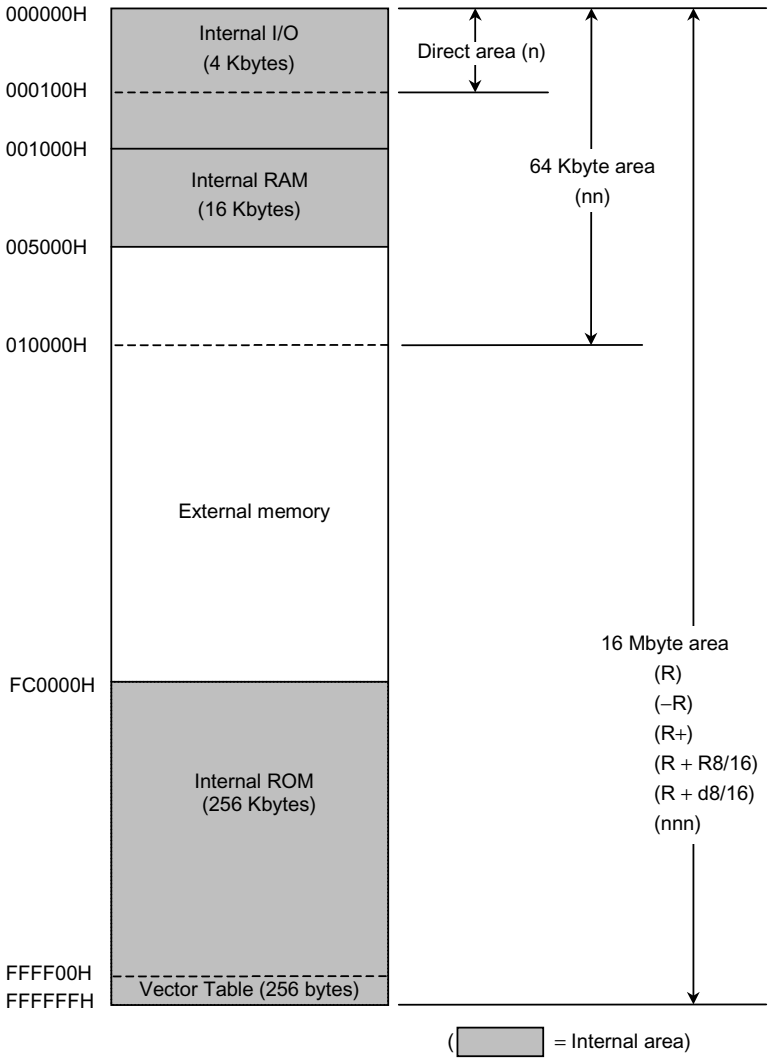



Figure 3.1.1 Memory Map

# 4. Electrical Characteristics

## 4.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power Supply Voltage | Vcc | −0.5 to 4.0 | V |
| Input Voltage | VIN | −0.5 to Vcc + 0.5 | V |
| Output Current | IOL | 2 | mA |
| Output Current | IOH | −2 | mA |
| Output Current (total) | ΣIOL | 80 | mA |
| Output Current (total) | ΣIOH | −80 | mA |
| Power Dissipation (Ta = 85°C) | PD | 600 | mW |
| Soldering Temperature (10 s) | TSOLDER | 260 | °C |
| Storage Temperature | TSTG | −65 to 150 | °C |
| Operating Temperature | TOPR | −40 to 85 | °C |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (1/2)

| Parameter | | Symbol | Condition | | Min | Typ. (Note) | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Power Supply Voltage (AVcc = DVcc) (AVss = DVss = 0 V) | | VCC | fc = 4 to 27 MHz | fs = 30 to 34 kHz | 2.7 | | 3.6 | V |
| | | | fc = 2 to 10 MHz | | 1.8 | | | |
| Input Low Voltage | P00 to P17 (AD0 to 15) | $V_{IL}$ | Vcc ≥ 2.7 V | | –0.3 | | 0.6 | V |
| | | | Vcc < 2.7 V | | | | 0.2Vcc | |
| | P20 to PA7 (except P63) | $V_{IL1}$ | Vcc ≥ 2.7 V | | | | 0.3Vcc | |
| | | | Vcc < 2.7 V | | | | 0.2Vcc | |
| | $\overline{RESET}$, $\overline{NMI}$, P63 (INT0) | $V_{IL2}$ | Vcc ≥ 2.7 V | | | | 0.25Vcc | |
| | | | Vcc < 2.7 V | | | | 0.15Vcc | |
| | AM0, 1 | $V_{IL3}$ | Vcc ≥ 2.7 V | | | | 0.3 | |
| | | | Vcc < 2.7 V | | | | 0.3 | |
| | X1 | $V_{IL4}$ | Vcc ≥ 2.7 V | | | | 0.2Vcc | |
| | | | Vcc < 2.7 V | | | | 0.1Vcc | |
| Input High Voltage | P00 to P17 (AD0 to 15) | $V_{IH}$ | Vcc ≥ 2.7 V | | 2.0 | | Vcc + 0.3 | |
| | | | Vcc < 2.7 V | | 0.7Vcc | | | |
| | P20 to PA7 (except P63) | $V_{IH1}$ | Vcc ≥ 2.7 V | | 0.7Vcc | | | |
| | | | Vcc < 2.7 V | | 0.8Vcc | | | |
| | $\overline{RESET}$, $\overline{NMI}$, P63 (INT0) | $V_{IH2}$ | Vcc ≥ 2.7 V | | 0.75Vcc | | | |
| | | | Vcc < 2.7 V | | 0.85Vcc | | | |
| | AM0, 1 | $V_{IH3}$ | Vcc ≥ 2.7 V | | Vcc – 0.3 | | | |
| | | | Vcc < 2.7 V | | Vcc – 0.3 | | | |
| | X1 | $V_{IH4}$ | Vcc ≥ 2.7 V | | 0.8Vcc | | | |
| | | | Vcc < 2.7 V | | 0.9Vcc | | | |
| Output Low Voltage | | $V_{OL}$ | IOL = 1.6 mA | Vcc ≥ 2.7 V | | | 0.45 | V |
| | | | IOL = 0.4 mA | Vcc < 2.7 V | | | 0.15Vcc | |
| Output High Voltage | | $V_{OH}$ | IOH = –400 μA | Vcc ≥ 2.7 V | 2.4 | | | |
| | | | IOH = –200μA | Vcc < 2.7 V | 0.8Vcc | | | |

Note: Typical values are for when Ta = 25°C and Vcc = 3.0 V unless otherwise noted.

## 4.2 DC Characteristics (2/2)

| Parameter | Symbol | Condition | Min | Typ. (Note 1) | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage Current | ILI | $0.0 \leq V_{IN} \leq Vcc$ | | 0.02 | ±5 | μA |
| Output Leakage Current | ILO | $0.2 \leq V_{IN} \leq Vcc - 0.2$ | | 0.05 | ±10 | |
| Power Down Voltage (at STOP, RAM back-up) | VSTOP | V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc | 1.8 | | 3.6 | V |
| $\overline{RESET}$ Pull-up Resistor | RRST | Vcc = 3 V ± 10% | 100 | | 400 | KΩ |
| | | Vcc = 2 V ± 10% | 200 | | 1000 | |
| Pin Capacitance | CIO | fc = 1 MHz | | | 10 | PF |
| Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0 | VTH | Vcc ≥ 2.7 V | 0.4 | 1.0 | | V |
| | | Vcc < 2.7 V | 0.3 | 0.8 | | |
| Programmable Pull-up Resistor | RKH | Vcc = 3 V ± 10% | 100 | | 400 | KΩ |
| | | Vcc = 2 V ± 10% | 200 | | 1000 | |
| NORMAL (Note 2) | Icc | Vcc = 3 V ± 10% fc = 27 MHz | | 10.0 | 13.0 | mA |
| IDLE2 | | | | 2.5 | 3.5 | |
| IDLE1 | | | | 1.0 | 1.8 | |
| NORMAL (Note 2) | | Vcc = 2 V ± 10 % fc = 10 MHz (Typ.: Vcc = 2.0 V) | | 1.7 | 2.5 | mA |
| IDLE2 | | | | 0.6 | 0.9 | |
| IDLE1 | | | | 0.25 | 0.4 | |
| SLOW (Note 2) | | Vcc = 3 V ± 10 % fs = 32.768 kHz | | 11.6 | 30 | μA |
| IDLE2 | | | | 5.2 | 19 | |
| IDLE1 | | Ta ≤ 70℃ | | 3.0 | 8 | |
| | | Ta ≤ 85℃ | | | 15 | |
| SLOW (Note 2) | | Vcc = 2 V ± 10 % fs = 32.768 KHz (Typ.: Vcc = 2.0 V) | | 7.7 | 20 | μA |
| IDLE2 | | | | 3.5 | 13 | |
| IDLE1 | | | | 2.0 | 10 | |
| STOP | | Vcc = 1.8 to 3.3V | | 0.1 | 10 | μA |

Note 1: Typical values are for when Ta = 25°C and Vcc = 3.0 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL, SLOW):
All functions are operating; output pins are open and input pins are fixed.

## 4.3 AC Characteristics

(1) Vcc = 3.0 V ± 10%

| No. | Symbol | Parameter | Variable | | $f_{FPH}$ = 27 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | $t_{FPH}$ | $f_{FPH}$ Period ( = x) | 37.0 | 31250 | 37.0 | | ns |
| 2 | $t_{AL}$ | A0 to A15 Vaild → ALE Fall | 0.5x – 14 | | 4 | | ns |
| 3 | $t_{LA}$ | ALE Fall → A0 to A15 Hold | 0.5x – 16 | | 2 | | ns |
| 4 | $t_{LL}$ | ALE High Width | x – 20 | | 17 | | ns |
| 5 | $t_{LC}$ | ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall | 0.5x – 14 | | 4 | | ns |
| 6 | $t_{CLR}$ | $\overline{RD}$ Rise → ALE Rise | 0.5x – 10 | | 8 | | ns |
| 7 | $t_{CLW}$ | $\overline{WR}$ Rise → ALE Rise | x – 10 | | 27 | | ns |
| 8 | $t_{ACL}$ | A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall | x – 23 | | 14 | | ns |
| 9 | $t_{ACH}$ | A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall | 1.5x – 26 | | 29 | | ns |
| 10 | $t_{CAR}$ | $\overline{RD}$ Rise → A0 to A23 Hold | 0.5x – 13 | | 5 | | ns |
| 11 | $t_{CAW}$ | $\overline{WR}$ Rise → A0 to A23 Hold | x – 13 | | 24 | | ns |
| 12 | $t_{ADL}$ | A0 to A15 Valid → D0 to D15 Input | | 3.0x – 38 | | 73 | ns |
| 13 | $t_{ADH}$ | A0 to A23 Valid → D0 to D15 Input | | 3.5x – 41 | | 88 | ns |
| 14 | $t_{RD}$ | $\overline{RD}$ Fall → D0 to D15 Input | | 2.0x – 30 | | 44 | ns |
| 15 | $t_{RR}$ | $\overline{RD}$ Low Width | 2.0x – 15 | | 59 | | ns |
| 16 | $t_{HR}$ | $\overline{RD}$ Rise → D0 to A15 Hold | 0 | | 0 | | ns |
| 17 | $t_{RAE}$ | $\overline{RD}$ Rise → A0 to A15 Output | x – 15 | | 22 | | ns |
| 18 | $t_{WW}$ | $\overline{WR}$ Low Width | 1.5x – 15 | | 40 | | ns |
| 19 | $t_{DW}$ | D0 to D15 Valid → $\overline{WR}$ Rise | 1.5x – 35 | | 20 | | ns |
| 20 | $t_{WD}$ | $\overline{WR}$ Rise → D0 to D15 Hold | x – 25 | | 12 | | ns |
| 21 | $t_{AWH}$ | A0 to A23 Valid → $\overline{WAIT}$ Input (1 WAIT +n Mode) | | 3.5x – 60 | | 69 | ns |
| 22 | $t_{AWL}$ | A0 to A15 Valid → $\overline{WAIT}$ Input (1 WAIT +n Mode) | | 3.0x – 50 | | 61 | ns |
| 23 | $t_{CW}$ | $\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold (1 WAIT +n Mode) | 2.0x + 0 | | 74 | | ns |
| 24 | $t_{APH}$ | A0 to A23 Valid → Port Input | | 3.5x – 89 | | 40 | ns |
| 25 | $t_{APH2}$ | A0 to A23 Valid → Port Hold | 3.5x | | 129 | | ns |
| 26 | $t_{AP}$ | A0 to A23 Valid → Port Valid | | 3.5x + 80 | | 209 | ns |

AC Measuring Conditions

- Output Level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input Level: High = 0.9 Vcc, Low = 0.1 Vcc

Note: "x" used in an expression shows a frequency for the clock $f_{FPH}$ selected by SYSCR1<SYSCK>.
The value of "x" changes according to whether a clock gear or a low-speed oscillator is selected.
An example value is calculated for fc, with gear=1/fc (SYSCR1<SYSCK,GEAR2 to 0> = 0000) .

(2) Vcc = 2.0 V ± 10%

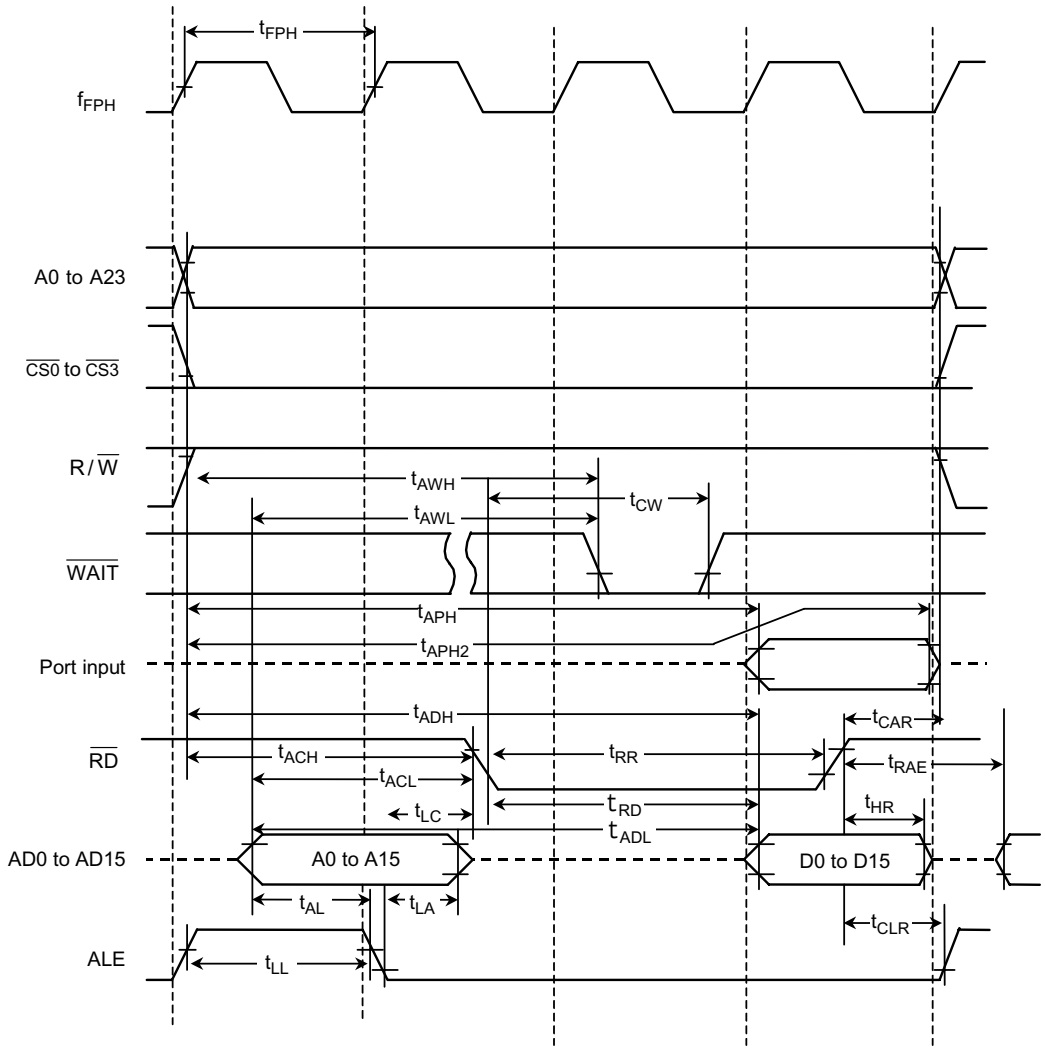
| No. | Symbol | Parameter | Variable | | $f_{FPH}$ =10M Hz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | $t_{FPH}$ | $f_{FPH}$ Period ( = x) | 100 | 31250 | 100 | | ns |
| 2 | $t_{AL}$ | A0 to A15 → ALE Fall | 0.5 x – 28 | | 22 | | ns |
| 3 | $t_{LA}$ | ALE Fall → A0 to A15 Hold | 0.5 x – 35 | | 15 | | ns |
| 4 | $t_{LL}$ | ALE High Width | x – 40 | | 60 | | ns |
| 5 | $t_{LC}$ | ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall | 0.5x – 28 | | 22 | | ns |
| 6 | $t_{CLR}$ | $\overline{RD}$ Rise → ALE Rise | 0.5x – 20 | | 30 | | ns |
| 7 | $t_{ACW}$ | $\overline{WR}$ Rise → ALE Rise | x – 20 | | 80 | | ns |
| 8 | $t_{ACL}$ | A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall | x – 75 | | 25 | | ns |
| 9 | $T_{ACH}$ | A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall | 1.5x –70 | | 80 | | ns |
| 10 | $t_{CAR}$ | $\overline{RD}$ Rise → A0 to A23 Hold | 0.5x – 30 | | 20 | | ns |
| 11 | $T_{CAW}$ | $\overline{WR}$ Rise → A0 to A23 Hold | x – 30 | | 70 | | ns |
| 12 | $t_{ADL}$ | A0 to A15 Valid → D0 to D15 Input | | 3.0x – 76 | | 224 | ns |
| 13 | $t_{ADH}$ | A0 to A23 Valid → D0 to D15 Input | | 3.5x – 82 | | 268 | ns |
| 14 | $T_{RD}$ | $\overline{RD}$ Fall → D0 to D15 Input | | 2.0x – 60 | | 140 | ns |
| 15 | $t_{RR}$ | $\overline{RD}$ Low Width | 2.0x – 30 | | 170 | | ns |
| 16 | $t_{HR}$ | $\overline{RD}$ Rise → D0 to D15 Hold | 0 | | 0 | | ns |
| 17 | $t_{RAE}$ | $\overline{RD}$ Rise → A0 to A15 Output | x – 30 | | 70 | | ns |
| 18 | $t_{WW}$ | $\overline{WR}$ Low Width | 1.5 x – 30 | | 120 | | ns |
| 19 | $t_{DW}$ | D0 to D15 Valid → $\overline{WR}$ Rise | 1.5 x – 70 | | 80 | | ns |
| 20 | $t_{WD}$ | $\overline{WR}$ Rise →D0 to D15 Hold | x – 50 | | 50 | | ns |
| 21 | $t_{AWH}$ | A0 to A23 Valid → $\overline{WAIT}$ Input $\left[\begin{smallmatrix}1WAIT\\+n\ mode\end{smallmatrix}\right]$ | | 3.5x – 120 | | 230 | ns |
| 22 | $t_{AWL}$ | A0 to A15 Valid → $\overline{WAIT}$ Input $\left[\begin{smallmatrix}1WAIT\\+n\ mode\end{smallmatrix}\right]$ | | 3.0x – 100 | | 200 | ns |
| 23 | $t_{CW}$ | $\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold $\left[\begin{smallmatrix}1WAIT\\+n\ mode\end{smallmatrix}\right]$ | 2.0x + 0 | | 200 | | ns |
| 24 | $t_{APH}$ | A0 to A23 Valid → Port Input | | 3.5x – 170 | | 180 | ns |
| 25 | $t_{APH2}$ | A0 to A23 Valid → Port Hold | 3.5x | | 350 | | ns |
| 26 | $t_{AP}$ | A0 to A23 Valid → Port Valid | | 3.5x + 170 | | 520 | ns |

AC Measuring Conditions

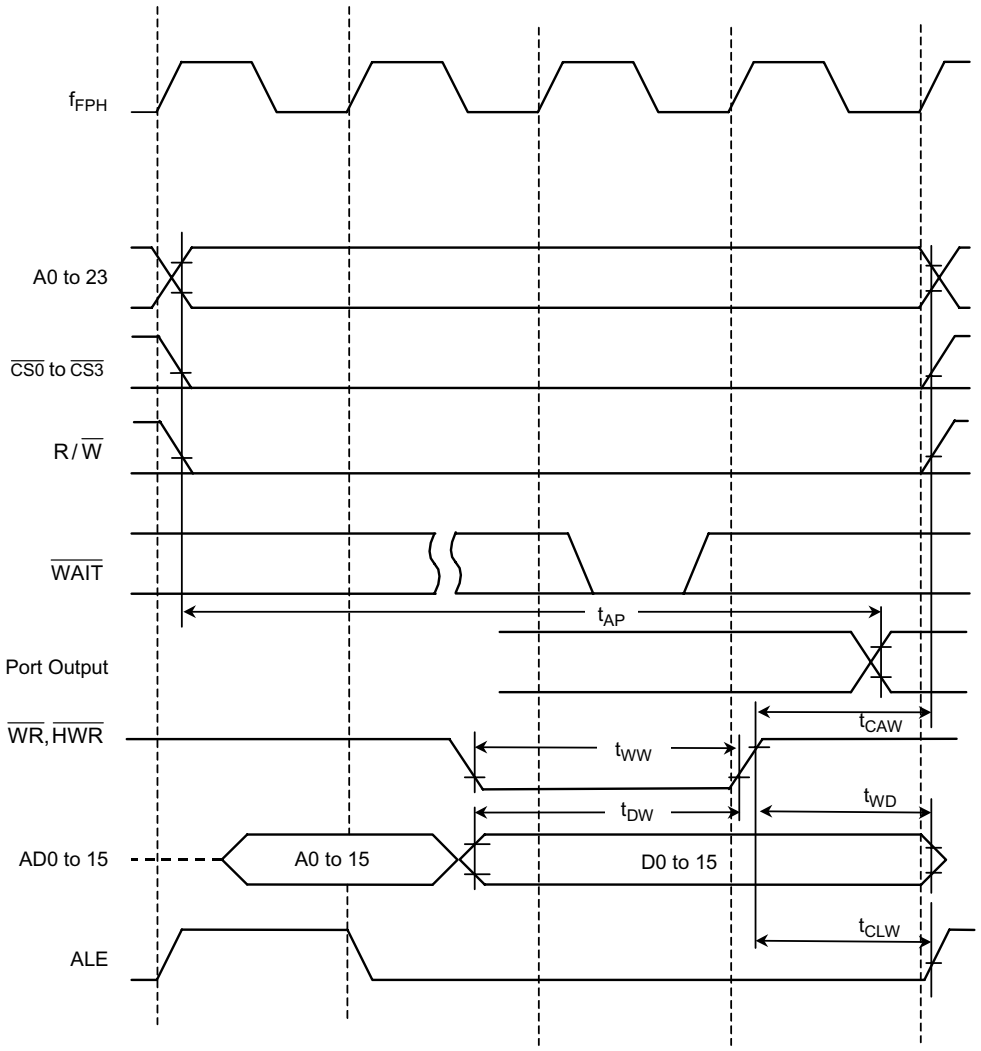
- Output Level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input Level: High = 0.9 Vcc, Low = 0.1 Vcc

Not: "x" used in an expression shows a frequency for the clock $f_{FPH}$ selected by SYSCR1<SYSCK>. The value of "x" changes according to whether a clock gear or a low-speed oscillator is selected. An example value is calculated for fc, with gear = 1/fc (SYSCR1<SYSCK,GEAR2 to 0> = 0000) .

(3) Read Cycle


tFPH
fFPH
A0 to A23
CS0 to CS3
R/W
tAWH
tAWL
tCW
WAIT
tAPH
tAPH2
Port input
tADH
tCAR
RD
tACH
tRR
tRAE
tACL
tLC
tRD
tHR
tADL
AD0 to AD15
A0 to A15
D0 to D15
tAL
tLA
tCLR
ALE
tLL

(4) Write Cycle



## 4.4 AD Conversion Characteristics

AVcc = Vcc, AVss = Vss

| Symbol | parameter | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| VREFH | Analog Reference Voltage (+) | Vcc = 3 V ± 10% | Vcc − 0.2 V | Vcc | Vcc | V |
| | | Vcc = 2 V ± 10% | Vcc | Vcc | Vcc | |
| VREFL | Analog Reference Voltage (−) | Vcc = 3 V ± 10% | Vss | Vss | Vss + 0.2 V | |
| | | Vcc = 2 V ± 10% | Vss | Vss | Vss | |
| VAIN | Analog Input Voltage Range | | $V_{REFL}$ | | $V_{REFH}$ | |
| IREF (VREFL = 0V) | Analog Current for Analog Reference Voltage <VREFON> = 1 | Vcc = 3 V ± 10% | | 0.94 | 1.20 | mA |
| | | Vcc = 2 V ± 10% | | 0.65 | 0.90 | |
| | <VREFON> = 0 | Vcc = 1.8 V to 3.3 V | | 0.02 | 5.0 | μA |
| − | Error (not including quantizing errors) | Vcc = 3 V ± 10% | | ± 1.0 | ± 4.0 | LSB |
| | | Vcc = 2 V ± 10% | | ± 1.0 | ± 4.0 | |

Note 1: 1 LSB = (VREFH − VREFL)/1024 [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value for $I_{CC}$ includes the current which flows through the AVCC pin.

## 4.5 Serial Channel Timing (I/O Internal Mode)

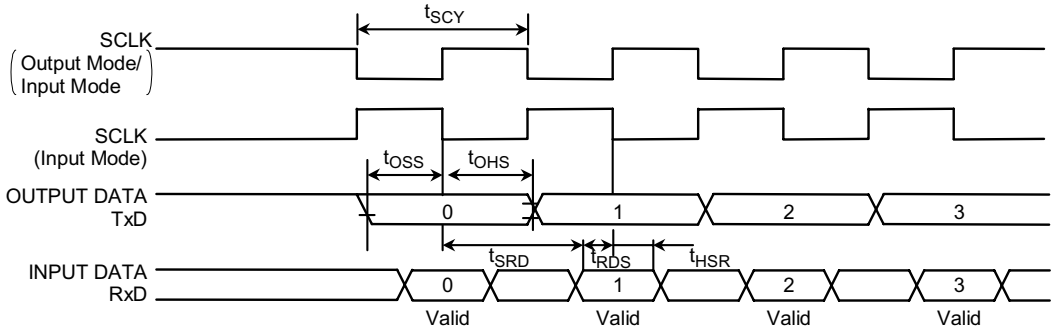
(1) SCLK Input Mode

| Symbol | Parameter | Variable | | 10 MHz | | 27 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{SCY}$ | SCLK Period | 16X | | 1.6 | | 0.59 | | μs |
| $t_{OSS}$ | Output Data → SCLK Rising /Falling Edge* | $t_{SCY}/2 - 4x-110$ (Vcc=3V±10%) | | 290 | | 38 | | ns |
| | | $t_{SCY}/2 - 4x-180$ (Vcc=2V±10%) | | 220 | | — | | |
| $t_{OHS}$ | SCLK Rising/Falling Edge* → Output Data Hold | $t_{SCY}/2 + 2X + 0$ | | 1000 | | 370 | | ns |
| $t_{HSR}$ | SCLK Rising/Falling Edge* → Input Data Hold | 3x+10 | | 310 | | 121 | | ns |
| $t_{SRD}$ | SCLK Rising/Falling Edge* → Valid Data Input | | $t_{SCY} - 0$ | | 1600 | | 592 | ns |
| $t_{RSD}$ | Valid Data Input →SCLK Rising/Falling Edge* | 0 | | 0 | | 0 | | ns |

*) SCLK Rinsing/Falling Edge: The rising edge is used in SCLK Rising Mode.
The falling edge is used in SCLK Falling Mode.

(2) SCLK Output Mode

| Symbol | Parameter | Variable | | 10 MHz | | 27 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{SCY}$ | SCLK Period (programable) | 16X | 8192X | 1.6 | 819 | 0.59 | 303 | μs |
| $t_{OSS}$ | Output Data →SCLK Rising Edge | $t_{SCY}/2 - 40$ | | 760 | | 256 | | ns |
| $t_{OHS}$ | SCLK Rising Edge → Output Data Hold | $t_{SCY}/2 - 40$ | | 760 | | 256 | | ns |
| $t_{HSR}$ | SCLK Rising Edge → Input Data Hold | 0 | | 0 | | 0 | | ns |
| $t_{SRD}$ | SCLK Rising Edge → Valid Data Input | | $t_{SCY} - 1X - 180$ | | 1320 | | 375 | ns |
| $t_{RDS}$ | SCLK Rising Edge → Valid Data Input | 1X + 180 | | 280 | | 217 | | ns |



## 4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

| Symbol | Parameter | Variable | | 10 MHz | | 27 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{VCK}$ | Clock period | 8X + 100 | | 900 | | 396 | | ns |
| $t_{VCKL}$ | Clock Low level width | 4X + 40 | | 440 | | 188 | | ns |
| $t_{VCKH}$ | Clock High level width | 4X + 40 | | 440 | | 188 | | ns |

## 4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 to INT4 Interrupts

| Symbol | Parameter | Variable | | 10 MHz | | 27 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{INTAL}$ | $\overline{NMI}$, INT0 to INT4 Low level width | 4X + 40 | | 440 | | 188 | | ns |
| $t_{INTAH}$ | $\overline{NMI}$, INT0 to INT4 High level width | 4X + 40 | | 440 | | 188 | | ns |

(2) INT5 to INT8 Interrupts, Capture

The INT5 to INT8 input width depends on the system clock and prescaler clock settings.

| System Clock Selected <SYSCK> | Prescaler Clock Selected <PRCK1, PRCK0> | $t_{INTBL}$ (INT5 to INT8 Low level Width) | | $t_{INTBH}$ (INT5 to INT8 High Level Width) | | Unit |
|---|---|---|---|---|---|---|
| | | Variable | $f_{FPH}$ = 27 MHz | Variable | $f_{FPH}$ = 27 MHz | |
| | | Min | Min | Min | Min | |
| 0 (fc) | 00 ($f_{FPH}$) | 8X + 100 | 396 | 8X + 100 | 396 | ns |
| | 10 (fc/16) | 128Xc + 0.1 | 4.8 | 128Xc + 0.1 | 4.8 | μs |
| 1 (fs) | 00 ($f_{FPH}$) | 8X + 0.1 | 244.3 | 8X + 0.1 | 244.3 | |

Note: Xc = Period of Clock fc

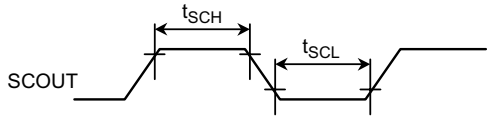
## 4.8 SCOUT Pin AC Characteristics

| Symbol | Parameter | Variable | | 10 MHz | | 27 MHz | | Condition | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{SCH}$ | Low level width | 0.5T – 13 | | 37 | | 5 | | Vcc ≥ 2.7 V | ns |
| | | 0.5T – 25 | | 25 | | - | | Vcc < 2.7 V | |
| $t_{SCL}$ | High level width | 0.5T – 13 | | 37 | | 5 | | Vcc ≥ 2.7 V | ns |
| | | 0.5T – 25 | | 25 | | - | | Vcc < 2.7 V | |

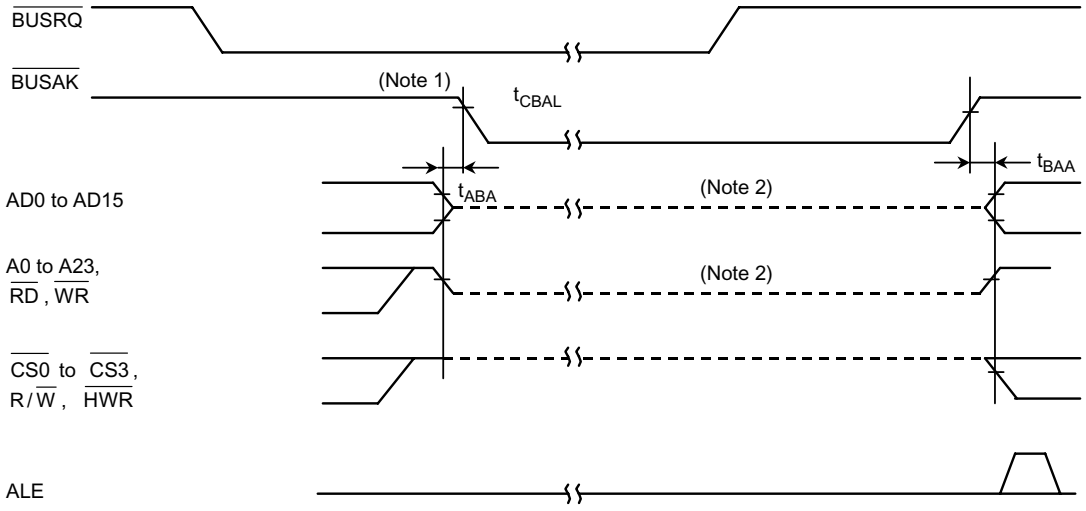
Note: T = Period of SCOUT

Measrement Condition

- Output Level: High 0.7 Vcc/Low 0.3 Vcc, CL = 10pF



## 4.9 Bus Request/Bus Acknowledge




| Symbol | Paramter | Variable | | $f_{FPH}$ = 10 MHz | | $f_{FPH}$ = 27 MHz | | Condition | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{ABA}$ | Output Buffer Off to $\overline{BUSAK}$ Low | 0 | 80 | 0 | 80 | 0 | 80 | Vcc ≥ 2.7 V | ns |
| | | 0 | 300 | 0 | 300 | 0 | 300 | Vcc < 2.7 V | |
| $t_{BAA}$ | $\overline{BUSAK}$ High to Output Buffer On | 0 | 80 | 0 | 80 | 0 | 80 | Vcc ≥ 2.7 V | ns |
| | | 0 | 300 | 0 | 300 | 0 | 300 | Vcc < 2.7 V | |

Note 1: Even if the $\overline{BUSRQ}$ Signal goes Low, the bus will not be released while the $\overline{WAIT}$ signal is Low. The bus will only be released when $\overline{BUSRQ}$ goes Low while $\overline{WAIT}$ is High.

Note 2: This line shows only that the output buffer is in the Off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resister during bus release, careful design is necessary, since fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

## 4.10 Recommended Oscillation Circuit

The TMP91CY22F has been evaluated by the following resonator manufacturer. The evaluation results are shown below for your information.

Note: The load capacitance of the oscillation terminal is the sum of the load capacitances of C1 and C2 to be connected and the stray capacitance on the board. Even if the ratings of C1 and C2 are used, the load capacitance varies with each board and the oscillator may malfunction. Therefore, when designing a board, make the pattern around the oscillation circuit shortest. It is recommended that final evaluation of the resonator be performed on the board.

(1) Examples of resonator connection

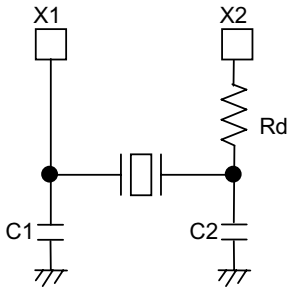



Figure 4.10.1 High-frequency Oscillator Connection

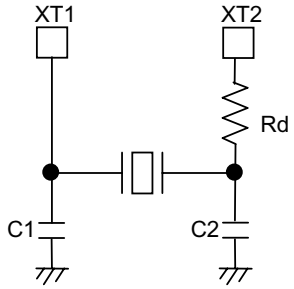



Figure 4.10.2 Low-frequency Oscillator Connection

(2) Recommended ceramic resonators for the TMP91CY22F: Murata Manufacturing Co., Ltd.

Ta = −40 to 85°C

| Item | Oscillation frequency [MHz] | Recommened resonator | Recommended rating | | | VCC[V] | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1[pF] | C2[pF] | Rd[kΩ] | | |
| High-frequency oscillator | 2.0 | CSTLS2M00G56-B0 | (47) | (47) | 0 | 1.8 to 2.2 | — |
| | | CSTCC2.00MG0H6 | (47) | (47) | | | |
| | 2.5 | CSTLS2M50G56-B0 | (47) | (47) | | | |
| | | CSTCC2.50MG0H6 | (47) | (47) | | | |
| | 4.0 | CSTS0400MG06 | (47) | (47) | | 2.7 to 3.3 | |
| | | CSTCR4M00G55-R0 | (39) | (39) | | | |
| | 6.75 | CSTS0675MG06 | (47) | (47) | | | |
| | | CSTCR6M75G55-R0 | (39) | (39) | | | |
| | 10.0 | CSTS1000MG03 | (15) | (15) | | 1.8 to 2.2 | |
| | | CSTCC10.0MG | (15) | (15) | | | |
| | 12.5 | CST12.5MTW | (30) | (30) | | 2.7 to 3.3 | |
| | | CSTCV12.5MTJ0C4 | (22) | (22) | | | |
| | 20.0 | CSTLS20M0X51-B0 | (5) | (5) | | | |
| | | CSTCW2000MX01 | (6) | (6) | | | |
| | 27.0 | CSALS27M0X51-B0 | 3 | 3 | | | |
| | | CSACW2700MX01 | 3 | 3 | | | |

- The values enclosed in brackets in the C1 and C2 columns apply to the condenser built-in type.
- The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

  http://www.murata.co.jp/search/index.html