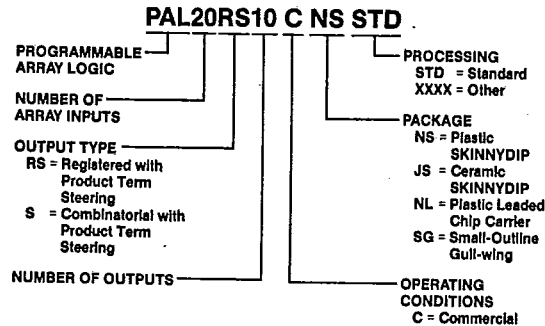


PAL20RS10 Series**20S10, 20RS10
20RS8, 20RS4****Features/Benefits**

- Product term steering allows up to 16 product terms per output
- Programmable polarity
- Register preload
- Power-up reset
- Security fuse

Ordering Information**PAL20RS10 Series**

	ARRAY INPUTS	OUTPUTS		t _{PD} * (ns)	I _{CC} (mA)
		COMBINATORIAL	REGISTERED		
PAL20S10	20	10	0	35/40	240
PAL20RS10	20	0	10	35	240
PAL20RS8	20	2	8	35/40	240
PAL20RS4	20	6	4	35/40	240

*35 ns active low, 40 ns active high

Description

The PAL20RS10 Series offers product term steering, which allows up to sixteen product terms to be used at a single output.

The PAL device transfer function is the familiar Boolean sum of products. The PAL device consists of a programmable AND array driving a fixed OR array. Product terms with all bits programmed (disconnected) assume the logical high state, and product terms with both true and complement of any signal connected assume the logical low state.

Variable Input/Output Pin Ratio

The registered devices have ten dedicated input lines, and each combinatorial output is an I/O pin. The combinatorial device has twelve dedicated input lines, and only eight of the ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied directly to VCC or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with programmable three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any combination of device inputs or output feedback. The output provides a bidirectional I/O pin in the combinatorial configuration, and may be configured as a dedicated input if the buffer is always disabled.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops which are loaded on the low-to-high transition of the clock input.

Package Drawings

(refer to PAL Device Package Outlines, page 3-179)

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Programmable Polarity

Each flip-flop has individually programmable polarity. The unprogrammed state is active low.

Product Term Steering

Product term steering allows each pair of outputs to share its product terms with one output or the other (not both). Each pair has a total of sixteen product terms; thus, one output can use zero to sixteen terms while the other has sixteen to zero. Product terms can only be shared mutually exclusively. If both outputs need the same term, it must be created twice, once for each output.

Preload and Power-Up Reset

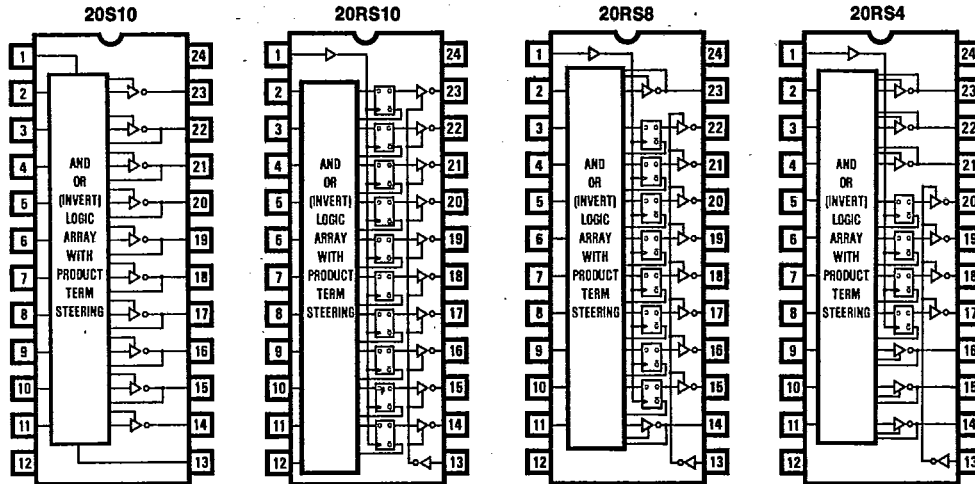
The 20RS10 Series offers register preload for device testability. The registers can be preloaded from the outputs by using super-voltages in order to simplify functional testing. The 20RS10 Series also offers Power-Up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

Packages

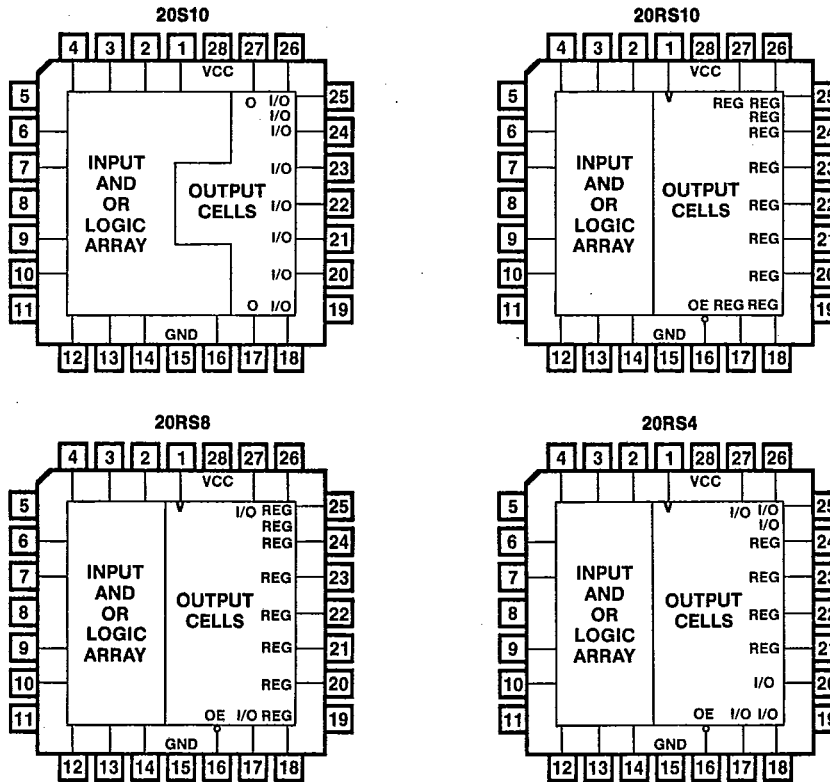
The commercial PAL20RS10 Series is available in the plastic SKINNYDIP (NS), ceramic SKINNYDIP (JS), plastic leaded chip carrier (NL), and small outline (SG) packages.

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DIP/SO Pinouts



PLCC Pinouts



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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7.0 V	-0.5 V to 12.0 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature		-65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			UNIT
		MIN	TYP	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
t_w	Width of clock	Low		15	ns
		High		10	
t_{su}	Set up time from input or feedback to clock	20RS10, 20RS8, 20RS4			ns
t_h	Hold time	0			ns
T_A	Operating free-air temperature	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}^1	Low-level input voltage					0.8	V
V_{IH}^1	High-level input voltage			2			V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$	-0.8	-1.5		V
I_{IL}^2	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$	-0.02	-0.25		mA
I_{IH}^2	High-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4 \text{ V}$		25		μA
I_I	Maximum input current	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$		100		μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 24 \text{ mA}$	0.3	0.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -3.2 \text{ mA}$	2.4	2.8		V
I_{OZL}^2	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$		-100		μA
I_{OZH}^2			$V_O = 2.4 \text{ V}$		100		μA
I_{OS}^3	Output short-circuit current	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$	-30	-70	-130	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$			175	240	mA

- These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

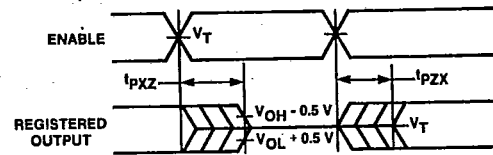
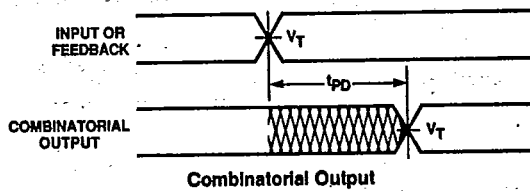
SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output 20S10, 20RS8, 20RS4	Polarity fuse intact	$R_1 = 200 \Omega$ $R_2 = 390 K\Omega$	25	35	ns	
		Polarity fuse programmed		30	40		
t_{CLK}	Clock to output or feedback			12	17	ns	
t_{CF}	Clock to feedback			10	15	ns	
t_{PZX}	Pin 13 to output enable except 20S10			10	20	ns	
t_{PXZ}	Pin 13 to output disable except 20S10			11	20	ns	
t_{EA}	Input to output enable	20S10, 20RS8, 20RS4		25	35	ns	
t_{ER}	Input to output disable	20S10, 20RS8, 20RS4		13	25	ns	
f_{MAX}	Maximum frequency	External		19	27	MHz	
		Internal		20	28		
		No feedback		33	50		

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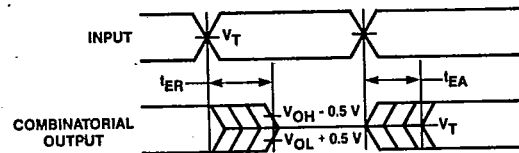
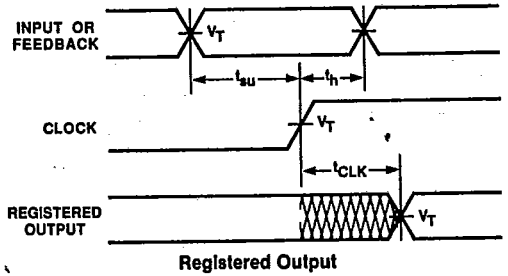
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Switching Waveforms

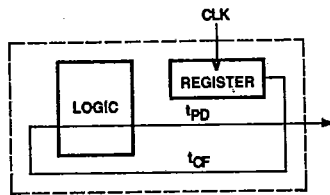
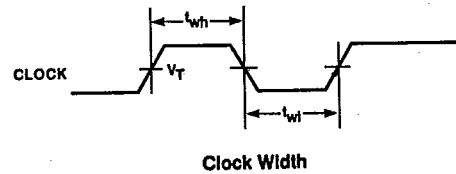
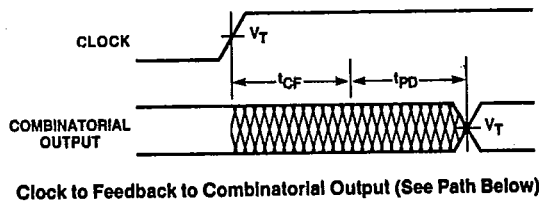
T-46-13-47



Pin 13 to Output Disable/Enable



Input to Output Disable/Enable



- Notes:
 1. $V_T = 1.5\text{ V}$
 2. Input pulse amplitude 0 V to 3.0 V
 3. Input rise and fall times 2-5 ns typical

Key to Timing Diagrams

WAVEFORM	INPUTS	OUTPUTS
	DONT CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Switching Test Load

(refer to page 5-164)

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)

Register Preload Waveform

(refer to page 5-164)

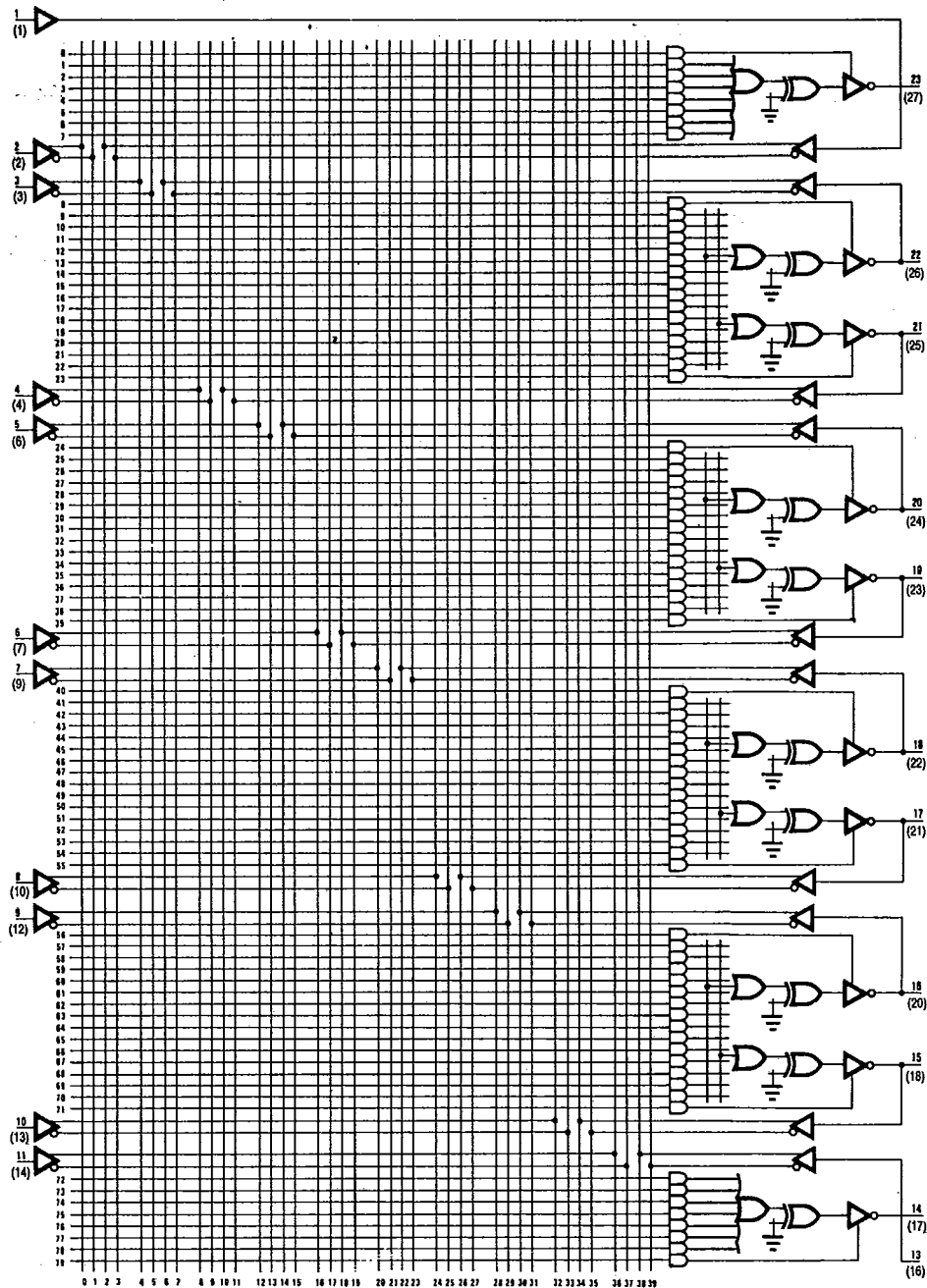
Power-Up Reset Waveform

(refer to page 5-164)

Schematic of Inputs and Outputs

(refer to page 5-164)

20S10



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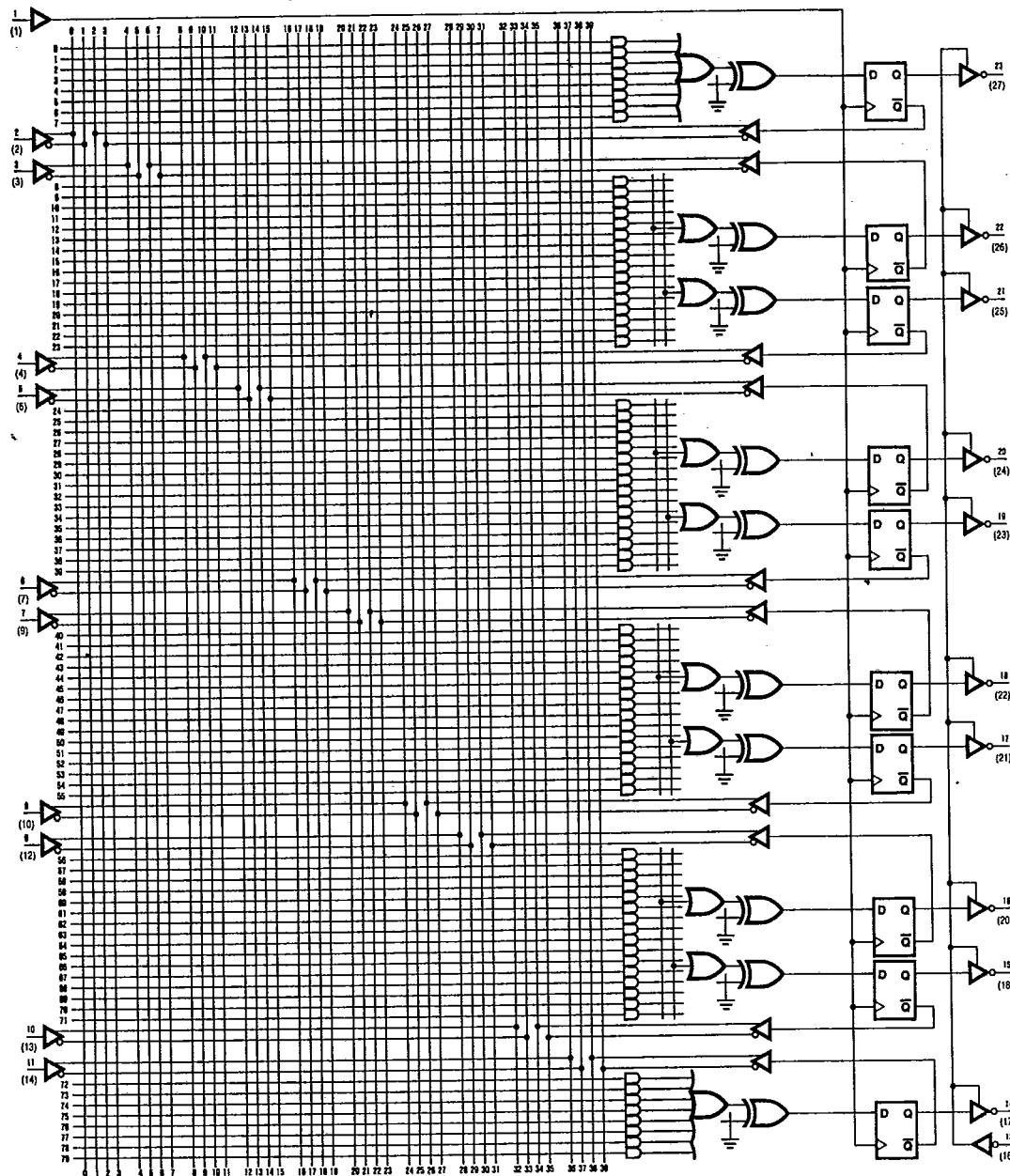
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20RS10

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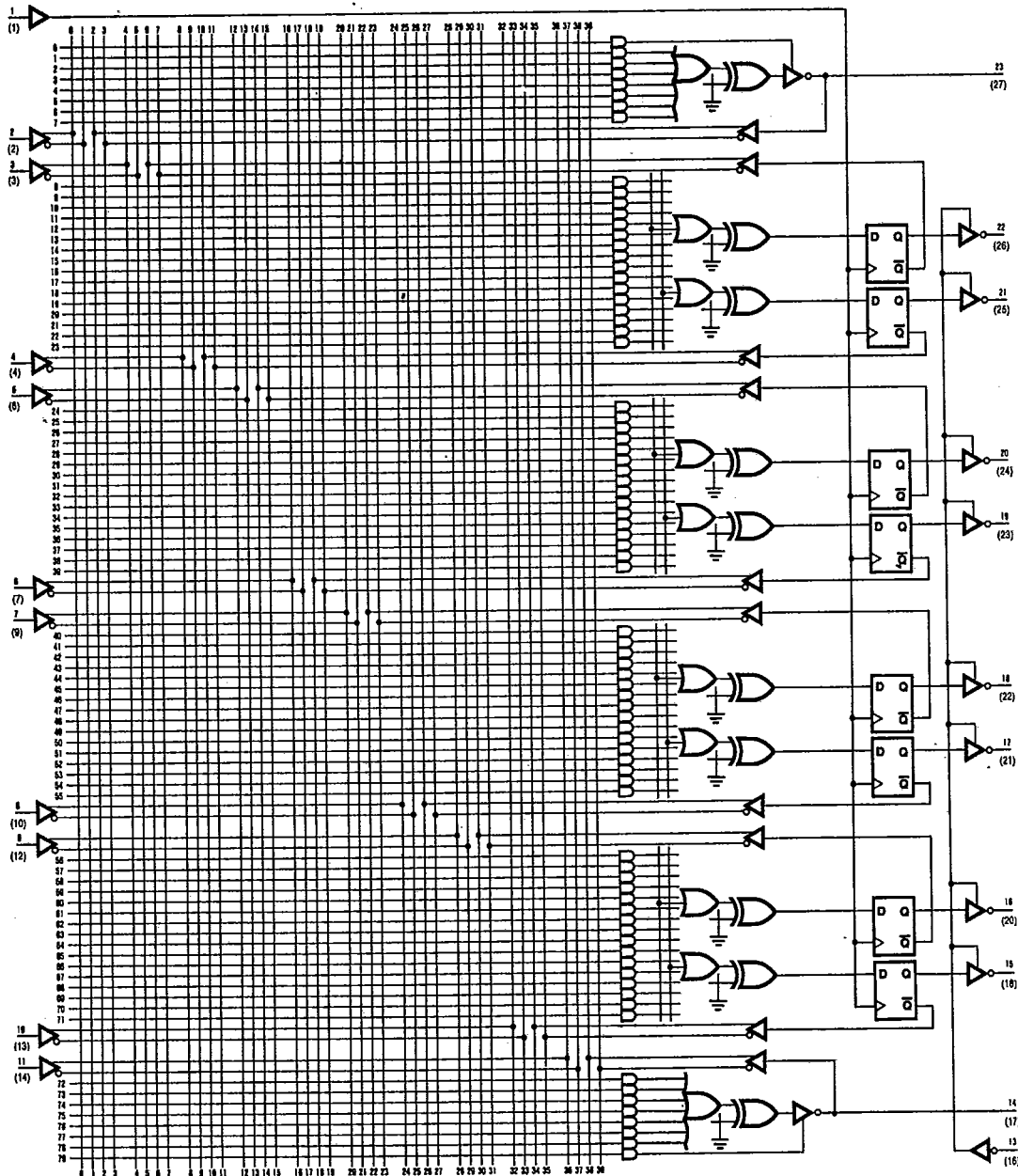
PAL20RS10 Series
20S10, 20RS10, 20RS8, 20RS4

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96D 27169 D

20RS8

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PAL20RS10 Series
20S10, 20RS10, 20RS8, 20RS4

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0257526 ADV MICRO PLA/PLE/ARRAYS

96D 27170 D

20RS4