National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC432A-X REV 0A0

Original Creation Date: 01/06/99
Last Update Date: 04/05/99
Last Major Revision Date: 04/01/99

DUAL WIDEBAND MONOLITHIC OP AMP

General Description

The CLC432 is a current-feedback amplifier that provides a wide bandwidth and high slew rate for applications where board density and power are key considerations. This amplifier provides a dc-coupled small signal bandwidth exceeding 92MHz while consuming only 7mA per channel. Operating from ±15V supplies, the CLC432's enhanced slew rate circuitry delivers large-signal bandwidths with output voltage swings up to 28Vpp. A wide range of bandwidth-insensitive gains are made possible by virtue of the CLC432's current-feedback topology.

The large common-mode input range and fast settling time (70ns to 0.05%) makes this amplifier well suited for CCD & data telecommunication applications. Many high performance video applications requiring signal gain and/or switching will be satisfied with the CLC432 due to it's very low differential gain and phase errors (less than 0.1% and 0.1 degrees; Av = +2V/V at 4.43MHz into 150Ohms load).

Quick 8ns rise and fall times on 10V pulses allow the CLC432 to drive either twisted pair or coaxial transmission lines over long distances.

The CLC432's combination of low input voltage noise, wide common-mode input voltage range and large output voltage swings makes it especially well suited for wide dynamic range signal processing applications.

Industry Part Number

CLC432A

NS Part Numbers

CLC432AJ-QML

Prime Die

LB1792A

Controlling Document

5962-9472502MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide bandwidth: 92Mhz (Av = +1)
  62MHz (Av = +2)
- Fast slew rate: 2000V/us
- Fast disable: 1us to high-Z output
- High channel isolation: 70dB at 10MHz
- Single or dual supplies: ±5V to ±16.5V

Applications

- Video signal multiplexing
- Twisted-pair differential driver
- CCD buffer & level shifting
- Discrete gain-select amplifier
- Transimpedance amplifier

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vs)		±16.5 V dc
Output Current (Iout)		100mA
Common Mode Input Voltage (Vcm)		±Vs
Differential Input Voltage(Vid)		±10 V
Maximum Power Dissipation (Pd) (Note 2)		1.02W
Lead Temperature (Soldering, 10 seconds)		+300 C
Junction Temperature (Tj)		+175 C
Storage Temperature Range		-65 C to +150 C
Thermal Resistance		
Junction -to-ambient	(ThetaJA)	
Ceramic DIP	(Still Air)	128 C/W
	(500 LFPM)	67 C/W
Junction -to-case	(ThetaJC)	
Ceramic DIP		23 C/W
Package Weight (Typical)		
Ceramic DIP		TBD
ESD Tolerance (Note 3)		
ESD Ratings		2000 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum package power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable package power dissipation at any temperature is Pdmax = (Tjmax -TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±15V dc
Gain Range (Av)	±1 V/V to ±10 V/V
Ambient Operating Temperature Range (TA)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Static and DC Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V dc, Av = +2, and load resistance (Rl) = 100Ohms. Gain Resistance (Rg) and Feedback resistance (Rf) equals 750Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input Bias Current, noninverting				-8	+8	uA	1, 2
					-18	+18	uA	3
Ibi	Input Bias Current, inverting				-6	6	uA	1, 2
					-9	9	uA	3
Vio	Input Offset Voltage				-6	6	mV	1, 3
					-9	9	mV	2
Dibn	Average Input Bias Current Drift, noninverting	Ta = +125 C, -55 C	1		-150	150	nA/C	2, 3
Dibi	Average Input Bias Current Drift, inverting	Ta = +125 C, -55 C	1		-40	40	nA/C	2, 3
Dvio	Average Input Offset Voltage Drift	Ta = +125 C, -55 C	1		-50	50	uV/C	2, 3
Icc	Supply Current	No Load				15.8	mA	1, 2
						19.6	mA	3
PSRR	Power Supply Rejection Ratio	+Vs = +4.0V to +5.0V, -Vs = -4.0V to -5.0V			59		dB	4, 6
					57		dB	5
CMRR	Common Mode Rejection Ratio	Vcm = ±1V	1		58		dB	4
			1		56		dB	5, 6

Electrical Characteristics

AC PARAMETERS: Frequency Domain Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15V dc, Av = +2, and load resistance (Rl) = 100Ohms. Gain Resistance (Rg) and Feedback resistance (Rf) equals 750Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwidth	-3 dB bandwidth, Vout < 4.0 Vpp			42		MHz	4
			2		34		MHz	5
			2		42		MHz	6
LSBW	Large Signal Bandwidth	-3 dB bandwidth, Vout < 10 Vpp	1		21		MHz	4, 6
			1		17		MHz	5
GFPH	Gain Flatness Peaking High	0.1 MHz to 100 MHz, Vout ≤ 4.0 Vpp				0.5	dB	4
			2			0.9	dB	5, 6
GFR	Gain Flatness Rolloff	0.1 MHz to 20 MHz, Vout ≤ 4.0 Vpp				0.8	dB	4
			2			0.8	dB	5, 6
DG	Differential Gain	4.43 MHz	1		0.18		%	4, 6
			1		0.22		%	5
DP	Differential Phase	4.43 MHz	1		0.18		Deg.	4, 6
			1		0.32		Deg.	5
LPD	Linear Phase Deviation	DC to 20MHz, Vout ≤ 4.0 Vpp	1		1.8		Deg.	4, 6
			1		2.3		Deg.	5

Electrical Characteristics

AC PARAMETERS: Distortion and Noise Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15V dc, Av = +2, and load resistance (Rl) = 100Ohms. Gain Resistance (Rg) and Feedback resistance (Rf) equals 750Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	2 Vpp at 10 MHz				38	dBc	4
			2			33	dBc	5
			2			38	dBc	6
HD3	3rd Harmonic Distortion	2 Vpp at 10 MHz				48	dBc	4
			2			48	dBc	5, 6
VN	Input Noise Voltage	> 1 MHz	1			4.2	nV/Sq RtHz	4, 6
			1			4.7	nV/Sq RtHz	5
-ICN	Inverting Input Noise Current	> 1 MHz	1			16	pA/Sq RtHz	4, 5
			1			18	pA/Sq RtHz	6
+ICN	Noninverting Input Noise Current	> 1 MHz	1			2.5	pA/Sq RtHz	4
			1			2.8	pA/Sq RtHz	5, 6

AC PARAMETERS: Timing Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15V dc, Av = +2, and load resistance (Rl) = 100Ohms. Gain Resistance (Rg) and Feedback resistance (Rf) equals 750Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SR	Slew Rate	Vout = ±10 V Step	1		1500		V/uS	9
			1		1400		V/uS	10, 11
Tr, Tf	Rise and Fall Time	10 V Step	1			12	nS	9, 11
			1			14	nS	10
Ts	Settling Time	2V step at 0.05% of the fixed value	1			100	nS	9, 11
			1			120	nS	10
OS	Overshoot	2 V Step, 1 ns rise/fall	1			10	%	9, 11
			1			14	%	10

Electrical Characteristics

DC PARAMETERS: Perfomance Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V dc, Av = +2, and load resistance (Rl) = 100Ohms. Gain Resistance (Rg) and Feedback resistance (Rf) equals 750Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
R+in	Positive Input Resistance		1		16		MOhms	4, 5
			1		5		MOhms	6
C+in	Positive Input Capacitance		1		1		pF	4, 5, 6
Vout	Output Voltage Range	No Load	1		-13.6	+13.6	V	1, 2
			1		-13.2	+13.2	V	3
Voutl	Output Voltage Range	Rl = 100Ohms	1		-3.7	+3.7	V	1, 2
			1		-2.7	+2.7	V	3
CMIR	Common Mode Input Voltage Range		1		12		V	1, 2
			1		11.5		V	3
Iout	Output Current		1		38		mA	1, 2
			1		28		mA	3

AC PARAMETERS: Switching Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15V dc, Av = +2, and load resistance (Rl) = 100Ohms. Gain Resistance (Rg) and Feedback resistance (Rf) equals 750Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

Ton	Switching turn on time	Vin = 4 Vpp at 10 MHz	1			150	uS	9, 10
			1			170	uS	11
Toff	Switching turn off time	Vin = 4 Vpp at 10 MHz	1			1000	uS	9, 11
			1			1400	uS	10
Vih	Disable Logic High Input Voltage	Single ended mode	1			2	V	1, 2, 3
Vil	Disable Logic Low Input Voltage	Single ended mode	1		0.8		V	1, 2, 3
Idin	Disable Logic Maximum Input Current	DIS = Vil to Vih	1			180	uA	1, 2
			1			210	uA	3
Vmin	Minimum Differential Voltage	DIS = Vil to Vih	1			0.4	V	1, 2
			1			0.5	V	3

Electrical Characteristics

AC PARAMETERS: Isolation Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15V dc, Av = +2, and load resistance (Rl) = 100Ohms. Gain Resistance (Rg) and Feedback resistance (Rf) equals 750Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
XTLK	Crosstalk, input referred isolation	10 MHz	1		64		dB	4, 5, 6
ISO	Off Isolation	10 MHz	1		53		dB	4, 5, 6

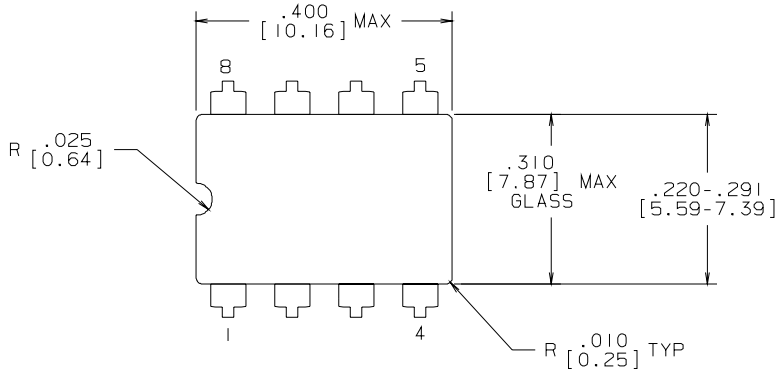
Note 1: If not tested, shall be guaranteed to the limits specified in table I
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

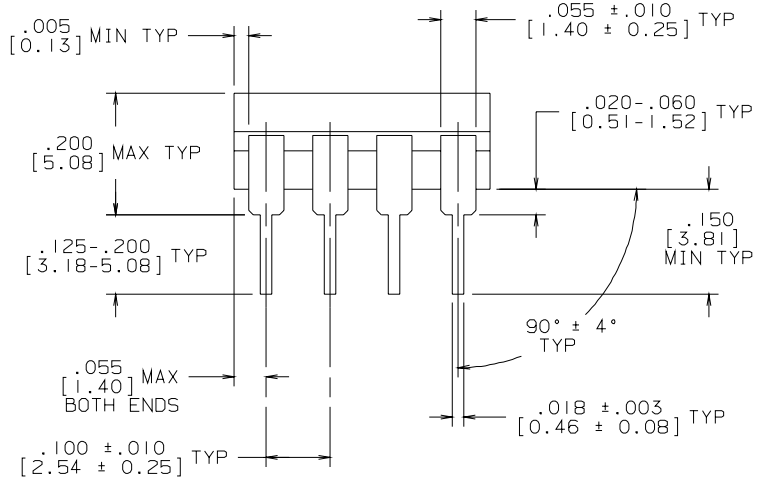
Graphics and Diagrams

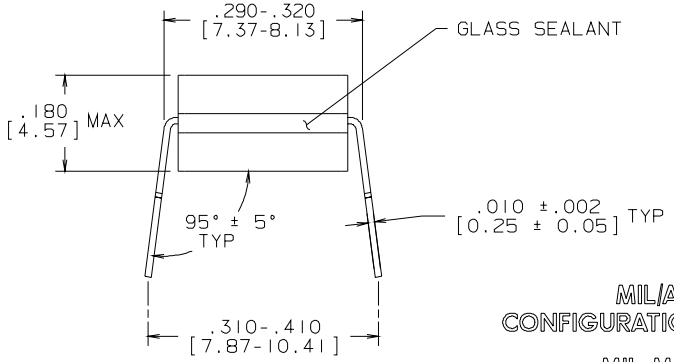
GRAPHICS#	DESCRIPTION
07082HRA2	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000405A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

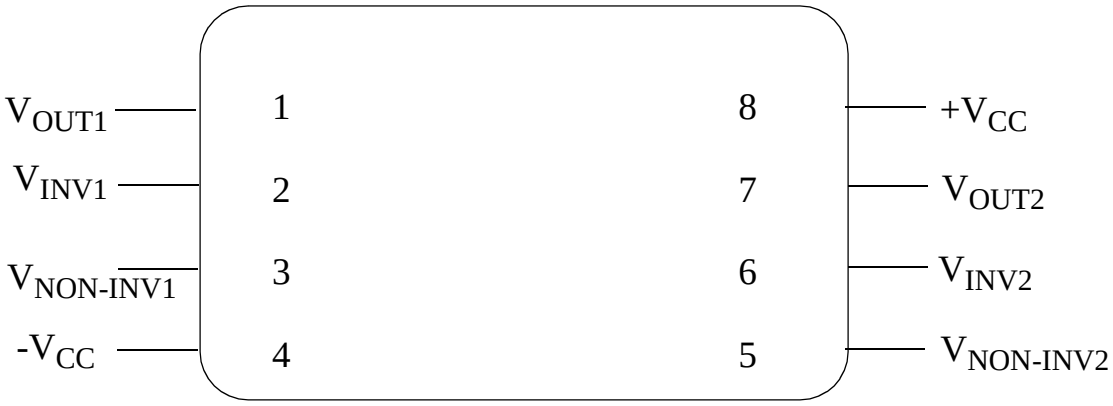
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC432J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000405A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003352	04/05/99	Shaw Mead	Initial MDS Release