ANALOGIC®

AH8304TM/TC

RGB 4-Bit Composite Video D/A Converters

Description

The **AH8304** video D/A converters are third generation hybrid devices that provide designers of low- to medium-cost color display systems with a complete, self-contained, TTL compatible, composite video subsystem in a 24 pin DIP. Offered as both an RGB 4-bit D/A only, or with integral color look-up table memory, the **AH8304** features advanced single-chip design that provides low power, high reliability, small size and low cost.

The **AH8304TM** color-mapped video D/A converter is designed for the color graphic system where space is at a premium. Both the functions of triple (RGB) video D/A converter **and** color look-up table memory are provided within a single 24-pin package. Data can be written into the internal 32 word RAM (one for each color channel) such that 32 colors can be defined out of a possible 4096 at any given time. During the display (Read) interval, any of these 32 colors can be addressed from a 5-bit bus. Separate Sync, Blanking and D/A Strobe control inputs are provided.

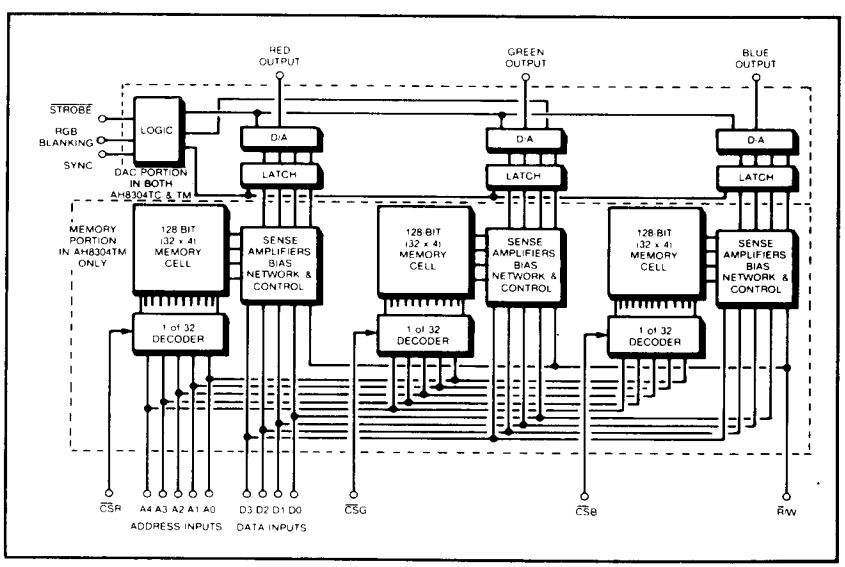
The **AH8304TC** D/A converter only is offered for those systems where a different configuration of look-up table memory is required. The D/A accepts 4-bit TTL data at an update rate of up to 100 MHz for each D/A. Common Blanking, Strobe and Sync (Green Channel only) controls are provided. The output of each channel is RS170/RS330/RS343 compatible, providing a 75Ω source impedance and 1 Vp-p output signal.

Features

- **Available with and without color look-up table**
  AH8304TC 100 MHz D/A
  AH8304TM 20 MHz D/A with 32 word memory
- **TTL compatible**
- **Synchronous Blanking**
- **4096 color palette**
- **RS170/RS330/RS343 composite video output**
- **Low Power Dissipation**
  2.0W maximum for D/A and memory
  1.75W maximum for D/A only
- **24-pin DIP**

Applications

- **Color graphic workstations**
- **Personal Computers**
- **Low-end CAD/CAM Systems**



AH8304TM/TC Block Diagram

SPECIFICATIONS

(All specifications are guaranteed at 25°C unless otherwise noted)
(All specifications applied to both AH8304TC and AH8304TM unless otherwise noted)

OUTPUT CHARACTERISTICS (Each Channel)

Gray Scale Output
0.000V to −0.643V, ±3% of Gray Scale; assumes load of 75Ω ±0.5% and −5.0V power supply

Recommended Load Impedance
75Ω, ±5%; dc to 50 MHz

Source (Thevenin) Impedance
75Ω, ±3%; dc to 50 MHz

LSB Size
42.9 mV, nominal

Full Scale Step Settling Time
5 ns typical, 7 ns maximum to 1 LSB after propagation delay

Glitch
Total Glitch Energy less than 250 pV-s for major code transition (0111 to 1000 or vice versa)

Cable Drive Capability
75Ω characteristic impedance; to avoid appreciable signal loss, total length should have no more than 7.5Ω dc resistance

RGB Blanking Level
−0.714V, with 71 mV (10 IRE Unit) setup; offset is 2 mV maximum, from 0°C to +55°C

Sync Level (Green Channel Only)
−1.000V; −0.286V (−40 IRE Units) with respect to Blanking level

TRANSFER CHARACTERISTICS (Each Channel)

Resolution
4-bits, 16 Gray Scale levels; 42.9 mV per step nominal

Reference White Level
1111 produces 0.000V absolute; 100 IRE Units relative to Blanking level

Reference Black Level
0000 produces −0.643V absolute, 10 IRE relative to Blanking level

Blanking Level
Active BLANKING control reset all DACs to 0000 and drives all outputs to −0.714V

Differential Non-linearity
±1/2 LSB, maximum

Monotonicity
Guaranteed

Transfer Gain (Slope) Tempco
±0.1% FSR/°C

RGB Blanking Input Delay
7 ns typical to 10% of final value after STROBE goes low

INPUT CHARACTERISTICS

Logic Levels (all inputs)
Standard TTL levels
Logic 1 >2.4V
Logic 0 <0.4V
No input to go below −0.3V
(CMOS limits)

Loading —
Data, Address, and Strobe
2 Unit Load
Control Inputs
2 Unit Load

Coding —
Data and Address
Binary

Data Update Rate
100 MHz maximum (AH8304TC); 20 MHz maximum (AH8304TM)

Memory Size
32 word by 4-bit (each RAM/channel) (AH8304TM only)

Control Inputs —
DAC $\overline{\text{Strobe}}$
Input data entered into all three DAC channels simultaneously on negative-going edge

Rise and Fall Time
<10 ns (10% to 90%)

DAC Propagation Delay
7 ns typical, $\overline{\text{STROBE}}$ to output, 50% points

Blanking Rise and Fall Time
<10 ns (10% to 90%)

RGB Blanking
Logic 1 on RGB Blanking input resets all DAC inputs to 0000 and drives all DAC outputs to −0.714V; RGB Blanking is synchronous with $\overline{\text{STROBE}}$; next $\overline{\text{STROBE}}$ after Blanking released loads input data

Sync
Logic 1 on RGB Blanking and Sync inputs resets all DAC inputs to 0000 drives Red and Blue outputs to −0.714V, and Green output to −1.000V absolute, −0.286V (−40 IRE Units) relative to Blanking level

Sync Rise and Fall Time
<10 ns (10% to 90%)

Read/Write
(AH8304TM only)
Logic 0 select Read operation; logic 1 selects Write operation; DAC outputs will retain previous Read value until STROBE input is applied; STROBE applied during Write operation causes Reference Black output level from all DACs

Address — 5-bits (A0 to A4)
(AH8304TM only)
Determines location in memory for Read or Write operation; used as Address input to load RAM arrays in Write mode and as look up table inputs in Read (Display) mode

Chip Select — CSR, CSG, CSB
(AH8304TM only)
CHIP SELECT for each channel (RED, GREEN, BLUE); logic 0 selects RAM channel for Read or Write operation; when deselected, RAM data output is all 0's to DAC inputs; DAC output of

deselected channels will retain last Read level if no STROBE applied, otherwise output will fall to Reference Black level; normally only one input at a time is enabled (selected) to write data to its corresponding RAM; all inputs are enabled to read data during display; these may be held at logic 0 throughout the read cycle

Data
16 Valid levels per channel;
D0-D3 (AH8304TC only)
R0-R3 (Red) (AH8304TM only)
G0-G3 (Green) (AH8304TM only)
B0-B3 (Blue) (AH8304TM only)

DYNAMIC CHARACTERISTICS

Width of Write Pulse
25 ns minimum (AH8304TM only)

Data and Address Before Write
30 ns minimum (AH8304TM only)

Data and Address Hold Time
20 ns minimum (AH8304TM only)

Data Setup Time
2 ns minimum (AH8304TC only)

Data Hold Time
1.5 ns minimum (AH8304TC only)

Address Access Time (after valid address)
48 ns maximum (AH8304TM only)

Chip Select Access
40 ns minimum (AH8304TM only)

Chip Select Disable
35 ns maximum (AH8304TM only)

POWER REQUIREMENTS

+5.0V, ±5%
50 mA maximum; 50 mVp-p ripple maximum (AH8304TC)
100 mA maximum; 50 mVp-p ripple maximum (AH8304TM)

−5.0V
200 mA maximum; 30 mVp-p ripple maximum (−4.75V to −5.5V operating range)

Power Dissipation
1.25W typical, 1.75W maximum (AH8304TC)
1.50W typical, 1.56W maximum (AH8304TM)

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +70°C

Storage Temperature
−25°C to +100°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

Dimensions
1.00" x 1.30" x 0.3" maximum
(25.4 x 33.14 x 7.62 mm)
24-pin triple width DIP

SPECIAL TESTING

Burn-In
24 Hours at +125°C to be performed prior to final test

Operation

The **AH8304TM** consists of two major functional blocks: (1) a memory organized as three 32-word by 4-bit blocks, one for each color channel, with common data, Read/Write control, and address inputs, separate chip select inputs and data outputs, and (2) a triple 4-bit D/A converter with common Sync, Blanking and Strobe control inputs. Data flow is always from the output of the memory to the input of the D/A converter.

During a Write operation, data to be loaded into the look-up table RAM is presented to the DATA inputs. The CHIP SELECT line for the color channel RAM that is to receive the data is brought low to enable it. The READ/WRITE line is pulsed, causing the data to be written into the RAM location corresponding to the address that is presented to the five ADDRESS inputs. The CHIP SELECT line is then brought high to disable that channel. The process can then be repeated for other addresses and/or color channels.

During a Read (display) cycle, all three CHIP SELECT lines are brought low to enable all channels, and the RAM address for the color to be displayed is presented to the ADDRESS inputs. After a propagation delay through the memory of 48 ns maximum, the data from the addressed RAM location appears at the output of the memory. The D/A STROBE line is then pulsed to latch the data into the D/A converter input register. After a propagation delay through the D/A converter, the corresponding analog output voltages appear at the three D/A outputs.

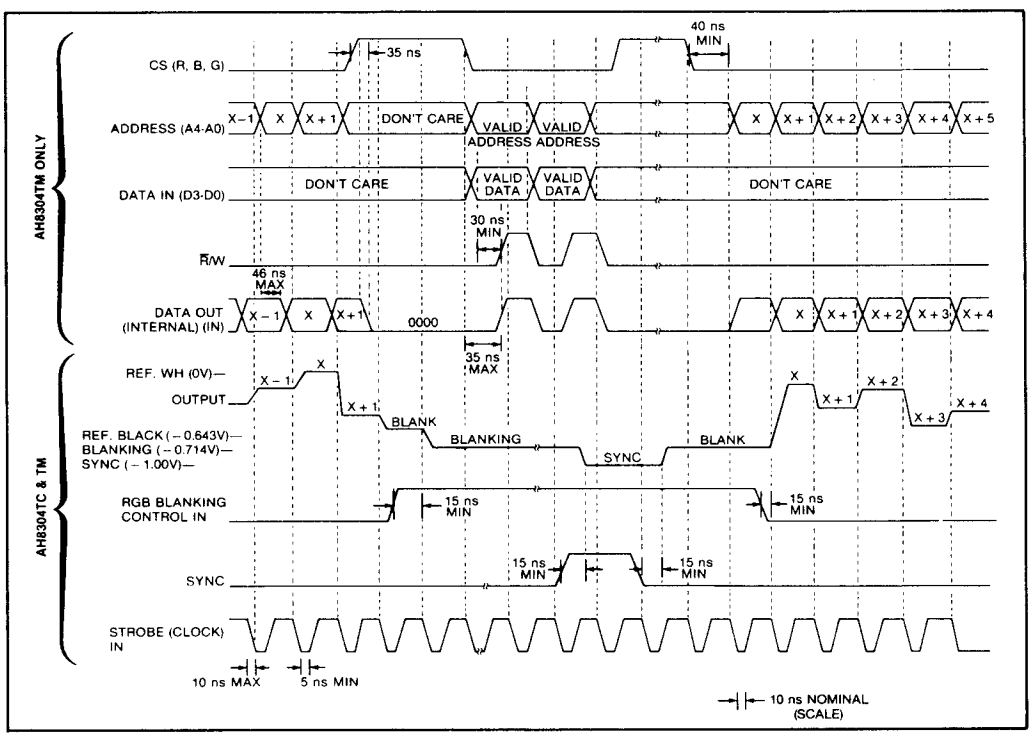
The **AH8304TC** D/A only (and the D/A portion of the **AH8304TM**) accepts a 4-bit data word for each of the three video channels (Red, Green, and Blue). The data is presented to the DATA inputs and held for the duration of the setup time, and the STROBE is pulsed to load the data into the three D/As. During the blanking interval, the BLANKING control line is activated by a logic 1. At the next STROBE pulse, this resets the three input registers to 0000 and drives the D/A outputs to the blanking level. When the SYNC line is activated, the output of the Green channel is driven to the sync level. At the end of the blanking/sync in-

terval, the SYNC and BLANKING controls are released (i.e. returned to a logic 0). At the next STROBE to the D/A, the data present at the DATA inputs to the D/A is loaded into the input registers, and will subsequently appear at the D/A outputs after the D/A propagation delay.

INPUTS							
DATA D3-D0	ADDRESS A4-A0	$\overline{CS}$	$\overline{R/W}$	BLANKING	SYNC	$\overline{STROBE}$	FUNCTION
X	VALID	L	L	L	L	H→L	RAM Data Loaded into DAC
X	X	L	L	H	L	H	Previous Data Value From RAM at DAC Output
X	X	L	L	H	L	H→L	DAC Output at Blanking Level
X	X	L	L	H	H	X	DAC Output at SYNC Level
X	X	H	L	L	L	H→L	DAC Output at Ref. Black Level
X	X	H	L	H	L	L	Last Data Value at DAC Output
VALID	VALID	L	H	H	L	H→L, then X	Data Loaded into RAM, DAC Out at Blanking Level
VALID	VALID	L	H	L	L	H→L	DAC Output at Reference Black

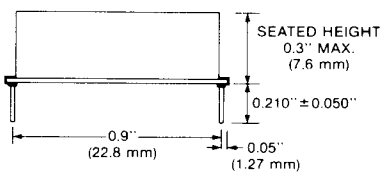
Truth Table — AH8304TM

X = don't care



TYPICAL TIMING AH8304TM/TC

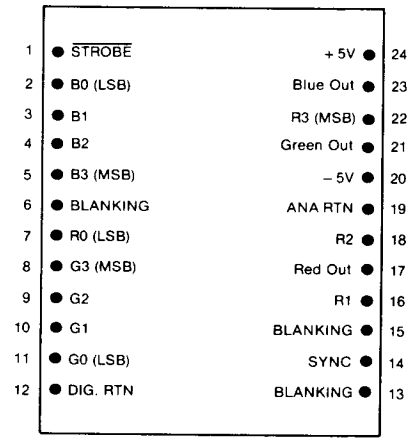
MECHANICAL



PINS ON 0.1" (2.5 mm) CENTERS

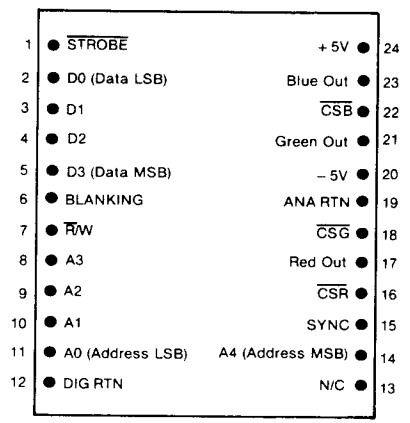
PINOUT

AH8304TC



Top View

AH8304TM



Top View

ORDERING GUIDE

20 MHz, RGB 4-bit D/A with 32 word lookup table memory.....Specify **AH8304TM**

100 MHz, RGB 4-bit D/A.....Specify **AH8304TC**