NEC
NEC Electronics Inc.

μPD42S64400, 42S65400
16,777,216 x 4-Bit
Dynamic CMOS RAM

Preliminary

September 1993

Description

The μPD42S64400 and μPD42S65400 are 64M-bit dynamic RAMs organized as 16,777,216 words by 4 bits. They are designed to operate from a single +3.3-volt power supply and have an optional fast-page mode.

Advanced polycide technology minimizes silicon areas and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state outputs are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles during a 256-ms refresh period.

Two versions of the 16M x 4-bit DRAM are available. The μPD42S64400 uses 8192 combinations of A_0 - A_{12} for $\overline{RAS}$-only refreshing and 4096 address combinations of A_0 - A_{11} to perform $\overline{CAS}$ before $\overline{RAS}$ and hidden refreshing of the memory during a 256-ms period. The μPD42S65400 uses 4096 address combinations of A_0 - A_{11} during a 256-ms period for all refresh modes.

The μPD42S64400 and μPD42S65400 are available in a 34-pin plastic SOJ and 34-pin plastic TSOP.

Features

- 16,777,216 x 4-bit organization
- Single +3.3-volt power supply
- Fast-page option
- Low power dissipation: 0.72 mW (max) standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh and self-refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 34-pin plastic SOJ and TSOP packaging

Ordering Information

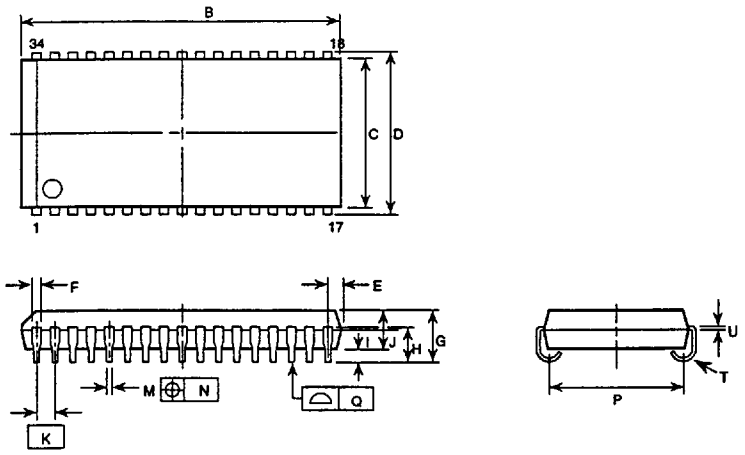
Part Number	Access Time (max)	R/W Cycle (max)	Fast-Page Cycle (max)	Active Power (max)	Package
μPD42S64400LG-A50	50 ns	90 ns	35 ns	360 mW	34-pin plastic SOJ
-A60	60 ns	110 ns	40 ns	324 mW	
-A70	70 ns	130 ns	45 ns	288 mW	
-A80	80 ns	150 ns	50 ns	252 mW	
μPD42S64400G7-A50	50 ns	90 ns	35 ns	360 mW	34-pin plastic TSOP
-A60	60 ns	110 ns	40 ns	324 mW	
-A70	70 ns	130 ns	45 ns	288 mW	
-A80	80 ns	150 ns	50 ns	252 mW	
μPD42S65400LG-A50	50 ns	90 ns	35 ns	468 mW	34-pin plastic SOJ
-A60	60 ns	110 ns	40 ns	396 mW	
-A70	70 ns	130 ns	45 ns	360 mW	
-A80	80 ns	150 ns	50 ns	324 mW	
μPD42S65400G7-A50	50 ns	90 ns	35 ns	468 mW	34-pin plastic TSOP
-A60	60 ns	110 ns	40 ns	396 mW	
-A70	70 ns	130 ns	45 ns	360 mW	
-A80	80 ns	150 ns	50 ns	324 mW	

μPD42S64400, 42S65400

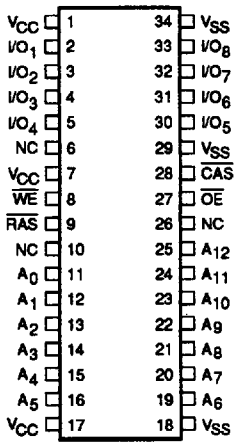
34-Pin Plastic SOJ (500-mil)

Item	Millimeters	Inches
B	22.42 ±0.2	.883 ±0.008
C	12.7	.500
D	13.72 ±0.2	.540 ±0.008
E	1.05 ±0.15	.041 +.007 −.005
F	0.74	.029
G	3.5 ±0.2	.138 ±.008
H	2.545 ±0.2	.100 ±.008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 +.004 −.005
N	0.12	.005
P*	11.94 ±0.2	.470 ±.008
Q	0.10	.004
T	0.85 rad	.033 rad
U	0.20 +0.10 −0.05	.008 +.004 −.002

* Item P to center of leads.



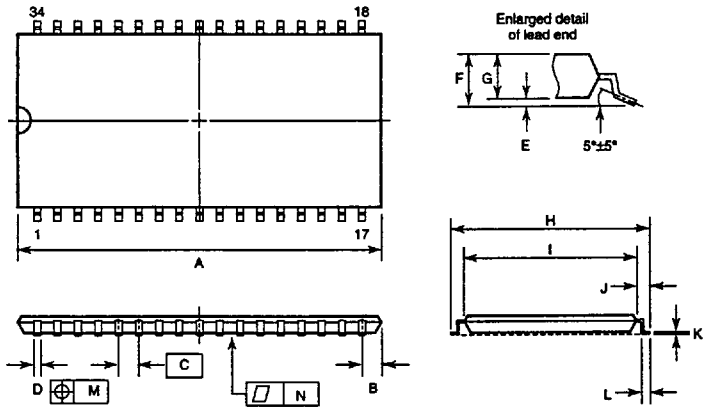
SOJ or TSOP



A_0 to $A_{11}(A_{12})$	Address inputs
I/O_1 to I/O_8	Data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Supply voltage
V_{SS}	Ground
NC	No connection

34-Pin Plastic TSOP (500 mil)

Item	Millimeters	Inches
A	22.66 max	.893 max
[illegible]	1.20 max	.048 max
[illegible]	1.27 (TP)	.050 (TP)
[illegible]	0.40 ±0.10	.016 ±.004
[illegible]	0.05 ±0.05	.002 ±.002
F	1.10 max	.044 max
G	0.97	.038
H	14.3 ±0.2	.563 ±0.008
I	12.7 ±0.1	.500 ±0.004
J	0.8 ±0.2	.031 ±.008
K	0.125 +0.10 −0.05	.005 +.004 −.002
L	0.5 ±0.1	.020 +.004 −.005
M	0.21	.009
N	0.10	.004



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