LSI LOGIC

5-Volt, Submicron 405K ASIC Products

Preliminary Datasheet

Cost Effective 5-Volt ASICs

405K ASIC products provide optimal solutions to meet the cost and performance requirements of today's 5-volt mainstream applications, such as PC system logic, add-in cards, peripherals, and networking. Available in both gate array and cell-based products, the 405K technology is based on LSI Logic's 0.65-micron effective channel length (0.8-micron drawn gate length) two-layer metal HCMOS process technology. The tight metal grid and resulting high gate density enables more than 250,000 usable gates in the cell-based implementation. An extensive selection of value-added elements—Phase-Locked Loop (PLL) cells, NTL/GTL I/O buffers, PECL I/O buffers, and Peripheral Component Interconnect (PCI) Bus I/O buffers—allow designers to maximize system performance. 405K technology is supported by industry-leading design and test tools and packaging options, which together provide a complete ASIC solution.

Features and Benefits

- Gate array architecture for quick prototype turnaround
- Cell-based architecture for high volume, price-sensitive designs
- Wide selection of high-performance I/O buffers, including NTL/GTL, PECL, and PCI
- High I/O-to-gate ratios with more than 600 fine-pitch I/O buffers to minimize silicon usage for pad-limited designs
- Cell-based low-profile I/O buffers to minimize die size
- Mixed signal interface capability
- Tight worst-case/best-case PVT delay window maximizes performance
- Maximized system integration with more than 250,000 usable gates in the cell-based implementation
- Extensive selection of advanced packaging with a wide range of pad pitches
- Comprehensive EDA design tool support for Synopsys, Cadence, Viewlogic, and Mentor Graphics design environments

Two ASIC Architectures

LCA405K Gate Array Series and LCB405K Cell-Based ASIC architectures are ideal for the specific integration and schedule requirements described below.

LCA405K Gate Array Series for Pad-Limited Designs and Fast Turnaround

The LCA405K Gate Array series offers flexibility and fast prototype and production using LSI Logic's Channel-Free® gate array architecture. The fine pad pitches, enabling more than 600 pads, provide the optimal solution for pad-limited designs.

- Fifteen masterslice sizes
- Up to 165,000 gates to support mid-range applications
- Metalized memory capability of up to 216 Kbits ROM and 54 Kbits RAM can be implemented on a single chip
- Fast prototype and production turnaround
- Three pad pitch options to minimize silicon usage for I/O-intensive designs

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The masterslices range in density from 4,500 to 162,000 usable gates with 104 to 656 I/O buffers. In Table 1, the pad counts for each masterslice correspond to the three different pad pitches for optimization of pad-limited designs. The "E" I/O buffers have the coarsest pad pitch. The "C" I/O buffers, supported by tape bonding, have the finest pad pitch.

Table 1. LCA405K Masterslices

Masterslice	Total Gates	Usable Gate		Pad Count by Pad Pitch Fine ◄——► Coarse		
		Nominal	Maximum	Tab (C)	WB (D)	WB(E)
LCA405 013	12,810	4,500	6,200	128	104	104
LCA405 023	22,518	7,900	10,800	168	136	128
LCA405 033	33,124	11,500	15,000	192	168	152
LCA405 040	40,176	14,000	18,900	216	176	168
LCA405 053	52,824	18,500	24,300	240	200	192
LCA405 074	74,382	26,000	33,500	288	232	224
LCA405 096	95,858	33,600	41,200	328	264	248
LCA405 122	122,472	43,000	52,700	368	296	280
LCA405 153	152,764	53,500	64,200	408	328	312
LCA405 185	185,136	64,800	77,800	448	360	344
LCA405 236	235,800	82,500	96,700	496	400	376
LCA405 276	274,510	96,000	112,500	536	432	408
LCA405 317	316,768	110,900	129,900	576	464	440
LCA405 355	355,488	124,400	145,800	608	488	464
LCA405 404	404,054	142,000	162,000	656	520	488

The actual usable gate count of a masterslice varies depending upon design methodology and content. Sixteen pads per die are dedicated to power and ground. Contact your LSI Logic applications engineer for detailed power and ground guidelines.

Refer to the "Packaging" section on page 10 for details on LSI Logic's advanced packaging options.

The LCA405K Gate Array Series supports asynchronous memory compilers for automatic generation of on-chip metalized memories. Table 2 provides maximum configurations and typical access times for low-power, metalized RAM and ROM.

Table 2. Low-Power, Metalized Memory

Memory Type	Maximum Configuration (bits x bits)	Typical Access Time (ns)
1-port asynchronous RAM (1 RW)	64 x 32	5.5
2-port asynchronous RAM (1R 1 RW)	64 x 32	5.6
ROM	256 x 32	5.9

LCB405K Cell-Based ASICs for the Highest Density

LCB405K Cell-Based ASICs offer the highest density and integration of the 405K ASIC products. The LCB405K macrocells are specially designed for high porosity and routability. In addition, the high density achieved with the LCB405K family results in an optimal die size that reduces costs for high-volume, price-sensitive applications.

- Minimal die size for economical high-volume production
- More than 250,000 usable gates
- Low-profile I/O cells to minimize die size for core-limited designs
- Mixed-signal interfaces
- Area-efficient memory compilers for implementing RAM and ROM
- Extensive selection of cells, which allows performance, area, and power trade-offs

LSI Logic tools automatically generate various custom memory sizes and help to shorten design development time. Maximum memory block sizes and cycle times for the low-power and high-density RAMs generated by the Memory Compiler tool are shown in Table 3.

Table 3. RAM and ROM Memory Compilers

Memory Type	Maximum Block Size (bits x bits)	Typical Access Time (ns)
1-port asynchronous low-power RAM	1000 x 72	7.7
2-port asynchronous low-power RAM	1000 x 72	12.1
1-port synchronous high-density RAM	2000 x 36	13.0
ROM	2000 x 72	12.0

Reliable, High-Volume Process and Manufacturing

405K products are manufactured using a reliable 0.65-micron effective, Channel-Free architecture at LSI Logic's high-volume production facility located in Tsukuba, Japan. The facility has produced more than 50 million 1-micron ASIC units.

Performance Optimization

405K products offer the following special circuitry to maximize chip-level and system-level performance:

- Single-ended trunk, double-ended trunk, and local buffered clock distribution architectures ensure less than 1.0 ns worst-case clock skew
- Balanced clock tree clock distribution architecture ensures less than 500 ps worst-case clock skew
- PLLs synchronize internal circuitry to within 300 ps of external ICs, provide on-chip frequency multiplication, and offer clock and data recovery
- Slew-rate controlled I/O buffers reduce ground bounce
- High-speed I/O buffers—including PCI, PECL, and GTL/NTL

Clock Distribution Circuitry

The clock distribution network distributes a clock signal to all clocked cells on a die. 405K clock distribution networks minimize clock skew by using the most suitable clock net scheme. See Table 4.

Table 4. Clock Distribution Specifications

Architecture	Worst-Case Skew (ps)	Max Operating Frequency (MHz)	Max Loads	Nominal Rise Time (ns)	Nominal Propagation Delay (ns)	I/O Pins
Single-ended tree	500	60	275	LCA 1.4-1.8 LCB 2.0-2.8	LCA 1.6-2.1 LCB 0.9-1.2	3
Double-ended tree	500	60	700	LCA 1.4-2.0 LCB 1.9-3.4	LCA 1.6-2.0 LCB 1.0-1.6	7
Local-buffered tree with LCLKBUF1A	1000	60	5000	LCA 1.6-2.0 LCB 1.8-2.4	LCA 3.0-3.6 LCB 2.5-2.9	7
with LCLKBUF2A	1000	60	5000	LCA 1.3-2.6 LCB 2.0-2.8	LCA 2.7-3.4 LCB 2.2-2.6	7
with LCLKBUF3A	1000	60	5000	LCA 1.6-2.0 LCB 1.8-2.5	LCA 2.8-3.4 LCB 2.0-2.4	7
Balanced clock tree	200-500	60	14,000	LCA 3.1-3.8 LCB 4.6-5.4	LCA 3.5-4.1 LCB 3.3-3.8	3

Phase-Locked Loops

To maximize system performance, clock skew must be minimized between different ICs in a system. PLLs synchronize the ASIC's internal clock to the external system clock, compensating for delays and changes in a clock signal caused by PC board trace lengths and capacitive and resistive loading effects. PLLs can also be used as frequency synthesizers to multiply up or divide down an incoming clock. The 405K analog PLL operates up to 150 MHz and reduces inter-chip clock skew to less than 350 ps. Specifications for high-frequency, low-jitter PLLs are shown in Table 5.

Table 5. PLL Specifications

Parameter	Specification
Operating frequency	33, 50, 66, 80, 150 MHz
Phase detection error	< 250 ps
Phase jitter	< 100 ps
Total error	< 350 ps
Power dissipation	< 100 mW (frequency dependent)

I/O Options

Designers may choose from a large selection of LSI Logic I/O buffers that all interface with existing bus standards. 5-volt I/O types offer separate CMOS and TTL outputs as well as the following options:

- 2 to 24 mA drive strength
- Moderate and full slew-rate control buffers
- Input multiplexer
- Input with pullup, pulldown resistors
- Open drain outputs
- Inverting and non-inverting inputs

High-Performance, Low-Noise I/O Buffers

LSI Logic minimizes I/O bottlenecks by offering a wide range of high-performance I/O solutions summarized in Table 6. The 405K Peripheral Component Interconnect (PCI) I/O makes it easy to interface to industry-standard PCI buses. It is an off-the-shelf, fully PCI-compliant solution that makes 405K ideal for EDP applications. Because the PCI I/O buffer uses only a single I/O slot, more PCI buffers can be included on a single die, and the die size is therefore minimized.

Table 6. I/O Types

I/O Type	Max Frequency (MHz)	Slots	Pads
TTL/CMOS	65	1	1
Matched-impedance TTL	100	1	1
Single-ended PECL	155	1	1
Differential PECL	155	2	2
Backplane GTL/NTL	83	2	1
PCI buffers	33	1	1

For telecommunications and other applications that require high-speed I/O buffers, Pseudo-ECL (PECL) is available in both single-ended and differential formats. PECL supports the 155 MHz high-speed I/O requirements for SONET interfacing in telecommunication applications.

405K GTL/NTL I/O buffers offer 83 MHz backplane performance. GTL/NTL offers high speed and signal quality without the power consumption penalty of bipolar interfaces.

Methodology Speeds Development and Ensures Right-First-Time™ Silicon

LSI Logic's Hierarchical Design Methodology (HDM) speeds development to meet ever shrinking time-to-market requirements. HDM, illustrated in Figure 1, reduces risk and ensures first-time success for even the most complex devices. System requirements are verified and managed at all levels of the design hierarchy, from design entry to completion of layout.

Size, power, performance, and testability specifications are budgeted to the top-level hierarchical system partitions and then subdivided to lower levels of the hierarchy until all hierarchical blocks have individual design constraints. Block-level iterations take place among design and test synthesis, floorplanning, and timing driven layout. Layout proceeds one block at a time with each layout checked against specifications. Final chip simulation verifies design goals.

Compared to flat methodologies, hierarchical design results in higher performance, minimal clock skew, lower power dissipation, timing predictability, and substantially improved design productivity for large designs.

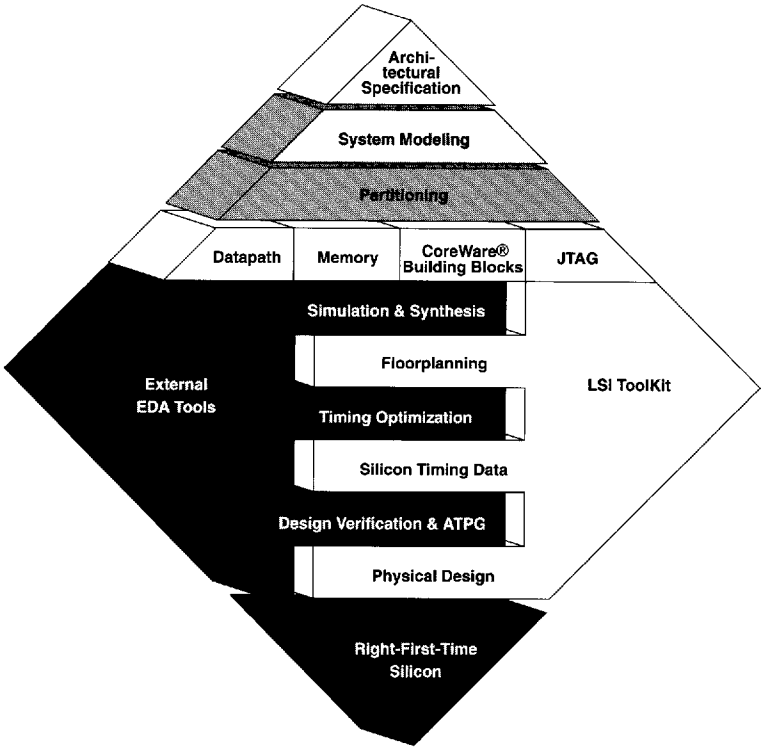


Figure 1. The LSI Logic Hierarchical Design Methodology

Accurate timing calculations are based on pin-to-pin timing models, actual or estimated wire lengths, wire capacitance, and derating factors for temperature, voltage, and process. Standard delay format is supported for back annotation of actual layout delays to the netlist.

LSI ToolKit supports HDM with a robust set of tools that integrate with industry-leading standard tools. LSI ToolKit capabilities include:

- Delay prediction
- Test insertion
- Test vector generation or translation
- Memory model generation
- Logic block synthesis
- Hierarchical layout
- Floor planning
- Support of industry standards: VHDL and Verilog

405K libraries are available in design kits for the following EDA environments:

- Synopsys
- Cadence
- Mentor Graphics
- Viewlogic

Logic Block Synthesis

The Logic Block Synthesis tool, which is an automated function generator, is included in LSI Logic's Hierarchical Design Methodology. It generates 405K netlists for function blocks ranging from simple adders and counters to complex floating-point multipliers and RAMBIST built-in self test circuitry. The generated netlists can be merged into a design as flat netlists, or they may be placed and routed as standalone functions. LSI Logic engineering design services are available to develop additional hardwired macrocells and macrofunctions. Example macrocells and macrofunctions that can be developed include:

- Adders – carry select, carry look-ahead, carry skip, ripple, advanced parallel
- Counters – Johnson, ripple, binary, shift, gray code
- Multiplexers – 2:1 to 16:1, up to 64 bits wide
- Incrementers and decrementers
- Decoders – 2:4 to 7:128
- Shifters – clear, set and/or load, synchronous or asynchronous
- Fall through FIFOs – Words: 2 to 1024; Bits: 1 to 128
- Comparators
- Multipliers – array or Wallace tree, signed or unsigned, pipelined or single-stage
- IEEE 1149.1 (JTAG) support circuitry – TAP controller, instruction register with instruction options, device ID register
- Barrel shifters – logical, arithmetic, circular
- ALUs – industry-standard 74181 or 2901 function sets
- Multiplier/Accumulator (sum-of-products) – multiple pipeline support
- RAMBIST – testability support for 405K metalized or embedded memory

Megafunctions

Large, high-performance, softwired megafunctions are available for 405K. In addition, LSI Logic engineering design services are available for specific megafunction development. Contact your local LSI Logic sales representative for a list of available functions or for more details regarding megafunction development.

Mixed-Signal Cores

Mixed-signal cores provide standardized interface functionality for system solutions in a variety of applications. Listed below are examples of 405K mixed-signal cores:

- Ethernet 10Base T interface
- Ethernet AUI interface
- Video DAC up to 135 MHz
- Programmable frequency synthesizer up to 150 MHz

High Fault Coverage Testability

LSI Logic's suite of testability tools and support of third-party testability tools ensure high device quality while speeding time-to-market. The quality of the 405K product line is ensured with the test tools described below.

Test Builder for Internal Scan Testing (Fully Compliant with IEEE 1149.1 Methodology)

Test Builder is an advanced scan design environment that reduces time-to-market. Its Scan Chain Synthesis achieves predictable test results by automatically inserting an optimized scan path. Scan ATPG automatically develops test vectors and achieves more than 99% stuck-at-fault coverage. Test Builder supports all synchronous blocks, random logic, core, and megafunction testing. Test Builder performs scan chain reordering, which minimizes routing congestion and increases testing performance.

JTAG Builder for Test Access Port and IEEE 1149.1 Boundary-Scan Insertion

JTAG Builder inserts JTAG logic and Test Access Port (TAP) controller logic. It generates the BSDL description of the boundary scan circuits automatically and provides a full set of test vectors for boundary scan logic.

RAMBIST Builder for Automatic Insertion of Built-In Self Test into Memory Blocks

RAMBIST Builder provides Built-In Self Test logic for on-chip embedded memories. RAMBIST tests memory at speed and reduces test time. It assures high product quality at low test cost and requires minimum silicon overhead. RAMBIST's test controller writes comprehensive marching patterns into memory, reads them back, and provides a pass/fail flag, which speeds test results analysis. For detailed failure analysis, a debug diagnostic mode makes it possible to shift out the memory contents at a failing address. In addition to stuck-at faults, RAMBIST is able to detect transition, coupling, and timing failures. RAMBIST Builder also provides full scan to test the RAMBIST logic.

Packaging

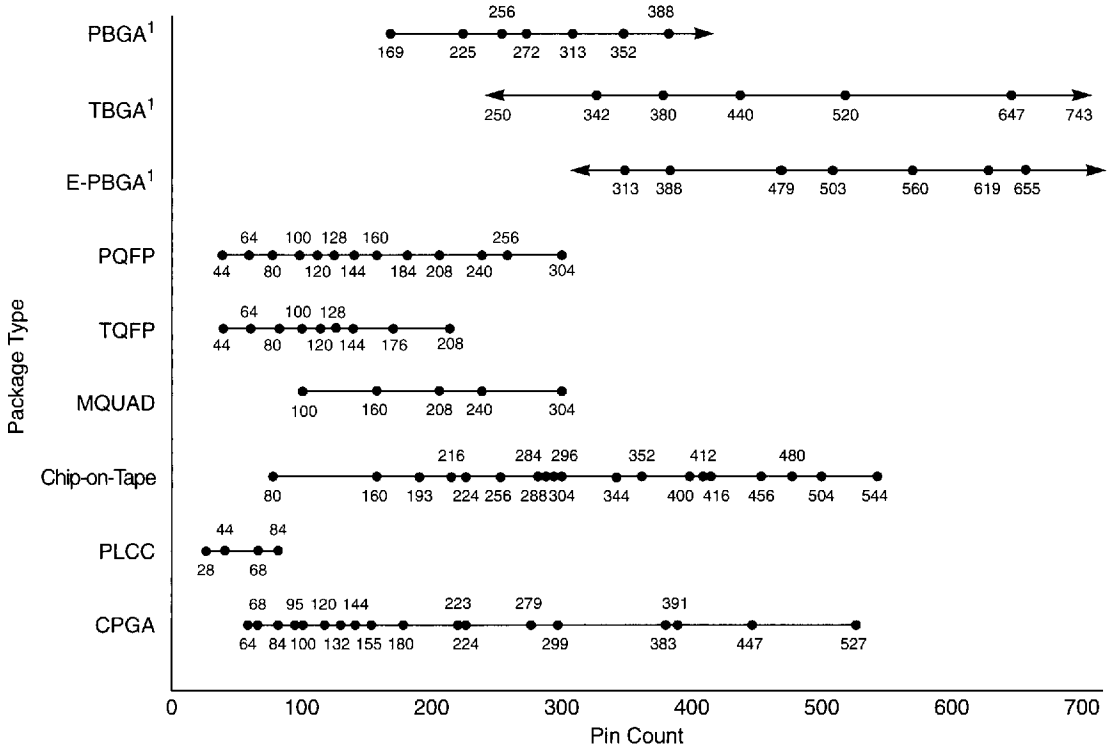
LSI Logic offers industry-standard, cost-effective PQFP, TQFP, and MQUAD packages for mainstream applications. The families of advanced Ball Grid Array (BGA, E-PBGA, and TBGA), Ceramic Pin Grid Array (CPGA), and COT (Chip-On-Tape) packages are also available for high pin count, high-frequency applications. All packaging solutions benefit from LSI Logic's experience in providing devices in high volume, on time, and within specification. Across all packaging technologies, LSI Logic provides thermal, electrical, and mechanical modeling of the package and silicon combination. When system design trade-offs need to be made, the designer can rely on the experience of LSI Logic's Field Design Engineers to help choose the package best suited for the application. Through research, investment, and by driving industry standards, LSI Logic continues to be the first to market with cost-effective packaging solutions that support high-performance requirements.

Table 7 lists the compatibility of available 405K pad pitches and various packages. Figure 2 provides information on available package pin counts.

Table 7. Package Pad Pitch Compatibility

	Pad Pitch Fine ← → Coarse		
Package	**TAB (C)**	**WB (D)**	**WB (E)**
PQFP/TQFP		x	x
PQFPi[1]	x		
PBGA		x	x
MQUAD		x	x
PGA		x	x
TBGA	x	x	x
E-PBGA		x	x
Chip-on-Tape	x	x	x

1. PQFP with package interposer.



1. New package families—pin count extensions underway.

Figure 2. Package Pin Counts

Specifications This section provides the electrical specifications for the 405K technology. Table 8 lists the 405K DC characteristics. Refer to the 405K databooks for AC characteristics.

Table 8. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Voltage input LOW TTL inputs CMOS levels				 0.8 0.2 V_{DD}	V
V_{IH}	Voltage input HIGH TTL inputs TTL Schmitt trigger inputs CMOS levels	 (Com/Ind/Mil temp range) (Ind/Mil temp range)	 2.0 2.25 0.7 V_{DD}			 V V V
V_T	Switching threshold	TTL CMOS		1.5 2.5		V V
V_{T+}	Schmitt trigger, positive-going threshold	CMOS TTL		1.77 2.0	2.0 2.25	V V
V_{T-}	Schmitt trigger, negative-going threshold	CMOS (5 V) TTL	1.0 0.8	1.5 1.04		V V
	Hysteresis, Schmitt trigger	CMOS (V_{IL} to V_{IH}) TTL (V_{IL} to V_{IH})	1.0 0.4	1.5 0.8		V
I_{IN}	Input current, CMOS, TTL Inputs Inputs with pulldown resistors (5 V) Inputs with pulldown resistors (3.3 V) TTL inputs and inputs with pullup resistors (5 V) TTL inputs and inputs with pullup resistors (3.3 V)	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{DD} V_{IN} = V_{SS} V_{IN} = V_{SS}	-10 35 35 -35 -35	±1 115 -115 -115 -115	10 222 138 -214 -131	µA µA µA µA µA
V_{OH}	Voltage output HIGH Type B1 Type B2 Type B4 Type B6 Type B8 Type B12[1]	Commercial and Military I_{OH} = -1 mA I_{OH} = -2 mA I_{OH} = -4 mA I_{OH} = -6 mA I_{OH} = -8 mA I_{OH} = -12 mA	 2.4 2.4 2.4 2.4 2.4 2.4			 V V V V V V
V_{OL}	Voltage output LOW Type B1 Type B2 Type B4 Type B6 Type B8 Type B12[1]	Commercial and Military I_{OL} =1 mA I_{OL} = 2 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 8 mA I_{OL} =12 mA		 0.2 0.2 0.2 0.2 0.2 0.2	 0.4 0.4 0.4 0.4 0.4 0.4	 V V V V V V
I_{OZ}	3-state output leakage current	V_{OH} = V_{SS} or V_{DD}	-10	±1	10	µA
I_{OS}	Output short circuit current[2]	V_{DD} = 5.25 V, V_O = V_{DD} V_{DD} = 5.25 V, V_O = V_{SS} V_{DD} = 3.45 V, V_O = V_{DD} V_{DD} = 3.45 V, V_O = V_{SS}	37 -117 50 -99	90 -75 110 -60	140 -40 182 -31	mA mA mA mA
I_{DD}	Quiescent supply current	V_{IN} = V_{DD} or V_{SS}	User-design dependent			
C_{IN}	Input capacitance	Any input and bidirectional buffers	2.5			pF
C_{OUT}	Output capacitance	Any output buffer[3]	2.0			pF

1. Requires two output pads.
2. Type B4 output. Output short circuit current for other outputs will scale.
3. Output using single buffer structure (excluding package).

Table 9 provides power dissipation values for a 2-input NAND gate (ND2) as an example of 405K power dissipation values. Table 10 lists the absolute maximum rating for the 405K technology. Operation beyond the limits specified in this table may cause permanent device damage. Table 11 lists the recommended operating conditions for 405K. Operation beyond these limits may impair the useful life of the device.

Table 9. Power Dissipation

405K Macrocell	Power Dissipation (μW/MHz/gate)[1]
LCA405K ND2 (2-input NAND)	2.50
LCB405K ND2 (2-input NAND)	2.30

1. Conditions: Standard temperature, voltage, and process with 0.5 mm of metal and a fanout of two (equivalent to approximately 10 standard loads).

Table 10. Absolute Maximum Rating (Referenced to V_{SS})

Parameter	Symbol	Limits[1]	Unit
DC supply voltage	V_{DD}	-0.3 to +7	V
Input voltage	V_{IN}	-1.0 to V_{DD}+0.3	V
DC input current	I_{IN}	± 10	mA
Storage temperature range (plastic)	T_{STG}	-40 to +125	°C

1. Note that the ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation.

ESD

Per ML-STD-883 Test Method 3015, Notice 8, Spec 2001V
Latchup over/undershoot: ±150 mA, 125° C
V_{DD} overstress: 2 * V_{DD} (7.2 V)

Table 11. Recommended Operating Conditions

Parameter	Symbol	Limits[1]	Unit
DC supply voltage	V_{DD}	+4.5 to 5.5	V
Operating ambient temperature range industrial commercial	 T_A T_A	 -40 to +85 0 to +70	 °C °C
Junction temperature	T_J	≤150	°C

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, may result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions.