Octal bidirectional latched pi-bus transceiver

54F776

DESCRIPTION

The 54F776 is an octal latched transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristic impedance range of 20 to 50Ω and is terminated on each end with a 30 to 40Ω resistor.

The 54F776 is an octal bidirectional transceiver with Open-Collector B and 3-State A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2V and features a controlled linear ramp to minimize crosstalk and ringing on the bus.

A separate high level control voltage (V_X) is provided to prevent the A side output high level from exceeding future high density processor supply voltage levels. For 5V systems, V_X is simply tied to V_{CC}.

FEATURES

- Latching Transceiver
- Controlled output ramp
- High drive Open-Collector output current with minimum output swing
- Pi-Bus specification compatible
- Multiple package options
- Controlled power on/off sequence

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
28-Pin Ceramic DIP (600mil)	54F776/BXA	GDIP1-T28
28-Pin Flatpack	54F776/BYA	GDFP2-F28
28-Pin LLCC	54F776/B3A	CQCC2-N28

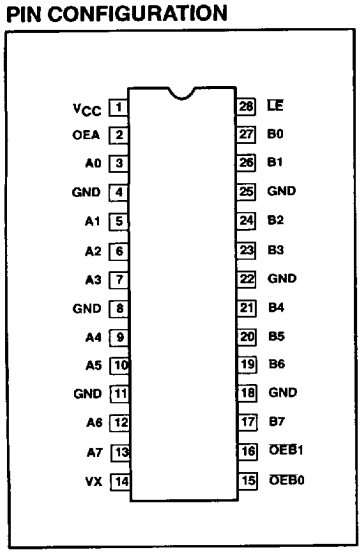
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

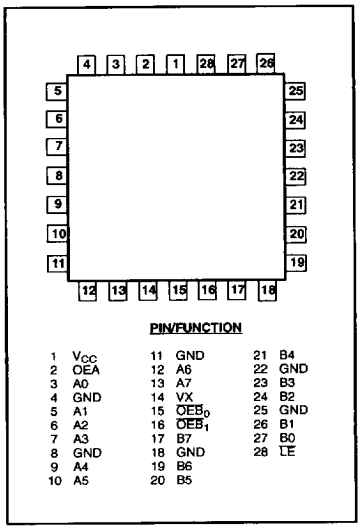
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ao - A7	PNP latched input	3.5/0.1167	70μA/70μA
B0 - B7	Data input with threshold circuitry	5.0/0.167	100μA/100μA
OEA	A output Enable input (active-High)	1.0/0.033	20μA/20μA
$\overline{OEB0}$, $\overline{OEB1}$	B output Enable inputs (active-Low)	1.0/0.033	20μA/20μA
$\overline{LE}$	Latch Enable input (active-Low)	1.0/0.033	20μA/20μA
A0 - A7	3-State outputs	150/33.3	3mA/20mA
B0 - B7	Open-Collector outputs	OC*/166.7	OC*/100mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state. * OC = Open-Collector

PIN CONFIGURATION



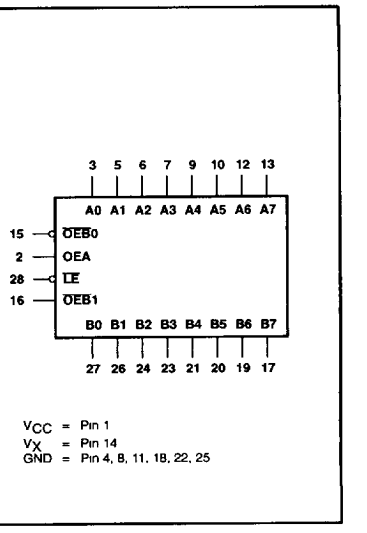
LLCC PIN CONFIGURATION



PIN/FUNCTION

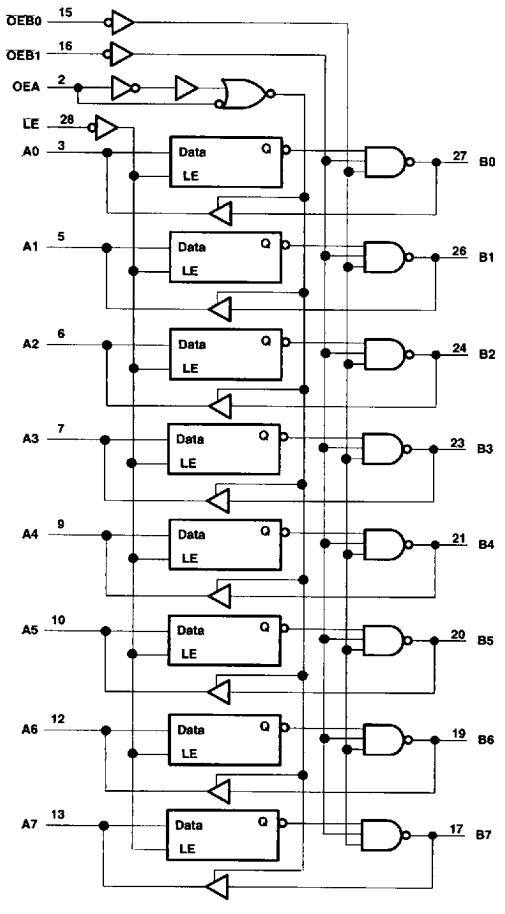
1	V_{CC}	11	GND	21	B4
2	OEA	12	A6	22	GND
3	A0	13	A7	23	B3
4	GND	14	VX	24	B2
5	A1	15	$\overline{OEB_0}$	25	GND
6	A2	16	$\overline{OEB_1}$	26	B1
7	A3	17	B7	27	B0
8	GND	18	GND	28	$\overline{LE}$
9	A4	19	B6		
10	A5	20	B5		

LOGIC SYMBOL



V_{CC} = Pin 1
V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

LOGIC DIAGRAM



V_{CC} = Pin 1, V_X = Pin 14,
GND = Pin 4, 8, 11, 18, 22, 25

PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0	3	I/O	PNP latched input/3-State output (with V_X control option)
A1	5	I/O	
A2	6	I/O	
A3	7	I/O	
A4	9	I/O	
A5	10	I/O	
A6	12	I/O	
A7	13	I/O	
B0	27	I/O	Data input with special threshold circuitry to reject noise/Open-Collector output High current drive
B1	26	I/O	
B2	24	I/O	
B3	23	I/O	
B4	21	I/O	
B5	20	I/O	
B6	19	I/O	
B7	17	I/O	
$\overline{OEB}0$	15	I	Enables the B outputs when both pins are Low
$\overline{OEB}1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

FUNCTION TABLE

INPUTS						LATCH	OUTPUTS		MODE
An	Bn[3]	$\overline{LE}$	OEA	$\overline{OEB0}$	$\overline{OEB1}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	H	A 3-State, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A 3-State, Latched data to B
-	-	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
-	H	H	H	L	L	H[2]	H	Off[2]	Preconditioned Latch enabling data
-	L	H	H	L	L	H[2]	L	Off[2]	transfer from B to A
-	-	H	H	L	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	X	H	Z	Off	B Off and A 3-State
L	X	L	L	H	X	L	Z	Off	
X	X	H	L	H	X	Qn	Z	Off	
-	H	L	H	H	X	H	H	Off	B Off, Data from B to A
-	L	L	H	H	X	L	L	Off	
-	H	H	H	H	X	Qn	H	Off	
-	L	H	H	H	X	Qn	L	Off	
H	X	L	L	X	H	H	Z	Off	B Off and A 3-State
L	X	L	L	X	H	L	Z	Off	
X	X	H	L	X	H	Qn	Z	Off	
-	H	L	H	X	H	H	H	Off	B Off, Data from B to A
-	L	L	H	X	H	L	L	Off	
-	H	H	H	X	H	Qn	H	Off	
-	L	H	H	X	H	Qn	L	Off	

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
- = Input not externally driven
Z = High Impedance (off) state
Qn = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transititon
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}$0 and $\overline{OEB}$1 are Low and $\overline{LE}$ is High
(3) = Precaution should be taken to insure that the B inputs do not float. If they do, they are equal to a Low state
off = Applies to "B" (OC) outputs only. Indicates that the outputs are turned off

CONTROLLED POWER SEQUENCING OPERATION

The F776 has a design feature which controls the output transitions during power up (or down). There are two possible conditions that occur.

1. When $\overline{LE}$ = Low and $\overline{OEB}$n = Low, the B outputs are disabled until the $\overline{LE}$ circuit can take control. This feature insures that the B outputs will follow the A inputs and allow only one transition during power up (or down).

2. If $\overline{LE}$ = High or $\overline{OEB}$n = High, then the B outputs will remain disabled during power up (or down).

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	V_{OH} output level control voltage (A outputs)		-0.5 to +7 0	V
V_I	Input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A0 - A7, B0 - B7	-0.5 to 5.5	V
I_I	Input current		-40 to +5	mA
V_O	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	B0 - B7	200	mA
		A0 - A7	40	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B0 - B7	2.0			V
		B0 - B7[4]	1.60			
V_{IL}	Low-level input voltage	Except B0 - B7			0.8	V
		B0 - B7[4]			1.45	
I_{IK}	Input clamp current	Except A0 - A7			-18	mA
		A0 - A7			-40	mA
I_{OH}	High-level output current	A0 - A7			-3	mA
I_{OL}	Low-level output current	A0 - A7			20	mA
		B0 - B7			100	
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High-level output current	B0 - B7	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2.0V, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A0 - A7	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH} = -3mA, V_X = V_{CC}	2.5	2.9	V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A0 - A7	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 20mA, V_X = V_{CC}		0.3	0.5	V
		B0 - B7		I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A0 - A7	V_{CC} = Min, I_I = I_{IK}				-0.5	V
		Except A0 - A7	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = Max, V_I = 7.0V			1	100	µA
		A0 - A7	V_{CC} = Max, V_I = 5.5V			0.01	1	mA
		B0 - B7	V_{CC} = Max, V_I = 5.5V			0.01	1	mA
I_{IH1}	High-level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = Max, V_I = 2.7V				20	µA
		B0 - B7	V_{CC} = Max, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = Max, V_I = 0.5V				-20	µA
		B0 - B7	V_{CC} = Max, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A0 - A7	V_{CC} = Max, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A0 - A7	V_{CC} = Max, V_O = 0.5V				-70	µA
I_X	High-level control current		V_{CC} = Max, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}$n = 2.7V, A0 - A7 = 2.7V, B0 - B7 = 2.0V		-100		100	µA
			V_{CC} = Max, V_X = 3.13V & 3.47V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}$n = A0 - A7 = 2.7V, B0 - B7 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A0 - A7 only	V_{CC} = Max, Bn = 1.6V, OEA = 2.0V, $\overline{OEB}$n = 2.7V		-60	-75	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max				100	mA
		I_{CCL}	V_{CC} = Max, V_{IL} = 0.5V				145	mA
		I_{CCZ}	V_{CC} = Max, V_{IL} = 0.5V				100	mA
I_{OFF}	Power-off output current	B0 - B7	Bn = 2.1V, V_{CC} = 0.0V, V_{IL} = Max, V_{IH} = Min				100	µA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A SIDE LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	7.0 4.5	9.5 6.0	12.5 9.0	4.5 6.0	13.0 9.5	ns ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 3, 4	8.0 8.5	10.5 11.0	13.5 13.5	7.0 8.5	16.5 18.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 3, 4	2.0 2.0	3.5 4.5	6.0 7.0	2.0 2.0	7.5 8.0	ns ns

SYMBOL	PARAMETER	TEST CONDITION	B SIDE LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	3.0 3.0	5.0 4.0	7.5 7.5	1.5 2.5	10.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.5 3.5	5.0 5.0	8.0 8.0	2.5 2.5	11.0 9.5	ns ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}$n to B	Waveform 1, 2	3.0 3.5	4.5 5.5	7.0 9.0	1.5 3.0	9.5 10.5	ns ns
t_{TLH} t_{THL}	Transition time, B side 1.3V to 1.7V, 1.7V to 1.3V	Test Circuit and Waveform	1.5 1.5	2.0 2.0	4.5 4.5	1.5 1.5	5.5 5.0	ns ns

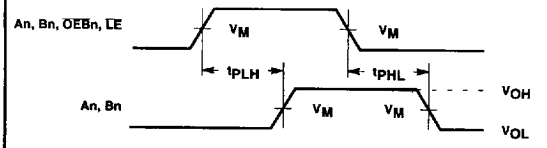
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, C_D = 30pF, R_u = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_S(H)$ $t_S(L)$	Set-up time A to $\overline{LE}$	Waveform 5	3.5 4.5			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 5	0.0 0.0			0.0 0.0		ns ns
$t_w(L)$	$\overline{LE}$ Pulse width Low	Waveform 5	4.0			7.0		ns

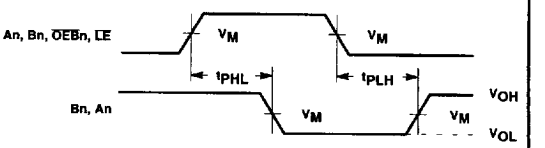
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} = 1.9V and for V_{IL} = 1.2V, however, the specified test limits and conditions are guaranteed.

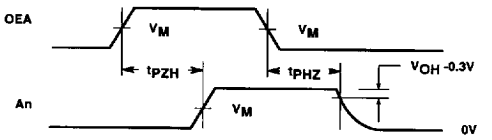
AC WAVEFORMS



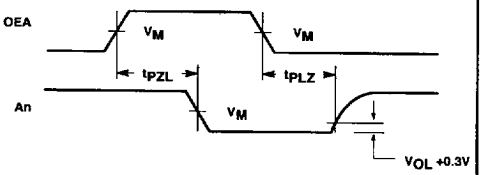
Waveform 1. Propagation Delay for Data to Output



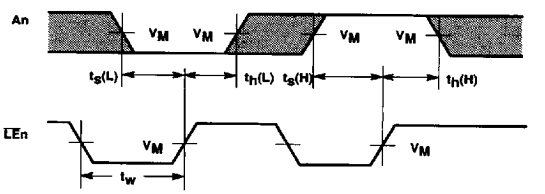
Waveform 2. Propagation Delay for Data to Output



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



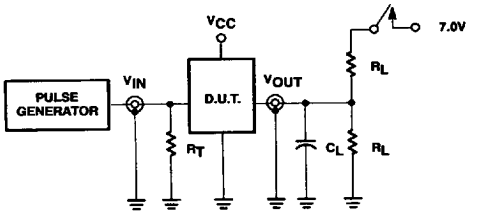
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 5. Data Setup and Hold Times

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance

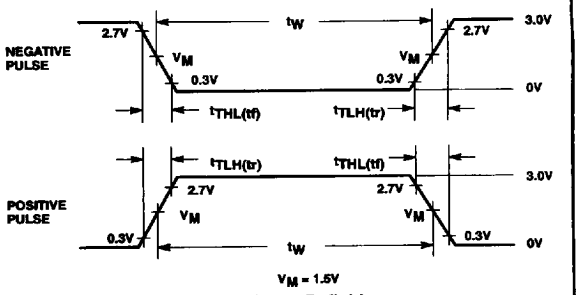
TEST CIRCUITS AND WAVEFORM



Test Circuit for 3-State Outputs on A Port

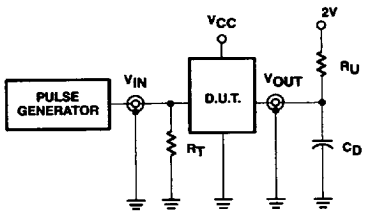
SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed
	open



V_M = 1.5V

Input Pulse Definition



Test Circuit for 3-State Outputs on B Port

FAMILY 54F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Side	3.0V	0.0V	1MHz	500ns	≤2.5ns	≤2.5ns
B Side	2.0V	1.0V	1MHz	500ns	≤4.0ns	≤4.0ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capicitance includes jig and probe capicitance; see AC Characteristics for value.
R_U = Pull up resistor; see AC Characteristics for value.