HYUNDAI

HY638256 Series
32Kx8bit CMOS FAST SRAM

DESCRIPTION

The HY638256 is a high-speed 32,768 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. This high reliability process coupled with high-speed circuit design techniques, yields maximum access time of 15ns. The HY638256 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. It is suitable for use in high-density high-speed system applications.

FEATURES

- Single 5V±10% Power Supply
- High speed - 15/20/25ns(max.)
- Low power consumption(Max.)

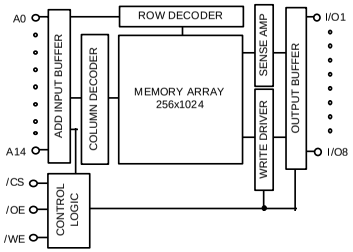
Mode	Conditions		Current	Units
Operating	15ns		100	mA
	20/25ns		90	mA
Standby	TTL		30	mA
	CMOS		2	mA
		L	100	uA

- Battery backup(L-part)
  - 2.0V(min) data retention
- Fully static operation and Tri-state outputs

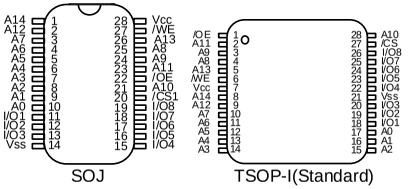
- No clock or refresh required

- TTL compatible inputs and outputs
- Standard pin configuration
  - 28pin 300mil SOJ
  - 28pin 8 x 13.4 mm TSOP-I

BLOCK DIAGRMM



PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0~A14	Adderss Input
I/O1~I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

ORDERING INFORMATION

Part No.	Speed	Power	Package
HY638256J	15/20/25		SOJ
HY638256LJ	15/20/25	L-part	SOJ
HY638256T1	15/20/25		TSOP-I Standard
HY638256LT1	15/20/25	L-part	TSOP-I Standard

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V±10%, T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Type	Max	Unit
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-2	-	2	uA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-2	-	2	uA
I_{CC1}	Average Operating Current	/CS = V_{IL}, $I_{I/O}$ = 0mA, Min. Duty Cycle = 100%	15ns	-	-	100	mA
			20/25ns	-	-	90	mA
I_{SB}	TTL Standby Current (TTL Inputs)	/CS = V_{IH}, V_{IN}=V_{IH} or V_{IL}, Min. Cycle		-	-	30	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	/CS ≥ V_{CC}-0.2V, V_{IN} ≥		-	-	2	mA
		V_{CC}-0.2V or V_{IN} ≤ 0.2V	L	-	20	100	uA
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA		2.4	-	-	V

Note : Typical values are at Vcc = 5.0V, T_A = 25°C

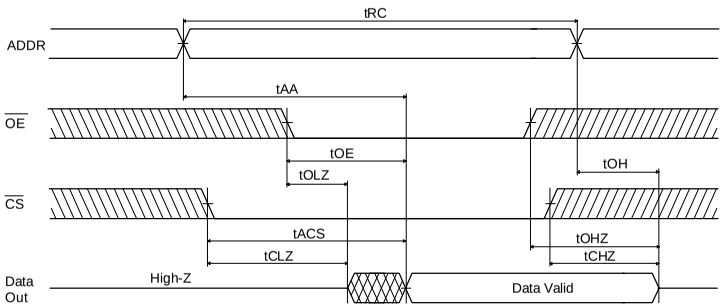
AC CHARACTERISTICS

Vcc = 5.0V±10%, T_A = 0°C to 70°C, unless otherwise specified.

#	Symbol	Parameter	-15		-20		-25		Unit
			Min	Max	Min	Max	Min	Max	
	READ CYCLE								
1	tRC	Read Cycle Time	15	-	20	-	25	-	ns
2	tAA	Address Access Time	-	15	-	20	-	25	ns
3	tACS	Chip Select Access Time	-	15	-	20	-	25	ns
4	tOE	Output Enable to Output Valid	-	8	-	10	-	12	ns
5	tCLZ	Chip Select to Output in Low Z	3	-	3	-	3	-	ns
6	tOLZ	Output Enable to Output in Low Z	3	-	3	-	3	-	ns
7	tCHZ	Chip Deselecting to Output in High Z	0	8	0	10	0	10	ns
8	tOHZ	Out Disable to Output in High Z	0	8	0	8	0	8	ns
9	tOH	Output Hold from Address Change	3	-	3	-	3	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	15	-	20	-	25	-	ns
11	tCW	Chip Select to End of Write	12	-	13	-	15	-	ns
12	tAW	Address Valid to End of Write	12	-	13	-	15	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	12	-	13	-	15	-	ns
15	tWR	Write Recovery Time	0	-	0	-	-	-	ns
16	tWHZ	Write to Output in High Z	0	7	0	9	0	10	ns
17	tDW	Data to Write Time Overlap	8	-	9	-	10	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	3	-	3	-	3	-	ns

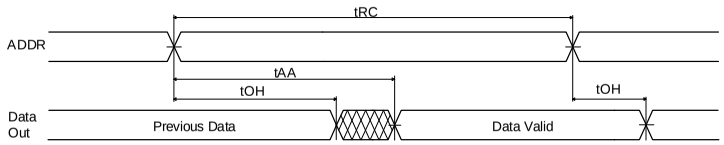
TIMING DIAGRAM

READ CYCLE 1



Note (Read Cycle)
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for read cycle.

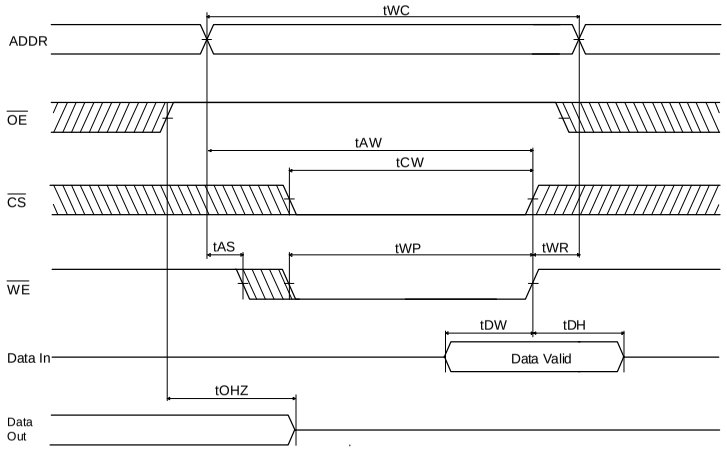
READ CYCLE 2



Note (Read Cycle)
1. /WE is high for read cycle.
2. Device is continuously selected /CS=VIL.
3. /OE=VIL.

HY638256 Series

WRITE CYCLE 1(/OE Low Clocked)



WRITE CYCLE 2(/OE Low Fixed)