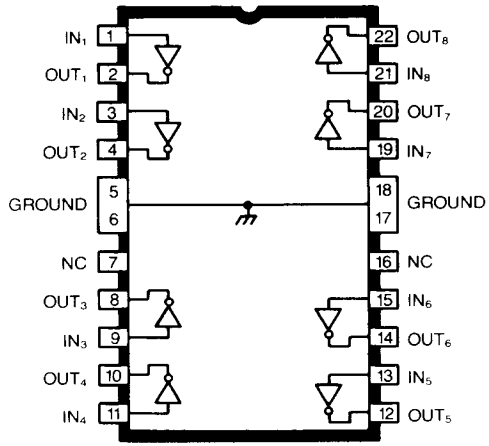
UDN-6540B
8-CHANNEL DMOS HIGH-VOLTAGE DRIVER

FEATURES

- 200 V Outputs
- CMOS, PMOS Compatible
- Internal Gate Limiting Resistors
- Diode Clamped Inputs and Outputs
- Improved Output SOA

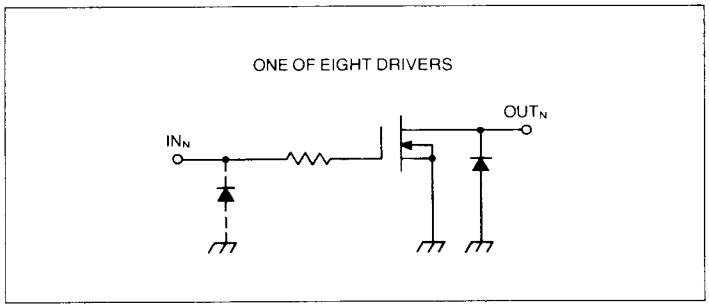


Dwg. No. W-103

The UDN-6540B is an eight-channel high-voltage DMOS driver capable of sinking 200 mA and maintaining an output OFF voltage of 200 V. This device has many possible applications such as driving piezoelectric elements, gas-discharge or electroluminescent displays, and other high-voltage power loads. This device is input compatible with 7-20 V logic such as PMOS, CMOS, and high-voltage open collector TTL.

Because DMOS outputs have output SOA superior to that of conventional bipolar technologies, the UDN-6540B is ideal for inductive load applications. Unlike NPN transistors, DMOS devices can operate safely to their breakdown voltage limit without risk of secondary breakdown (latch-back) or sacrifice of reliability.

The UDN-6540B is furnished in a 22-pin dual in-line package with 0.400" row centers and sink contact tabs. A copper-alloy lead frame provides maximum power dissipation using standard cooling methods. This lead configuration facilitates attachment of external heat-sinks for increased power dissipation with standard IC sockets and printed wiring boards.

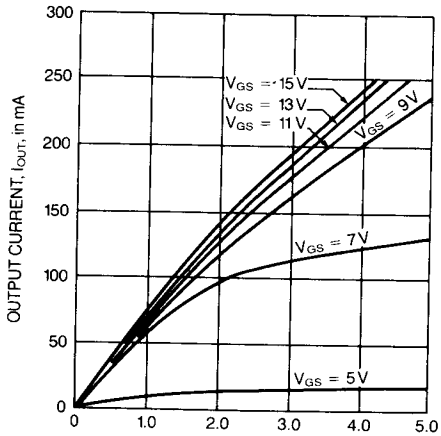


Dwg. No. W-104

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{DS} 200V
Input Voltage, V_{IN} 20V
Output Current, I_{OUT} 250mA
Power Dissipation, P_D . . . . . See Graph
Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range, T_A . . . . −20°C to +85°C

OUTPUT CURRENT AS A FUNCTION OF V_{DS}

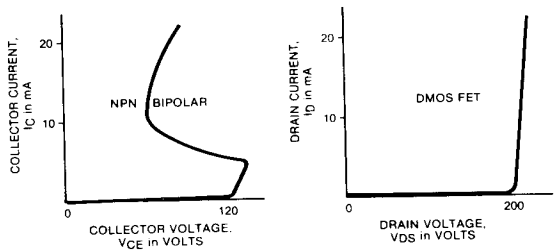


Dwg. No. W-169

ELECTRICAL CHARACTERISTICS at T_A = +25°C

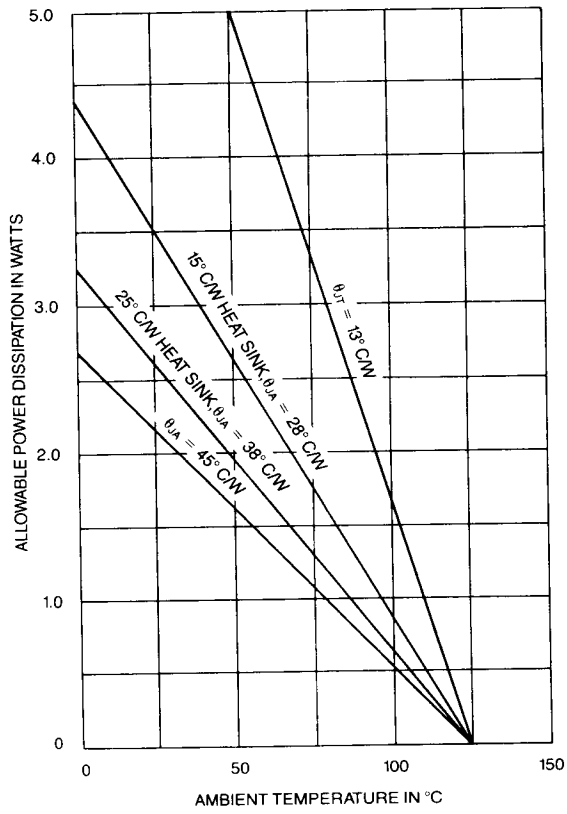
Characteristics	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{DSS}	V_{DS} = 200V, Gate Shorted to Source	—	10	µA
Drain to Source ON Voltage	$V_{DS(ON)}$	V_{GS} = 10V, I_{OUT} = 100mA	—	2.5	V
		V_{GS} = 10V, I_{OUT} = 200mA	—	5.0	V
		V_{GS} = 15V, I_{OUT} = 200mA	—	4.0	V
Input Threshold Voltage	V_{TH}	I_{OUT} = 10mA, V_{DS} = 0.5V	—	7.0	V
		I_{OUT} = 50mA, V_{DS} = 1.0V	—	8.5	V
Turn-On Delay	t_{ON}	0.5E_{IN} to 0.5E_{OUT}, R_L = 1 kΩ, V_{OUT} = 200V	—	0.5	µs
Turn-Off Delay	t_{OFF}	0.5E_{IN} to 0.5E_{OUT}, R_L = 1 kΩ, V_{OUT} = 200V	—	0.5	µs

BREAKDOWN CHARACTERISTICS



Dwg. No. SD-113

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. W-105