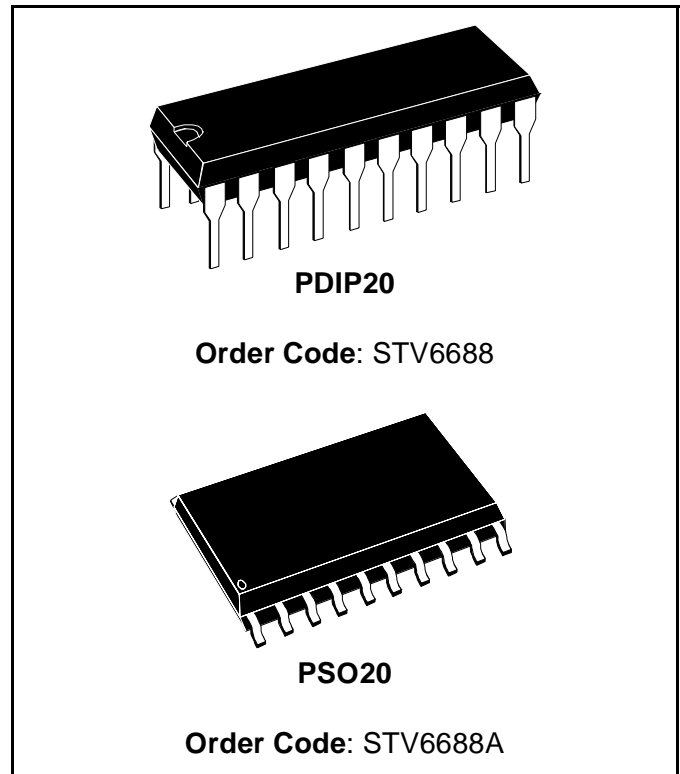


Video Switch Matrix for TV Applications with S Terminal

PRODUCT PREVIEW

Key Features

- I²C Bus Control
- Standby Mode
- 4 Y/CVBS Inputs (one for internal TV signal)
- 4 C Inputs (one for internal TV signal)
- 1 Y/C Adder
- 1 Y/CVBS and 1 C Output, each with 0 dB gain
- 1 CVBS Output with 6 dB gain and 150 Ω Buffer for Monitor
- SYNC Bottom Clamp on all CVBS/Y and Average Bias on C Inputs
- Bandwidth: 15 MHz
- Crosstalk: 50 dB (min.)

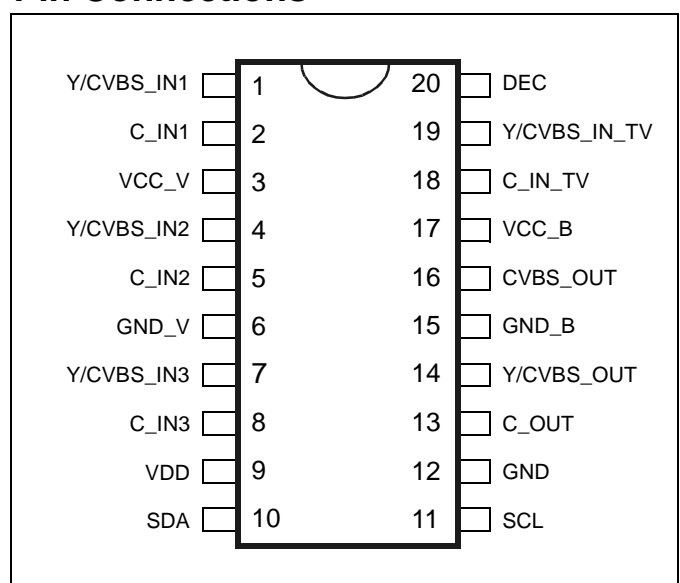


General Description

The STV6688 is a highly-integrated I²C bus-controlled video switch matrix, optimized for use in color TV applications.

It is used to control the switching of 4 video signals. These signals can be in Single Component form (CVBS) or in Two Component form (Y/C). In both cases, the STV6688 microcontroller provides a CVBS signal for an external device (monitor).

Pin Connections

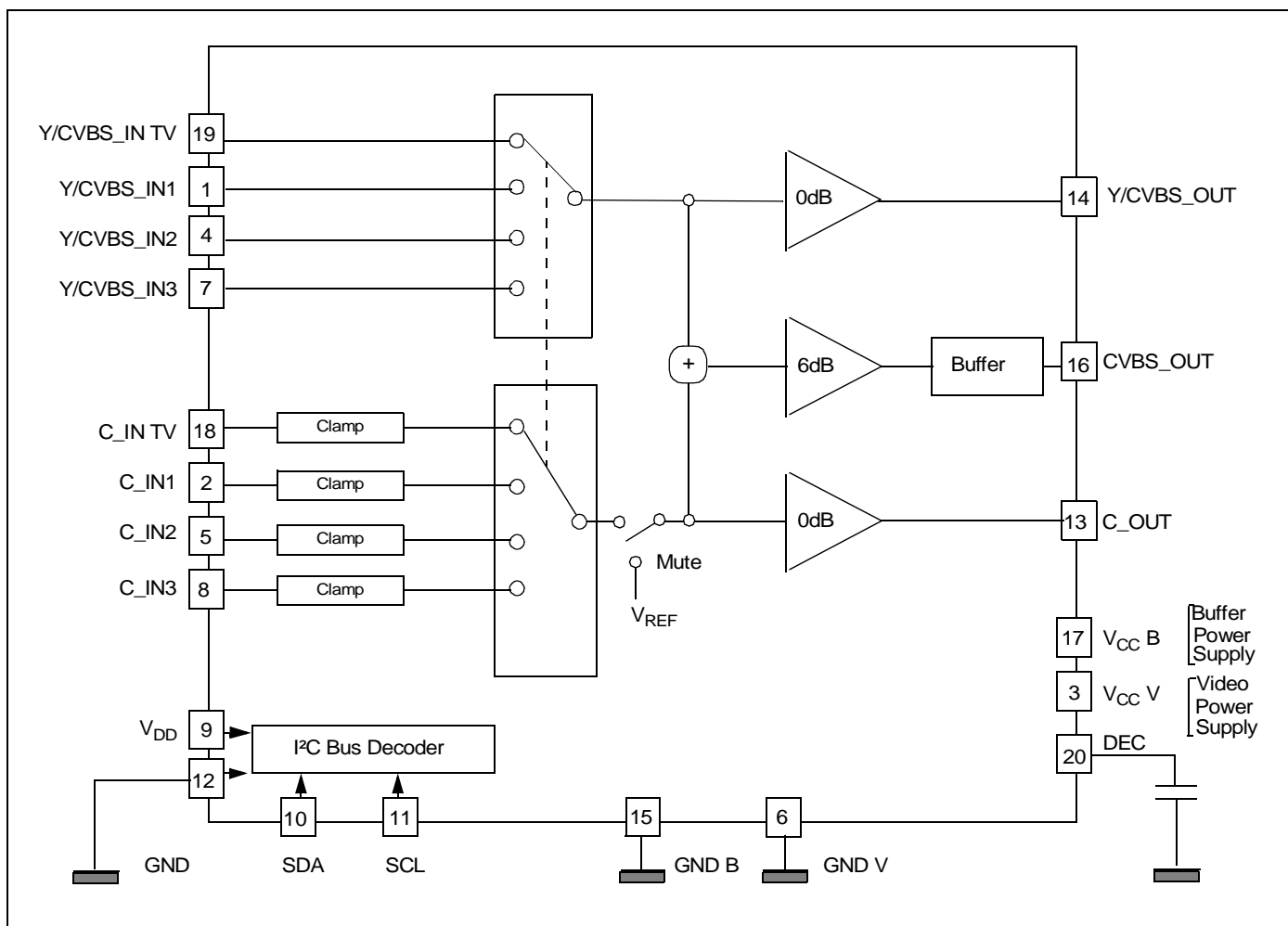


1 Functional Description

Table 1: Pin List

Pin	Symbol	Description	Pin	Symbol	Description
1	Y/CVBS_IN1	Y or CVBS Signal of Ext. Input 1	11	SCL	Serial Clock Line Input
2	C_IN1	C Signal of Ext. Input 1	12	GND	Digital Parts Ground
3	VCC_V	Video Switch Power Supply	13	C_OUT	C Signal Output
4	Y/CVBS_IN2	Y or CVBS Signal of Ext. Input 2	14	Y/CVBS_OUT	Y/CVBS Output
5	C_IN2	C Signal of Ext. Input 2	15	GND_B	Buffer Ground
6	GND_V	Video Switch Ground	16	CVBS_OUT	Y and C Adder Output
7	Y/CVBS_IN3	Y or CVBS Signal of Ext. Input 3	17	VCC B	Buffer Power Supply
8	C_IN3	C Signal of Ext. Input 3	18	C_IN_TV	C Signal of TV Input
9	VDD	Digital Parts Power Supply	19	Y/CVBS_IN_TV	Y or CVBS Signal of TV Input
10	SDA	Serial Data Line Input	20	DEC	Decoupling

Figure 1: STV6688 Block Diagram



2 Electrical Characteristics

$T_{AMB} = 25^{\circ}\text{C}$, $V_{CCV} = V_{CCB} = V_{DD} = 5\text{V}$, $R_{LoadYC} = 4.7\text{ k}\Omega$, $R_{LoadCVBS} = 150\ \Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Digital Supply Voltage		4.5	5	5.5	V
V_{CC}	Video Operating Supply Voltage		4.5	5	5.5	V
V_{CCB}	Buffer Supply Voltage		4.5	5	5.5	V
Active (Channels ON)						
I_{DD}	Digital Supply Current	$V_{DD} = 5\text{ V}$		3		mA
I_{CCV}	Total Video Supply Current (V_{CC}, V_{CCB})	$V_{CC} = 5\text{ V}$, No load $V_{CCV} = V_{CCB} = 5\text{V}$, with loads and signals		13 25		mA
Standby (All Channels OFF)						
I_{DD}	Digital Supply Current	$V_{DD} = 5\text{ V}$		3		mA
I_{CCVstd}	Total Video Supply Current	$V_{CC} = 5\text{ V}$		0.3		mA

2.1 Thermal Data

Symbol	Parameter	Package	Value	Unit
R_{thJA}	Maximum Junction-to-Ambient Thermal Resistance	DIP20 (STV6688)	80	$^{\circ}\text{C}/\text{W}$
		SO20 (STV6688A)	100	$^{\circ}\text{C}/\text{W}$

2.2 Y/CVBS Section

$T_{AMB} = 25^{\circ}\text{C}$, $V_{CCV} = V_{CCB} = V_{DD} = 5\text{V}$, $R_{LoadYC} = 4.7\text{ k}\Omega$, $R_{LoadCVBS} = 150\ \Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DCIN}	DC Input Level	Bottom Sync pulse		2		V
I_{CLAMP}	Clamping Current	at $V_{DCIN} - 400\text{ mV}$	1	2		mA
I_{LEAK}	Input Leakage Current	$V_{IN} = V_{DCIN} + 1\text{ V}$		1	10	μA
C_{IN}	Input Capacitance			2		pF
V_{IN}	Max Input Signal	$V_{CC} = 5\text{ V}$			1.5	V_{PP}
DYNY	Dynamic Y/CVBS Output Signal	$V_{CC} = 5\text{ V}$			1.5	V_{PP}
DYNCVBS	Dynamic CVBS Output Signal	$V_{CC} = 5\text{ V}$			3	V_{PP}
BW	Bandwidth at -3 dB Y/CVBS Y/C Mixer (on CVBS_OUT)	$V_{IN} = 1\text{ V}_{PP}$ $V_{IN} = 1\text{ V}_{PP}$	12 8	15 10		MHz

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Flatness	Spread of Gain in Video Band (15 kHz-5 MHz) Y/CVBS Y/C Mixer (on CVBS_OUT)	$V_{IN} = 1 V_{PP}$ $V_{IN} = 1 V_{PP}$		± 0.2 ± 0.5	± 0.5 ± 1.0	dB
CTi	Crosstalk Isolation between Y/CVBS Input Channels	$V_{IN} = 1 V_{PP}$ at $f = 4.43$ MHz, on one point.	55	60		dB
CTo	Crosstalk Isolation of Y/CVBS from C Channels	$V_{IN} = 1 V_{PP}$ at $f = 4.43$ MHz, on one point.	50	55		dB
GYCVBS	Gain at Y/CVBS out @1 MHz	$V_{IN} = 1 V_{PP}$	-0.5	0	+0.5	dB
GCVBS	Gain at CVBS out @1 MHz	$V_{IN} = 1 V_{PP}$	5.5	6	6.5	dB
R _{OUTY}	Y/CVBS Output Resistance			2.5	5.0	Ω
R _{OUTCVBS}	CVBS Output Resistance			1	5	Ω
G _{YCVBSM}	Gain matching between Y, CVBS inputs	$V_{IN} = 1 V_{PP}$	-0.5	0	+0.5	dB
DC _{OUTCVBS}	DC CVBS Output voltage	Bottom sync pulse		0.8		V
DC _{OUTY}	DC Y Output voltage	Bottom sync pulse for Y		1.3		V
DPHI	Differential Phase	$V_{IN} = 1 V_{PP}$ at $f = 4.43$ MHz		1	3	deg
DG	Differential Gain	$V_{IN} = 1 V_{PP}$ at $f = 4.43$ MHz		1	5	%
LNL	Luminance non-linearity			0.6	3	%
VSN	Video S/N ratio	Refer to Note 1	65			dB

Note: 1 $S/N = 20 \log (V_{OUT} \text{ Black to White} = 0.7 V_{PP} / V_{Noise} (mV_{RMS}) \text{ weighted CCIR567})$.

2.3 Chroma Section

$T_{AMB} = 25^{\circ}\text{C}$, $V_{CCV} = V_{CCB} = V_{DD} = 5\text{V}$, $R_{LoadYC} = 4.7 \text{ k}\Omega$, $R_{LoadCVBS} = 150 \Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DCIN}	DC Input Level			3		V
R _{IN}	Input Resistance		30	50		k Ω
C _{IN}	Input Capacitance			2		pF
V _{IN}	Max Input Signal				1.5	V _{PP}
DYN	Dynamic Output Signal				1.5	V _{PP}
CBW	Chroma Bandwidth	$C_{IN} = 1 V_{PP}$	10	12		MHz
CTi	Crosstalk Isolation between C Input Channels	$C_{IN} = 0.5 V_{PP}$ at $f = 4.43$ MHz, on one point.	55	60		dB
CTo	Crosstalk Isolation of C from Y Channels	$V_{IN} = 1 V_{PP}$ at $f = 4.43$ MHz, on one point.	50	55		dB
R _{OUT}	Output Resistance			2.5	5.0	Ω
G _{OUTC}	Gain at C_OUT @4.43 MHz	$V_{IN} = 1 V_{PP}$	-0.5	0	+0.5	dB
DC _{OUTC}	DC Output voltage			2.2		V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{CM}	Gain matching between C inputs	$V_{IN} = 1 V_{PP}$	-0.5	0	+0.5	dB
CToYdel	Chroma to Luma delay, Y/C source	V_{PP} @4.43 MHz		5	10	ns

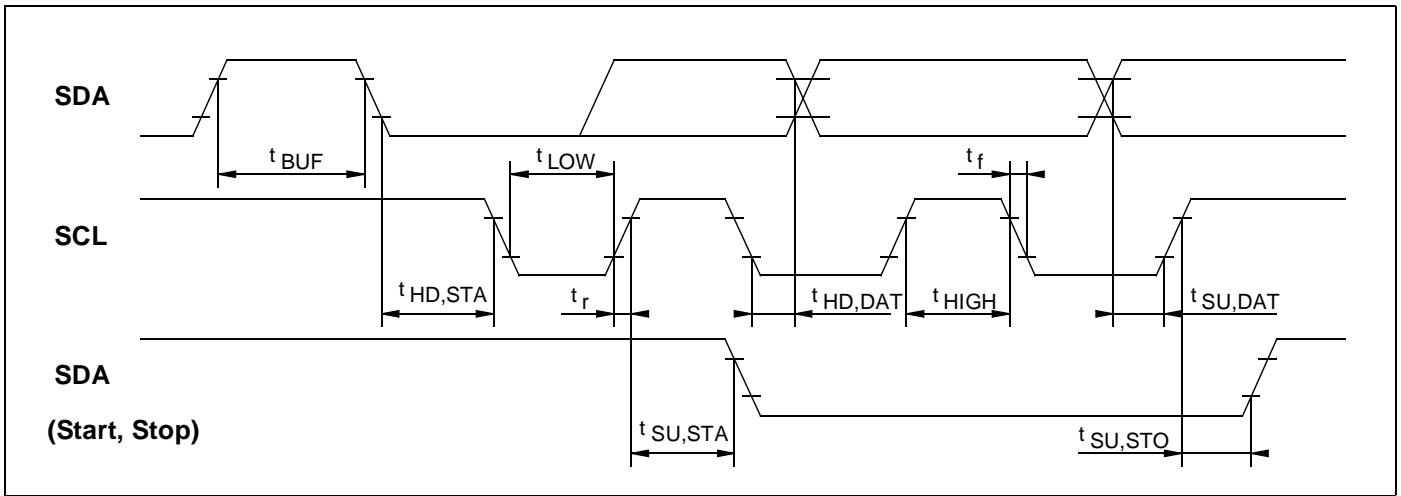
2.4 I²C Bus Characteristics

$T_{AMB} = 25^{\circ}\text{C}$, $V_{CCV} = V_{CCB} = V_{DD} = 5\text{V}$, $R_{LoadYC} = 4.7\text{ k}\Omega$, $R_{LoadCVBS} = 150\ \Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Address Selection Input						
ADDsel_L	Address Selection Low Level			0	0.2	V
ADDsel_H	Address Selection High Level		2.5		V_{DD}	V
ILEAK	Leakage Current				10	μA
SCL						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		3		5.5	V
I_{LI}	Input Leakage Current	$V_{IN} = 0\text{ to }5.5\text{ V}$	-10	0	10	μA
SDA						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		3		5.5	V
I_{LI}	Input Leakage Current	$V_{IN} = 0\text{ to }5.5\text{ V}$	-10	0	10	μA
C_I	Input Capacitance				10	pF
t_R	Input Rise Time	1.5 V to 3 V			1	μs
t_F	Input Fall Time	3 V to 1.5 V			300	ns
V_{OL}	Low Level Output Voltage	$I_{OL} = 3\text{ mA}$			0.4	V
t_F	Output Fall Time	3 V to 1.5 V			250	ns
C_L	Load Capacitance				400	pF
Timing (Clock Frequency = 100 kHz, see Note 2)						
t_{LOW}	Clock Low Period		4.7			μs
t_{HIGH}	Clock High Period		4			μs
$t_{SU,DAT}$	Data Setup Time		250			ns
$t_{HD,DAT}$	Data Hold Time		0		340	ns
$t_{SU,STO}$	Setup Time from Clock High to Stop		4			μs
t_{BUF}	Start Setup Time following a Stop		4.7			μs
$t_{HD,STA}$	Start Hold Time		4			μs
$t_{SU,STA}$	Start Setup Time following Clock Low to High Transition		4.7			μs

Note: 2 The device can also operate at 400 kHz.

Figure 2: I²C Bus Timings



2.5 I²C Bus Selection

Data transfers follow the usual I²C format: after the Start condition (S), a 7-bit slave address is sent, followed by an 8-bit word which is a data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register.

The I²C Bus Decoder of the microcontroller provides the Automatic Incrementation mode in Write mode.

String Format: Write Only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	SLAVE ADDRESS: 94h	A	00h	A	DATA	A	P
---	--------------------	---	-----	---	------	---	---

Input Signals Summary: (Write Mode)

Reg.Addr. (Hex)	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
	General Stand-by	Buffer Stand-by	Always set to 1					Switch Control

Input Signal: (Write Mode) Data Byte

Reg. Addr.	Description	Bits	Data								Comments
			D7	D6	D5	D4	D3	D2	D1	D0	
0x00	General Stand-by	1	0	X	1	X	X	X	X	X	All disabled
			1	X	1	X	X	X	X	X	All active
0x00	Buffer Stand-by	1	X	0	1	X	X	X	X	X	Buffer disabled
			X	1	1	X	X	X	X	X	Buffer active
0x00	Y/CVBS and C Selection	2	X	X	1	X	X	X	0	0	INT TV
			X	X	1	X	X	X	0	1	IN1
			X	X	1	X	X	X	1	0	IN2
			X	X	1	X	X	X	1	1	IN3

3 Input/Output Groups

Figure 3: Bottom Clamped Video Inputs (Pins 1, 4, 7 and 19)

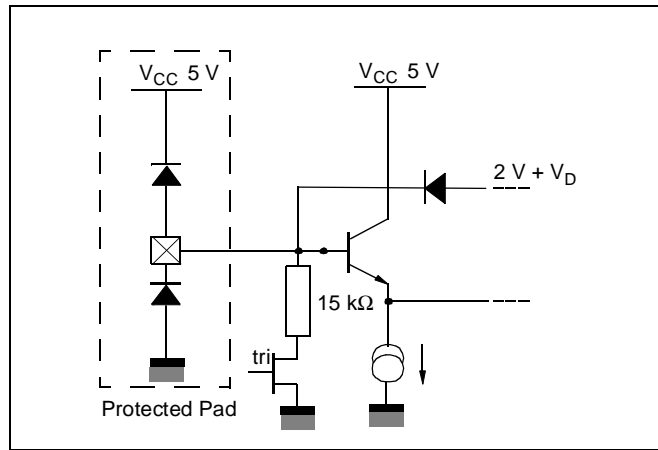


Figure 4: Average Clamped Video Inputs (Pins 2, 5, 8 and 18)

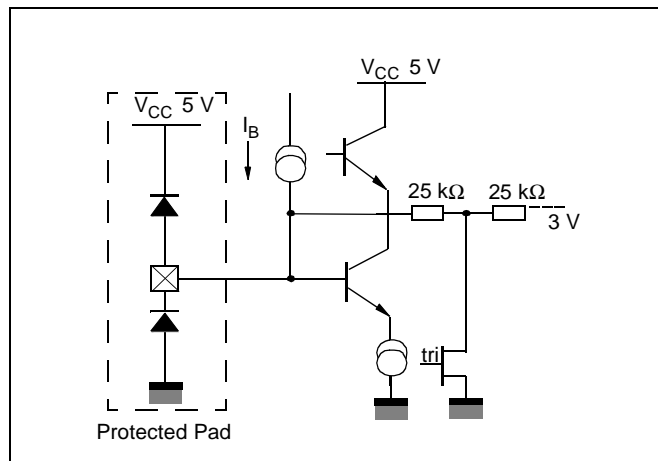


Figure 5: Video Outputs (Pins 13, 14 and 16)

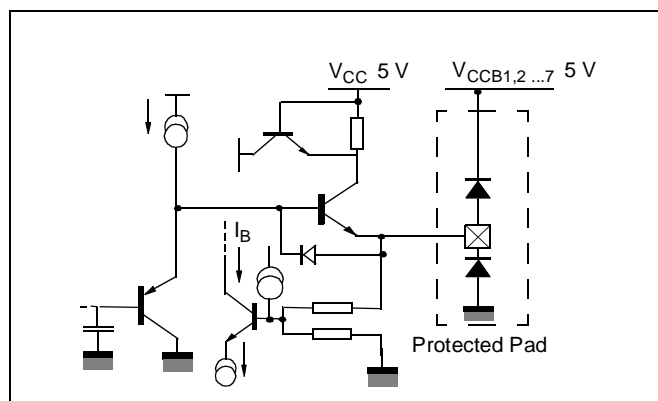
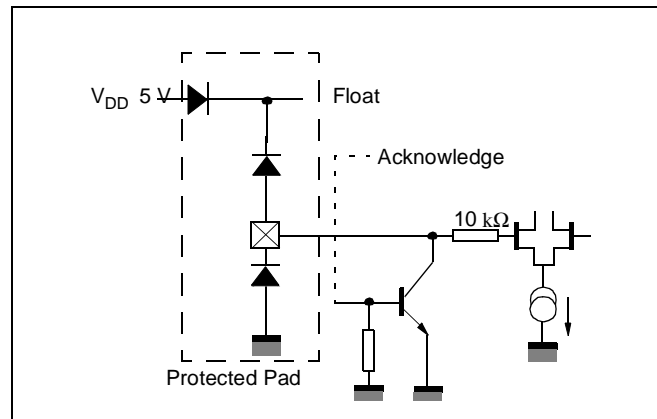
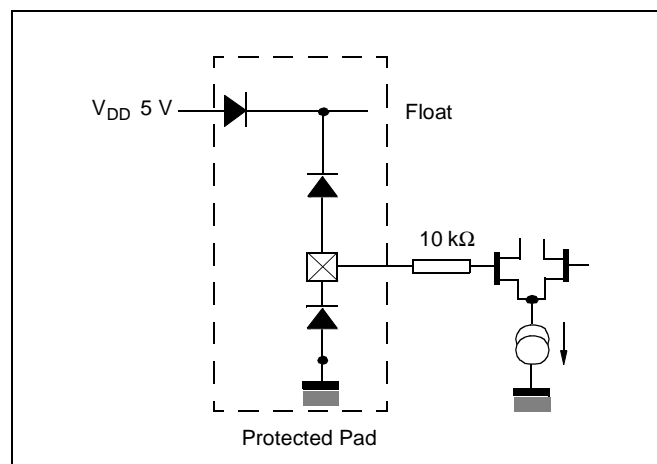
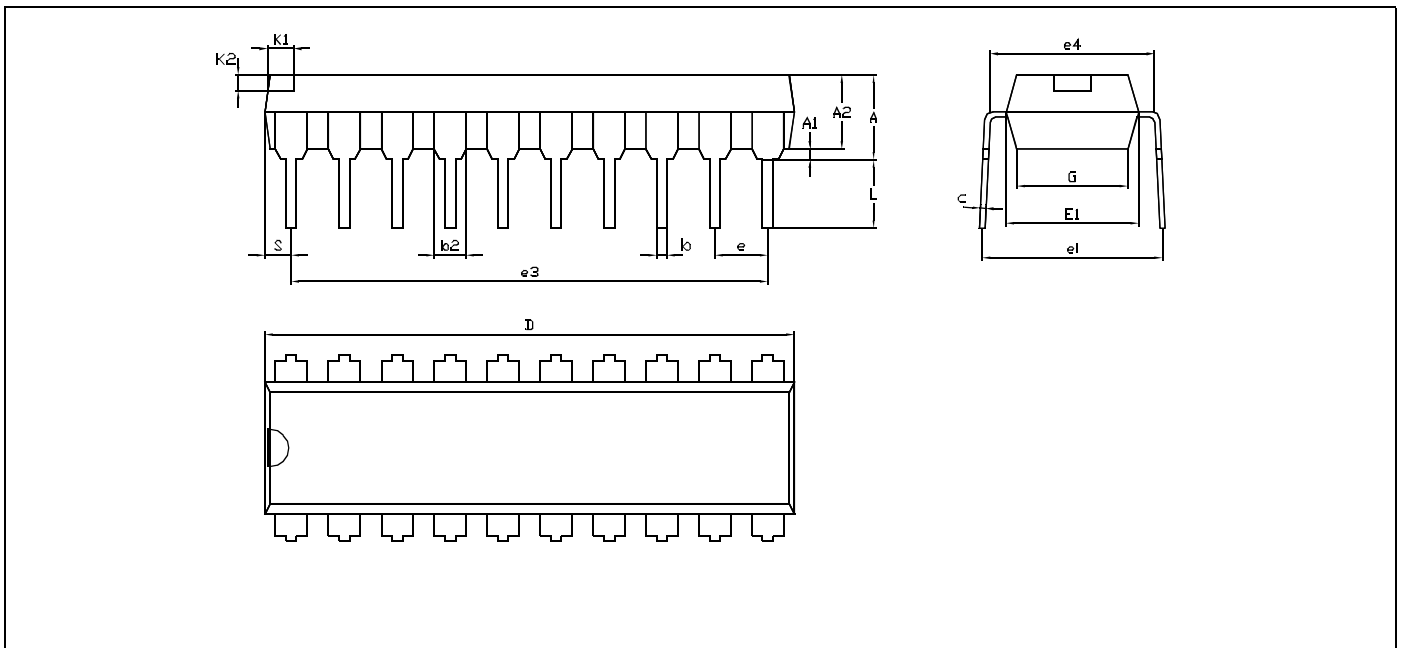


Figure 6: I²C Bus SDA (Pin 10)Figure 7: I²C Bus SCL (Pin 11)

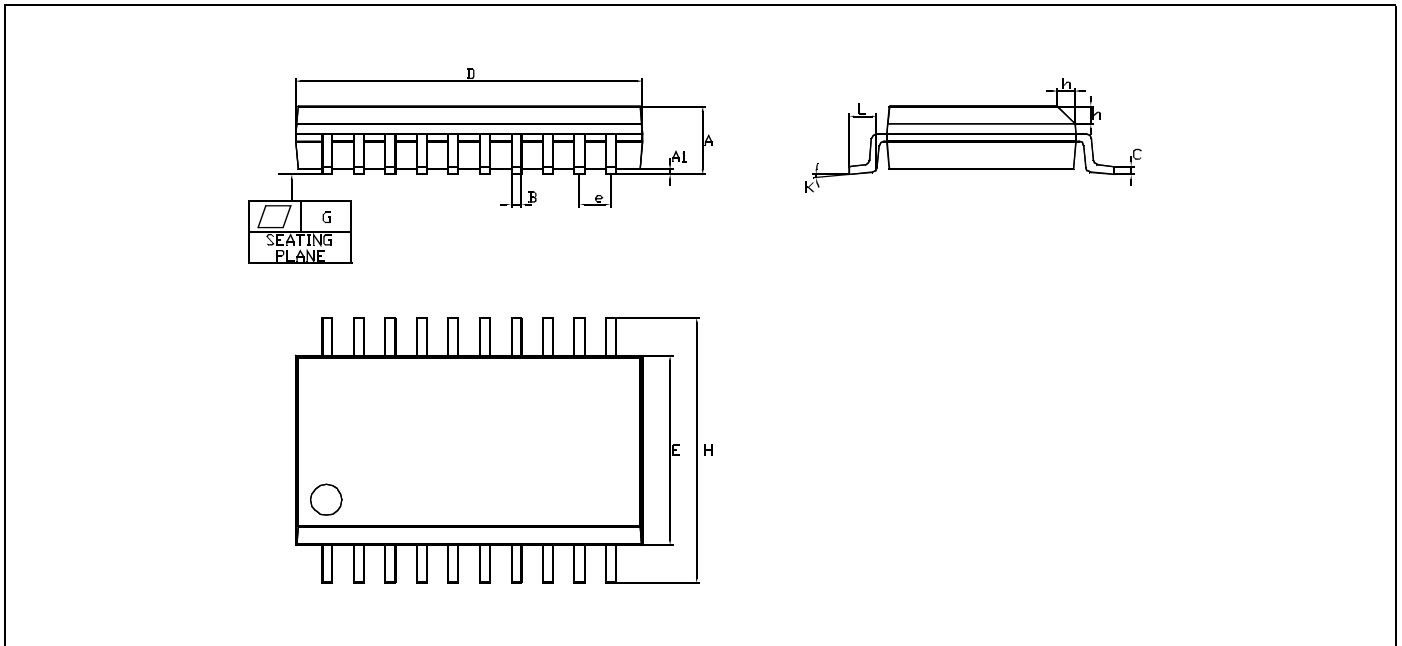
4 Package Mechanical Data

Figure 8: 20-Pin Plastic Single in Line Package (PDIP20)



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	24.89		26.92	0.980		1.060
e		2.54			0.100	
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150

Figure 9: 20-Pin Plastic Small Outline Package, 300-mil Width (PSO20)



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.0926		0.1043
A1	0.10			0.0040		
B	0.33		0.51	0.0130		0.0200
C			0.32			0.0125
D	4.98		13.00	0.1961		0.5118
E	7.40		7.60	0.2914		0.2992
e		1.27			0.050	
H	10.01		10.64	0.394		0.419
h	0.25		0.74	0.010		0.029
K	0°		8°	0°		8°
L	0.41		1.27	0.016		0.050
G			0.10			0.004
	Number of Pins					
N	20					

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