EG&G RETICON

RA0128NIU
128 x 128 PtSi Focal Plane Array

T-41-55

Introduction

Reticon has successfully combined the advantages of thin film PtSi SBD technology with our standard photodiode arrays to produce a 128 x 128 monolithic area array which is sensitive in the mid-infrared (MIR) spectral region. The platinum silicide Schottky barrier diode (PtSi SBD) is the most practical and cost effective technology for providing high resolution infrared staring focal plane arrays (FPA) for both industrial and military applications.

The 128 x 128 PtSi FPA is backside illuminated and is sensitive in the 1 to 5.5 μm spectral range. Visible and near infrared photons are absorbed in the silicon before they reach the photo-detector area, and long-wavelength IR (LWIR) photons create holes with insufficient energy to jump the metal-semiconductor (Schottky) Barrier. With backside illumination, the array is sensitive to wavelengths from 1 to 5.5 μm without the need for external filters. Applications include noncontact temperature monitoring for industrial and medical uses, missile seekers, surveillance, tracking, process control, and nondestructive testing.

Key Features

- High resolution: 128 x 128 elements
- High fill factor: 59% with a 60 μm x 60 μm pixel size
- Two horizontal readout registers for high speed imaging
- High frame rate: greater than 450 frames/sec
- Spectral response: 1 to 5.5 μm
- Excellent element-to-element uniformity: 0.5% rms
- High video sampling rates: up to 10 MHz pixel rate
- On-chip pre-amplifer and reset structure
- High electron sensitivity: 0.7 μV/e^-
- Wide dynamic range ≥1000:1 rms
- Backside illumination provides inherent (visible and near infrared) filtering
- 28-pin dual-inline ceramic package

Description

The 128 x 128 PtSi FPA has 16,348 pixels arranged in a matrix of 128 rows by 128 columns. Each pixel has a fill factor of 59% and is 60 μm x 60 μm. The chip dimensions are 433 mil x 453 mil of which 302 mil x 302 mil is the sensing area. This device is provided in a standard 28-pin dual-inline ceramic package, (see Figure 7), which accommodates backside illumination of the chip and simplifies cryogenic cooling. Figure 1 shows the pinout configuration and Table 1 shows the pin description of the 128 x 128 PtSi FPA.

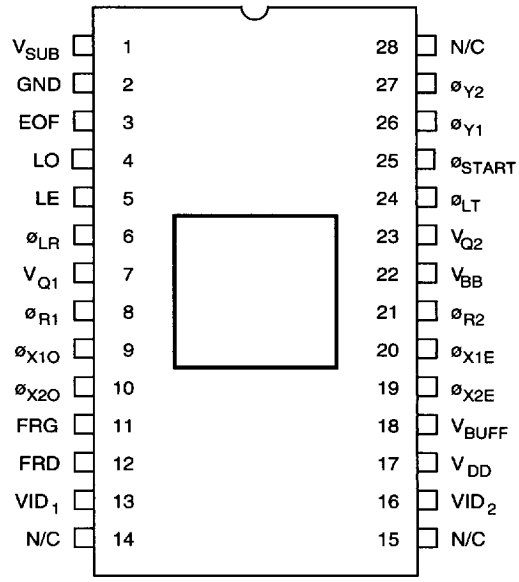

Figure 1. Pinout Configuration

The array can be scanned with pixel readout rates up to 10 MHz to yield frame rates greater than 450 frames/sec. Each line of photodiodes is parallel loaded into two high speed bucket-brigade device (BBD) analog shift registers and then sequentially shifted out. The outputs of the two BBDs can then be easily multiplexed externally to reconstruct the line information. The entire frame of 128 lines may be sequentially accessed, or just the odd or even lines may be read out. If the output of one BBD is used and just the even or odd lines are accessed, a frame will contain every other pixel in 64 lines for a 64 x 64 array. The time between the readout of a pixel, one frame period, is the integration time.

The devices are fabricated using an advanced double poly NMOS process. Each device consists of several functional elements to control the operation of the device, as shown in Figure 2. The functional elements are described in the following paragraphs.

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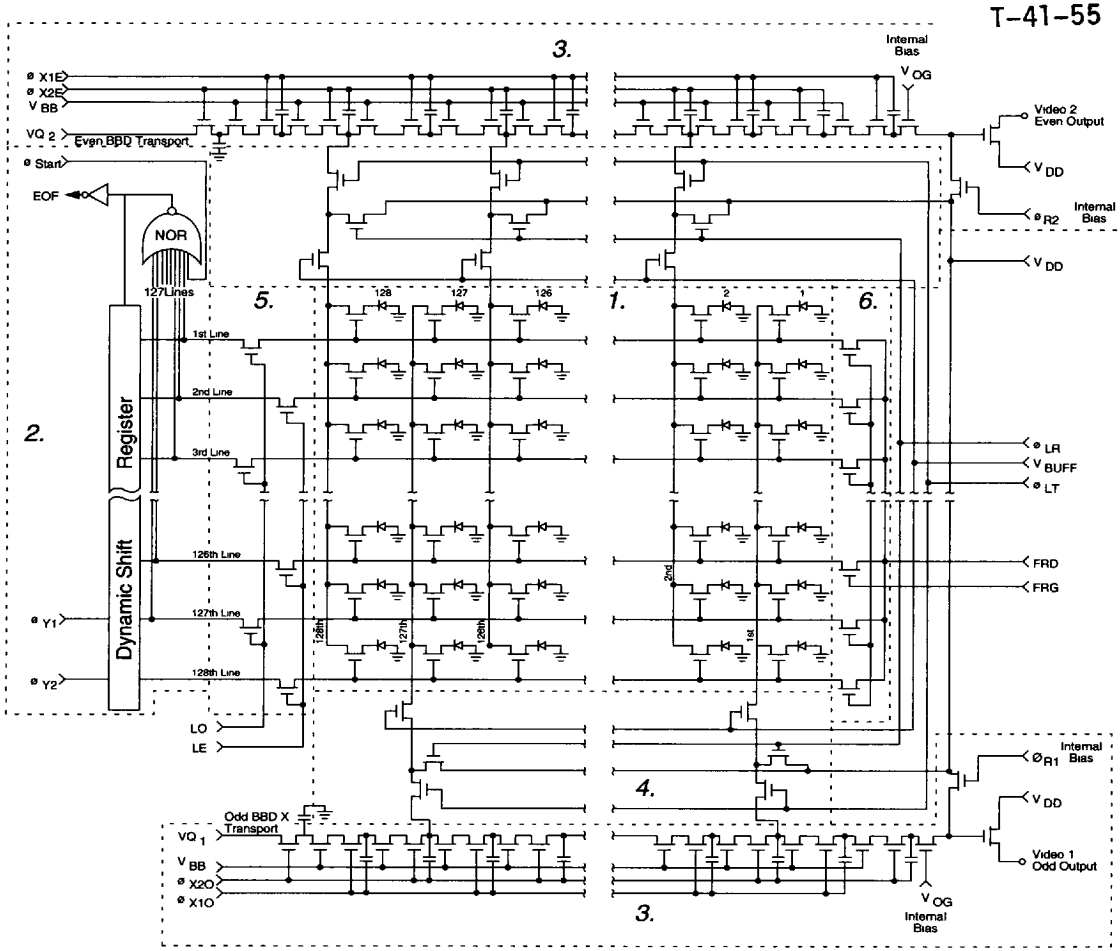

Figure 2. Schematic Diagram RA0128NIU

Photodiode Array

The first element consists of a 128 x 128 Schottky barrier photodiode array, schematically indicated by the columns and rows (lines) of individual photodiodes. Each diode in a column is connected through a multiplex switch to a column video line, which is common to all diodes in that column. The gates of all the multiplex switches in a row (line) are connected together, so that when a row of multiplex switches is turned on, the signal in a row of diodes is transferred simultaneously to the 128 column video lines. When a diode is selected by the multiplex switch, the potential of the diode will be reset to a value of (V_{GM} - V_{TM}), where V_{GM} and V_{TM} represent the clock high voltage and threshold voltage of the multiplex switch, respectively. The signal charge removed from the selected diode will be transferred through the column video line into the BBD for readout. After the multiplex switch is turned off, the diode starts to integrate the photon-generated charge. The total integration time of each diode is the time between two consecutive readouts of the same diode.

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Dynamic Shift Register

The second element consists of a two-phase (2ø) dynamic shift register. The shift register turns on each row (line) of multiplex switches in sequence, allowing the photodiode charge to transfer through each column video line into the appropriate BBD. The dynamic shift register is driven by two-phase clocks denoted by $ø_{Y1}$ and $ø_{Y2}$ in Figure 2. Odd lines are accessed while $ø_{Y1}$ clocks are high, even lines while $ø_{Y2}$ is high. The dynamic shift register can be self-starting if fast consecutive frames are desired, or it can be controlled by an external start pulse ($ø_{Start}$). These functions are performed by a "NOR" circuit. Tied to each output of the shift register (except for the 128th position) are inputs to a NOR gate. When there is an output from any of the 127 output positions, the NOR gate keeps the shift register from restarting. Once the bit occupies the last position, the NOR gate's output goes high and the shift register starts again with the rising edge of $ø_{Y1}$. The $ø_{Start}$ is also connected to the NOR gate. It can be used to inhibit the register from starting by pulling $ø_{Start}$ to V_{DD}. The shift register will not start to access lines until both $ø_{Start}$ and the outputs from lines 1 - 127 are low.

The NOR gate output is connected to an external pin, EOF (End of Frame), through an open drain inverter. This output is normally tied to V_{DD} through a 3KΩ resistor. When there is a bit in any row except the last, or if $ø_{Start}$ is active, EOF will remain high. It goes immediately low on the rising edge of $ø_{Y2}$ if $ø_{Start}$ is low, and none of the rows 1 - 127 are active.

Bucket-Brigade Device Analog Shift Register

Two bucket-brigade analog shift registers accept the signal from the column video lines and shift it out sequentially to two output amplifiers. Each BBD is driven by a two-phase clock, denoted by $ø_{X1}$ and $ø_{X2}$ in Figure 2. A "fat zero" input port is provided to improve the transfer efficiency of the register. The outputs from both BBD registers are multiplexed off-chip to obtain one line of combined video information.

As shown in Figure 2, there are several other terminals associated with the two BBD registers. V_{BB} is the tetrode-gate bias that is biased at a DC voltage a few volts below the $ø_{X1}$ and $ø_{X2}$ high level. V_{Q1} and V_{Q2} are the input bias for the "fat zero" input port. These inputs control the bias level in the dark. Normally, these terminals are biased to approximately 10V; however, when the odd and even videos are summed together, either input bias voltage may be used to adjust the corresponding dark-level output to remove the odd-and-even pattern. Figure 4 shows the relationship between the output dark signal level and V_{Q1}, V_{Q2} bias voltage. The shaded area represents the optimum bias range. $ø_{R1}$ and $ø_{R2}$ are the reset clocks for the output amplifiers, which are shown in Figure 2 at the outputs of both bucket brigades. On the even side, the signal appears at the gate of the output amplifiers when $ø_{X1}$ drops to a low potential. While $ø_{X1}$ is high and before the next sample appears, this node is cleared by charging it to the reset voltage, V_{DD}. This

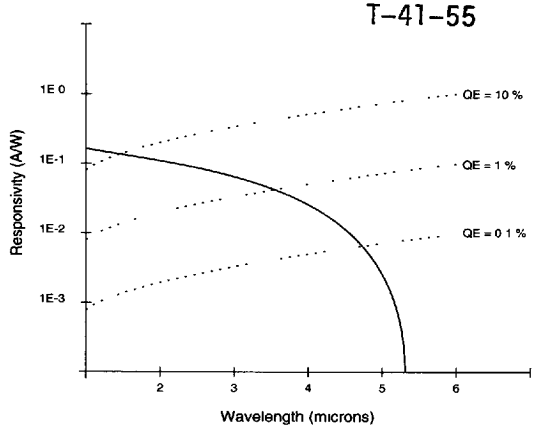

Figure 3. Spectral Response

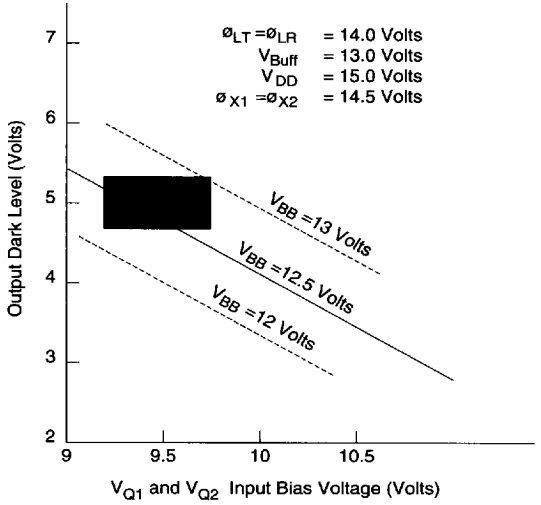

Figure 4. Operation Range of V_{Q1}, V_{Q2} Bias

can be easily done if $ø_{R2}$ is clocked synchronously with $ø_{X1}$. The complementary situation applies to the odd video output, with signal appearing while $ø_{X2}$ is low, and reset while $ø_{X2}$ is high. Normally, the synchronous relationship is obtained by direct connection of $ø_{X1}$ to $ø_{R2}$, and direct connection of $ø_{X2}$ to $ø_{R1}$.

VID_1 and VID_2 are the respective odd and even video output terminals. The video output is that of a source follower. Normally, the output of each source follower is terminated by a 3KΩ resistor to ground. This configuration provides the proper bias current for the source follower.

Line Transfer ($ø_{LT}$), Line Reset ($ø_{LR}$) and Buffer Gate (V_{BUFF})

The fourth functional element consists of a video line reset switch, $ø_{LR}$; a line transfer switch, $ø_{LT}$; and a buffer gate, V_{BUFF}. The line reset switch, $ø_{LR}$, provides a reference bias for all the video lines while all the sensor diodes are integrating signal charges. All the charges collected from stray capacitances along the video lines and all the excess signal charges leaked from the sensor diodes are drained into the sink voltage, V_{DD}, through operation of the $ø_{LR}$ gate. In this way, $ø_{LR}$ functions as an antiblooming and anticrosstalk gate. Prior to the moment when the dynamic shift register is to select a row of diodes, the $ø_{LR}$ gate is turned off and the transfer gate ($ø_{LT}$) is turned on. This prepares the video lines to accept charge from the next row of photodiodes to be transferred into the BBDs.

The bias applied to the $ø_{LR}$ switch should be lower than that of $ø_{LT}$. This will prevent possible loss of signal charge through the $ø_{LR}$ switch as a result of threshold voltage mismatch between the $ø_{LR}$ and $ø_{LT}$ transistors. The effect of different gate potentials on $ø_{LR}$ and $ø_{LT}$ results in adding a fixed amount of charge Qf into the video signal where $Q_f = (\Delta V_G + \Delta V_T)C_V$. These quantities ΔV_G and ΔV_T are the gate potential and threshold voltage differences of the $ø_{LR}$ and $ø_{LT}$ gates, respectively, and C_V is the capacitance of the video line.

To minimize Q_f, a buffer gate V_{BUFF} is introduced in front of the $ø_{LR}$ and $ø_{LT}$ switches. This buffer gate is biased at a DC potential below the $ø_{LR}$ and $ø_{LT}$ "high" potential. The function of this buffer gate is to isolate the video line capacitance C_V from the effect of ΔV_G and ΔV_T. With the introduction of this buffer gate, Q_f becomes $(\Delta V_G + \Delta V_T)C_J$, where C_J is the junction capacitance of the n^+ diffusion between $ø_{LR}$ and $ø_{LT}$ switches. The capacitance C_J is much smaller than C_V and results in great reduction of Q_f. Normally $ø_{LR}$ is clocked synchronously with $ø_{X2}$. However, to avoid crosstalk and permit adjustment for optimum blooming control, a separate driver is used for $ø_{LR}$.

Field Select Switches LO and LE

The fifth functional element consists of the field select switches LO and LE. As evident from Figure 2, the LO input terminal controls the gates that switch all of the odd-numbered outputs from the dynamic shift register; the LE terminal controls the gates that switch the even numbered outputs. These dynamic shift register outputs in turn control the row selection. When the LO line is held at V_{DD}, the odd rows of diodes may be selected by the dynamic shift register, and when the LE line is held at V_{DD}, the even rows of diodes may be selected. The LO and LE gates are turned on by applying a high (V_{DD}) potential and are turned off by applying a low (0V) potential. For sequential scan of all 128 lines, both LE and LO are held at V_{DD}.

Frame Reset Gate (FRG) and Frame Reset Drain (FRD)

The sixth element consists of the frame reset gate FRG and reset drain FRD. These switches provide an access to the multiplex switches of all the diodes in the matrix and allows the entire frame to be reset. When the frame reset control is not being used it is held low. However, when a particular exposure is desired, this control may be used to clear the diodes by taking the FRG terminal to V_{DD}. When using the frame reset, a shutter or pulsed-light input should be used to ensure the same exposure for all the photodiodes.

There are two inputs for controlling the frame reset operation, the frame reset gate, FRG, and frame reset drain, FRD. In addition, LE and LO must be pulsed off during the reset operation. The timing sequence for this operation is shown in Figure 6. The longest of the control pulses are LE and LO. They should be held negative 200 nanoseconds longer than the frame reset gate with pulse width overlap as seen in Figure 6. The FRD can be continuously active, but within and before the trailing edge of FRG. FRD must be pulled to ground to allow the vertical shift register's multiplexing line to discharge. This is done to ensure that the multiplexing switches are off.

Device Operation

Figure 5 shows the timing diagram for the device when operated in the noninterlaced and continuous mode of operation. It requires two sets of complementary clocks, $ø_{Y1}$ and $ø_{Y2}$, to drive the dynamic shift register and $ø_{X1}$ and $ø_{X2}$ to drive the two BBD registers. It also requires a $ø_{LT}$ clock to control the charge transfer from the column video lines into the BBDs. The line reset clock, $ø_{LR}$, is for blooming control and has the same timing as $ø_{X1}$. The reset gates $ø_{R1}$ and $ø_{R2}$ for the

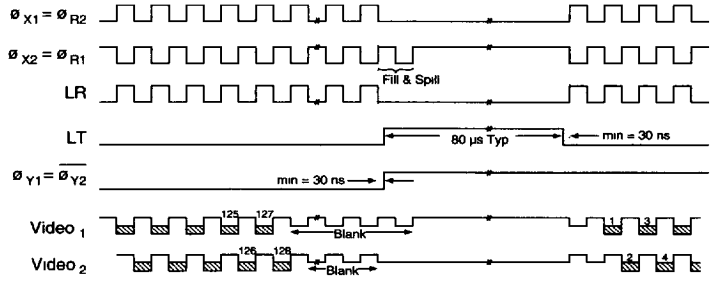

Figure 5. Timing Diagram for RA0128NIU Noninterlaced Continuous Operation

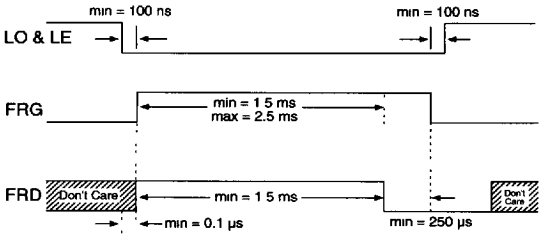

Figure 6. Timing Sequence for Frame Reset

output amplifiers are directly tied to ϕ_{X2} and ϕ_{X1}, respectively. The timing relations and rise and fall times of the various clocks are summarized in Table 3.

Before a new row of diodes is selected by the dynamic shift register, which occurs when ϕ_{Y1} and ϕ_{Y2} changes states, the line reset ϕ_{LR} should be turned off to prevent signal charge from being drained into V_{DD}. A minimum pulse width of ϕ_{LT} is also required to accommodate complete charge transfer from the video line into the BBD register. During the time when the signal is being transferred into the BBD register, the $\phi_{X1,2}$ clocks driving the register must stop with the clocks at high potential on the buckets receiving charge from video line. This will cause a deep potential well for the signal charge to flow into. The buckets receiving charge for both the odd and even transport registers are driven by ϕ_{X2} and the charge transfer takes place simultaneously for both registers during the time ϕ_{X2} is held high. Note that there is an extra clock of ϕ_{X2} with the ϕ_{LT} pulse. The function of this extra clock is to dump the "fat zero" charge of the BBD register into the video lines. This "fill and spill" action significantly improves the transfer efficiency of the signal charge from the video lines into the BBD register.

The ϕ_{LT} clock is then shut off before the BBD register shifts the signal charge to the output amplifiers. During readout, the odd BBD register produces the first pixel. It reads out on the second low-going ϕ_{X2} clock after the transfer period. The second pixel is produced by the even BBD register. Since this even pixel must transfer through an extra half-stage, which is controlled by ϕ_{X1}, it is produced when ϕ_{X1} goes low. This provides an easily multiplexed signal by means of a simple external adder-amplifer.

Specifications

Table 4 shows the operating biases and clock amplitudes in accordance with the timing diagram of Figure 5. With the exception of the supply inputs, such as V_{DD}, the input impedance to input terminals is essentially capacitive. The capacitances are listed in Table 2.

Optical to Electrical Performance

Table 5 lists a summary of optical characteristics, and the spectral response is shown in Figure 3.

Evaluation Detector Head

A complete LN2 cooled detector head useful for evaluating the performance and operating characteristics of the RA0128NIU is available from Reticon. The head consists of a LN2 dewar with 4 hour hold time, complete drive and video circuitry, and a 100 mm F1.8 silicon lens. The output at the RH0128NI detector head is RS170 compatible video which can be displayed on any standard TV monitor. Contact your local sales office for more information on the RH0128NI detector head.

Table 1. Pin Description

Pin Number	Pin Name	Pin Definition
1	V_{Sub}	Substrate voltage
2	GND	Ground
3	EOF	End of frame
4	LO	Odd line control
5	LE	Even line control
6	ϕ_{LR}	Video line reset switch
7	V_{Q1}	Odd analog shift register input bias
8	ϕ_{R1}	Reset gate clock for the odd reset switch
9	ϕ_{X1O}	Phase 1 clock to the Odd BBD register
10	ϕ_{X2O}	Phase 2 clock to the Odd BBD register
11	FRG	Frame reset gate
12	FRD	Frame reset drain
13	VID_1	Odd video output
14	NC	No connection
15	NC	No connection
16	VID_2	Even video output
17	V_{DD}	Power supply voltage
18	V_{BUFF}	Buffer gate switch bias
19	ϕ_{X2E}	Phase 2 clock to even BBD register
20	ϕ_{X1E}	Phase 1 clock to even BBD register
21	ϕ_{R2}	Reset gate clock of the even reset transistor
22	V_{BB}	Tetrode-gate bias
23	V_{Q2}	Input bias for the even analog shift register
24	ϕ_{LT}	Line transfer switch
25	ϕ_{Start}	Start pulse for Digital dynamic shift register
26	ϕ_{Y1}	Phase 1 clock to Digital register
27	ϕ_{Y2}	Phase 2 clock to Digital register
28	NC	No connection

Table 2. Terminal Input Capacitance

Pin Number	Symbol	Capacitance (pF)
1	V_{Sub}	Substrate
2	GND	800
3	EOF	5
4	LO	17
5	LE	17
6	$ø_{LR}$	17
7	V_{Q1}	4
8	$ø_{R1}$	3
9	$ø_{X1O}$	22
10	$ø_{X2O}$	23
11	FRG	12
12	FRD	140
13	VID_1	12
14	NC	No connection
15	NC	No connection
16	VID_2	12
17	V_{DD}	230
18	V_{BUFF}	32
19	$ø_{X2E}$	23
20	$ø_{X1E}$	23
21	$ø_{R2}$	3
22	V_{BB}	31
23	V_{Q2}	4
24	$ø_{LT}$	17
25	$ø_{Start}$	5
26	$ø_{Y1}$	33
27	$ø_{Y2}$	33
28	NC	No connection

Table 3. Clock Rise and Fall Timing

Parameters	Min	Typ	Max	Units
$ø_{X1}$, $ø_{X2}$ Rise time	20	60		ns
$ø_{X1}$, $ø_{X2}$ Fall time	20	60		ns
$ø_{Y1}$, $ø_{Y2}$ Rise time	20	60		ns
$ø_{Y1}$, $ø_{Y2}$ Fall time	20	60		ns
Clock crossing $ø_{X1}$, $ø_{X2}$	0 [1]	40	50	% V_{DD}
Clock crossing $ø_{Y1}$, $ø_{Y2}$	20	50	80	% V_{DD}

Note:

[1] Clocks may be nonoverlaping with maximum of 50 nanoseconds dead time between rising and falling edges.

Table 4. Electrical Characteristics (77°K)

Symbol	Parameter		Min	Typ	Max	Units
$ø_X$	Bucket-Brigade register clock	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
$ø_Y$	Digital register clock	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
$ø_{LT}$	Line transfer	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.2	0.5	
$ø_{LR}$	Line reset	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
$ø_R$	Video reset	High	V_{DD}	V_{DD}+1	V_{DD}+1.5	V
		Low	-0.5	0.3	0.5	
$ø_{Start}$	Digital register start pulse	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
$ø_{FRG}$	Frame reset gate (frame reset mode only)	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
$ø_{FRD}$	Frame reset drain (frame reset mode only)	High	V_{DD}-3.5	V_{DD}-3	V_{DD}-2.5	V
		Low	-0.5	0.3	0.5	
EOF	End of frame (sync current)	High			V_{DD}	V
		Low			1.5	mA
V_{DD}	Power supply voltage		12	15	18	V
V_Q	BBD input bias		9	10	11	V
V_{BUFF}	Isolation gate bias		V_{DD}-2	V_{DD}-1.5	V_{DD}	V
V_{BB}	Transport bias		V_{DD}-3	V_{DD}-2.5	V_{DD}-1	V
V_{Sub}	Substrate voltage		-1	0		V
LO & LE	Line control		V_{DD}-1	V_{DD}-0.5	V_{DD}	V

Table 5. Electro-optical Characteristics (77°K and 2.5 MHz Pixel Rate)

Parameter	Typical	Units
Architecture	Photodiode	
Array size	128 x 128	pixels
Pixel size	60 x 60	μm^2
Fill factor	59	%
Chip size	433 x 453	mil^2
Cutoff wavelength (λ_c) Optical:	5.0 ~ 5.5	µm
Saturation charge (Q_{Sat})	2000K	electrons
Electron sensitivity	0.7	µV/e
Horizontal clock frequency	5	MHz
Maximum data rate	10	MHz/pixel
Frame rate	>450	frames/sec
Horizontal CTE	>.99996	
Readout noise at 80°K background	2000	electrons rms
Readout noise at 300°K background	2200	electrons rms
Dynamic range	>1000:1	peak signal to rms noise
MRT (without uniformity correction)	1	°C
Uniformity (element to element)	≤0.5%	rms
(overall)	≤±5%	
Offspec pixels	≤20	pixels

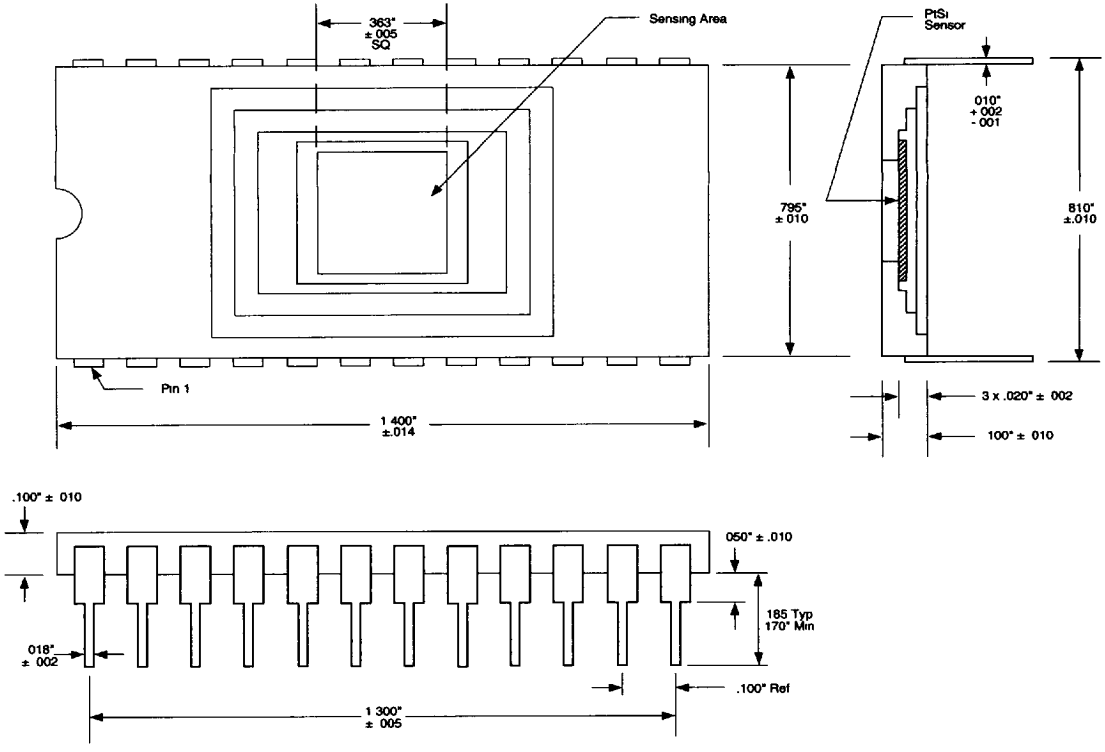

Figure 7. Package Dimensions

Ordering Information

Part Number	Detector Head
RA0128NIU-011	RH0128NIL-011

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