MAX44251/MAX44252

20V, Ultra-Precision, Low-Noise Op Amps

General Description

The MAX44251/MAX44252 are 20V, ultra-precision, low-noise, low-drift amplifiers that offer near-zero DC offset and drift through the use of patented autocorrelating zeroing techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of 1/f noise. These dual and quad devices feature rail-to-rail outputs, operate from a single 2.7V to 20V supply, and consume only 1.15mA per channel, while providing 5.9nV/√Hz input-referred voltage noise. The ICs are unity-gain stable with a gain-bandwidth product of 10MHz.

With excellent specifications such as offset voltage of 6µV (max), drift of 19nV/°C (max), and $123nV_{P-P}$ noise in 0.1Hz to 10Hz, the ICs are ideally suited for applications requiring ultra-low noise and DC precision such as interfacing with pressure sensors, strain gauges, precision weight scales, and medical instrumentation.

The ICs are available in 8-pin SOT23, 8-pin µMAX®, and 14-pin SOIC packages and are rated over the -40°C to +125°C temperature range.

***Ordering Information* appears at end of data sheet.**

***Functional Diagrams* appear at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX44251.related**.*

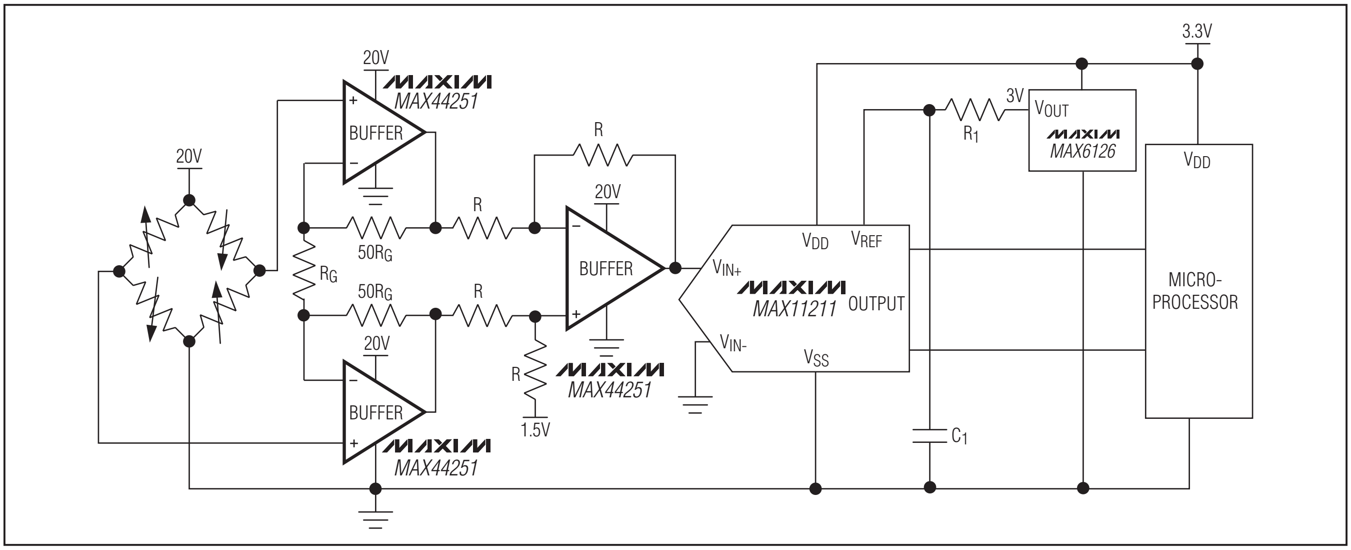
Benefits and Features

- **2.7V to 20V Power-Supply Range**
- **Integrated EMI Filter**
- **6µV Input Offset Voltage (max) at Room Temperature**
- **TCV_{OS} of 19nV/°C (max)**
- **Low 5.9nV/√Hz Input-Referred Voltage Noise**
- **$123nV_{P-P}$ in 0.1Hz to 10Hz**
- **Fast 400ns Settling Time**
- **10MHz Gain-Bandwidth Product**
- **Rail-to-Rail Output**
- **High Accuracy Enables Precision Signal Chain Acquisition**

Applications

Strain Gauges
Pressure Transducers
Medical Instrumentation
Precision Instrumentation
Load Cell and Bridge Transducer Amplification

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS})................................-0.3V to +22V
All Other Pins.................................(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Short-Circuit Duration to Either Supply Rail 1s
Continuous Input Current (any pin)................................ ±20mA
Differential Input Voltage... ±6V
Maximum Power Dissipation (T_A = +70°C)
SOT23 (derate 9.1 mW/°C above +70°C)..................727mW
µMAX (derate 4.5 mW/°C above +70°C) 362mW
SOIC (derate 8.3 mW/°C above +70°C) 666.7mW

Operating Temperature Range........................ -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

SOT23
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 196°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....70°C/W
µMAX
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....221°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....42°C/W

SOIC
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....120°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(**V_{DD} = 10V**, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V_{DD}	Guaranteed by PSRR		2.7		20	V
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{DD} = 2.7V to 20V, V_{CM} = 0V		140	145		dB
Quiescent Current per Amplifier	I_{DD}	R_L = ∞	T_A = +25°C		1.15	1.55	mA
			-40°C < T_A < +125°C			1.75	
Power-Up Time	t_{ON}				25		µs
DC SPECIFICATIONS							
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test		V_{SS} - 0.05		V_{DD} - 1.5	V
Common-Mode Rejection Ratio (Note 3)	CMRR	T_A = +25°C, V_{CM} = -0.05V to (V_{DD} - 1.5V)		133	140		dB
		-40°C < T_A < +125°C		130			

ELECTRICAL CHARACTERISTICS (continued)

(**V_{DD} = 10V**, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	V_{OS}	T_A = +25°C			3	6	µV
		-40°C < T_A < +125°C				7	
Input Offset Voltage Drift (Note 3)	TC V_{OS}				5	19	nV/°C
Input Bias Current (Note 3)	I_B	T_A = +25°C			200	1300	pA
		-40°C < T_A < +125°C				2400	
Input Offset Current (Note 3)	I_{OS}				400		pA
Open-Loop Gain (Note 3)	A_{VOL}	250mV ≤ V_{OUT} ≤ V_{DD} - 250mV, R_L = 10kΩ to V_{DD}/2	T_A = +25°C	145	154		dB
			-40°C < T_A < +125°C	136			
Output Short-Circuit Current		To V_{DD} or V_{SS}	Noncontinuous		96		mA
Output Voltage Low	V_{OL}	V_{OUT} - V_{SS}	R_L = 10kΩ to V_{DD}/2		12	25	mV
			R_L = 2kΩ to V_{DD}/2		45	85	
Output Voltage High	V_{OH}	V_{DD} - V_{OUT}	R_L = 10kΩ to V_{DD}/2		18	37	mV
			R_L = 2kΩ to V_{DD}/2		71	135	
AC SPECIFICATIONS							
Input Voltage-Noise Density	e_N	f = 1kHz			5.9		nV/√Hz
Input Voltage Noise		0.1Hz < f < 10Hz			123		nV_{P-P}
Input Current-Noise Density	i_N	f = 1kHz			0.6		pA/√Hz
Input Capacitance	C_{IN}				2		pF
Gain-Bandwidth Product	GBW				10		MHz
Phase Margin	PM	C_L = 20pF			60		Degrees
Slew Rate	SR	A_V = 1V/V, V_{OUT} = $2V_{P-P}$			8		V/µs
Capacitive Loading	C_L	No sustained oscillation, A_V = 1V/V			500		pF
Total Harmonic Distortion	THD	V_{OUT} = $2V_{P-P}$, A_V = +1V/V, R_L = 10kΩ to V_{DD}/2	f = 1kHz		-124		dB
			f = 20kHz		-119		
Settling Time		To 0.01%, V_{OUT} = 2V step, A_V = -1V/V			400		ns

ELECTRICAL CHARACTERISTICS

(**V_{DD} = 3.3V**, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Quiescent Current per Amplifier	I_{DD}	R_L = ∞	T_A = +25°C		1.1	1.5	mA
			-40°C < T_A < +125°C			1.65	
Power-Up Time	t_{ON}				25		µs
DC SPECIFICATIONS							
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test		V_{SS} - 0.05		V_{DD} - 1.5	V
Common-Mode Rejection Ratio (Note 3)	CMRR	T_A = +25°C, V_{CM} = -0.05V to (V_{DD} - 1.5V)		120	129		dB
		-40°C < T_A < +125°C		117			
Input Offset Voltage (Note 3)	V_{OS}	T_A = +25°C			3	5.5	µV
		-40°C < T_A < +125°C				6.5	
Input Offset Voltage Drift (Note 3)	TC V_{OS}				8	18	nV/°C
Input Bias Current (Note 3)	I_B	T_A = +25°C			200	1100	pA
		-40°C < T_A < +125°C				1200	
Input Offset Current (Note 3)	I_{OS}				400		pA
Open-Loop Gain (Note 3)	A_{VOL}	250mV ≤ V_{OUT} ≤ V_{DD} - 250mV, R_L = 10kΩ to V_{DD}/2	T_A = +25°C	136	151		dB
			-40°C < T_A < +125°C	133			
Output Short-Circuit Current		To V_{DD} or V_{SS}	Noncontinuous		58		mA
Output Voltage Low	V_{OL}	V_{OUT} - V_{SS}	R_L = 10kΩ to V_{DD}/2		5	22	mV
			R_L = 2kΩ to V_{DD}/2		17	42	
Output Voltage High	V_{OH}	V_{DD} - V_{OUT}	R_L = 10kΩ to V_{DD}/2		9	22	mV
			R_L = 2kΩ to V_{DD}/2		29	52	
AC SPECIFICATIONS							
Input Voltage-Noise Density	e_N	f = 1kHz			6.2		nV/√Hz
Input Voltage Noise		0.1Hz < f < 10Hz			123		nV_{P-P}
Input Current-Noise Density	i_N	f = 1kHz			0.3		pA/√Hz
Input Capacitance	C_{IN}				2		pF
Gain-Bandwidth Product	GBW				10		MHz

ELECTRICAL CHARACTERISTICS (continued)

(**V_{DD} = 3.3V**, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 2)

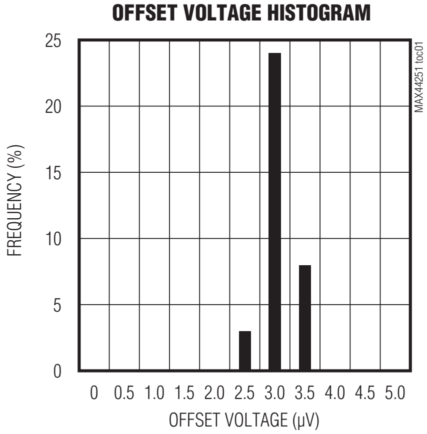
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Phase Margin	PM	C_L = 20pF			60		Degrees
Slew Rate	SR	A_V = 1V/V, V_{OUT} = $1V_{P-P}$, 10% to 90%			5		V/µs
Capacitive Loading	C_L	No sustained oscillation, A_V = 1V/V			500		pF
Total Harmonic Distortion	THD	V_{OUT} = $1V_{P-P}$, A_V = +1V/V, V_{CM} = V_{DD}/4, R_L = 10kΩ to V_{DD}/2	f = 1kHz		-124		dB
			f = 20kHz		-100		
Settling Time		To 0.01%, V_{OUT} = 1V step, A_V = -1V/V			200		ns

Note 2: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 3: Guaranteed by design.

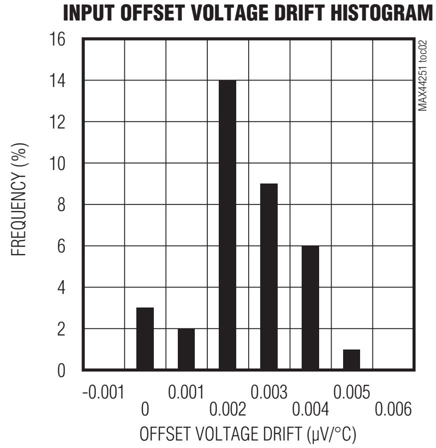
Typical Operating Characteristics

(V_{DD} = 10V, V_{SS} = 0V, outputs have R_L = 10kΩ to V_{DD}/2. T_A = +25°C, unless otherwise specified.)

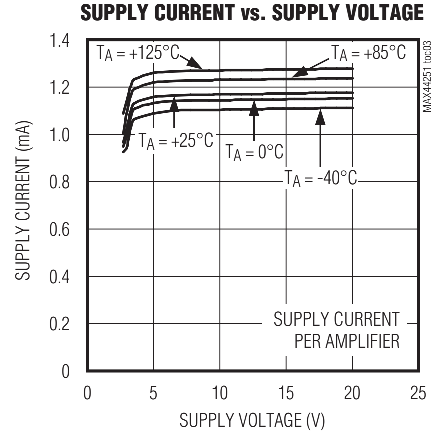
OFFSET VOLTAGE HISTOGRAM



INPUT OFFSET VOLTAGE DRIFT HISTOGRAM

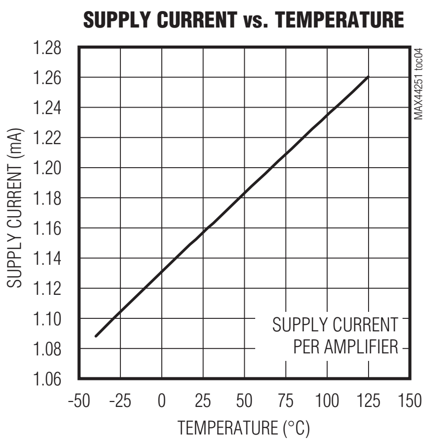


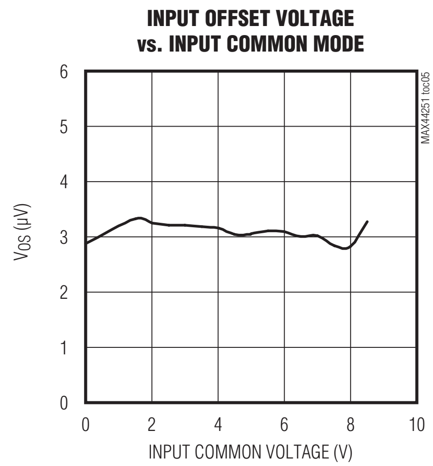
SUPPLY CURRENT vs. SUPPLY VOLTAGE

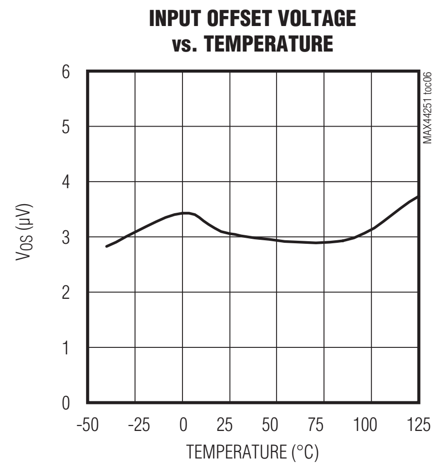


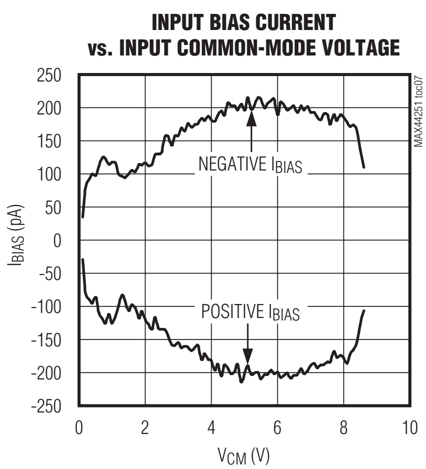
Typical Operating Characteristics (continued)

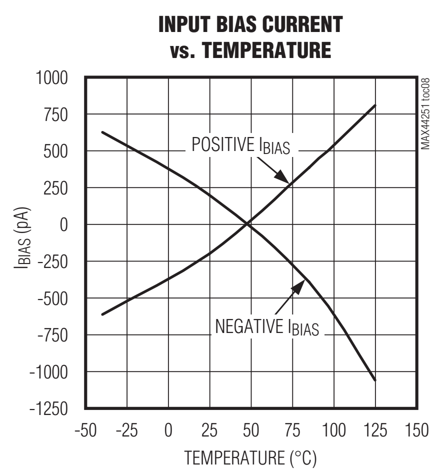
(V_{DD} = 10V, V_{SS} = 0V, outputs have R_L = 10kΩ to V_{DD}/2. T_A = +25°C, unless otherwise specified.)

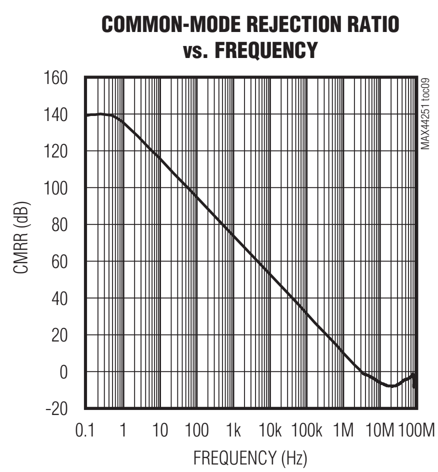








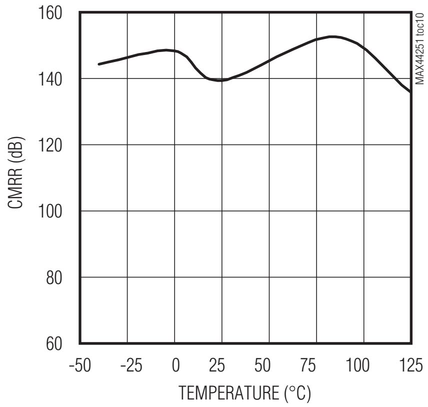




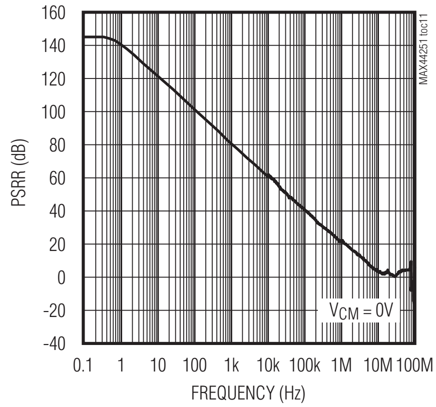
Typical Operating Characteristics (continued)

(V_{DD} = 10V, V_{SS} = 0V, outputs have R_L = 10kΩ to $V_{DD}/2$. T_A = +25°C, unless otherwise specified.)

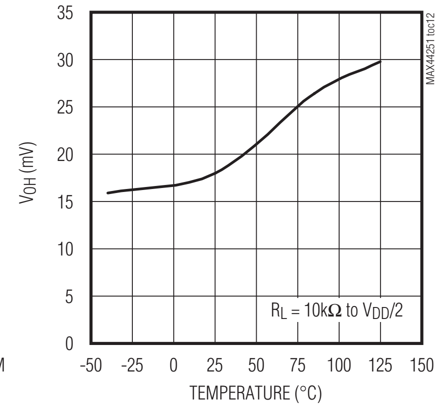
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



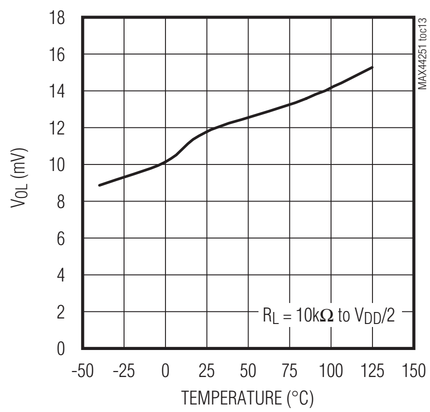
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



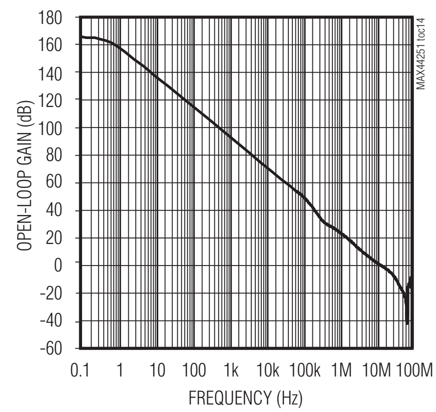
OUTPUT VOLTAGE SWING HIGH vs. TEMPERATURE



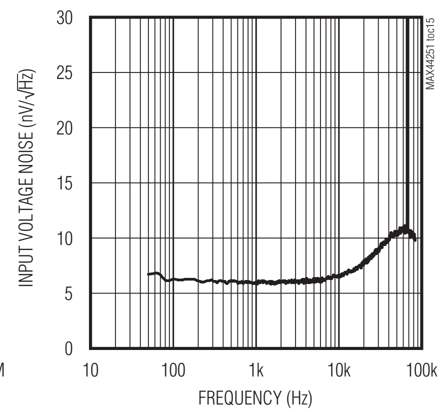
OUTPUT VOLTAGE SWING LOW vs. TEMPERATURE



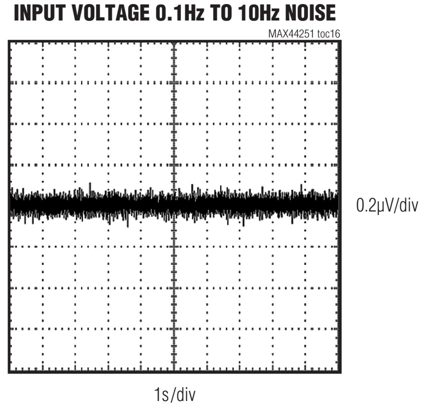
OPEN-LOOP GAIN vs. FREQUENCY



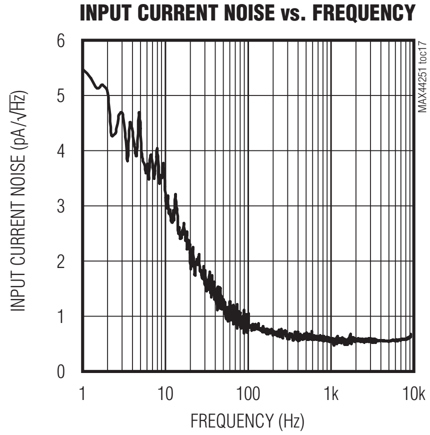
INPUT VOLTAGE NOISE vs. FREQUENCY



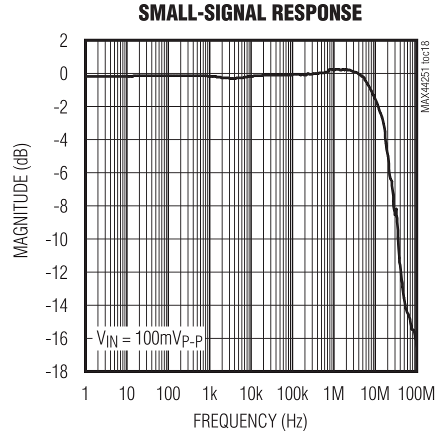
INPUT VOLTAGE 0.1Hz TO 10Hz NOISE



INPUT CURRENT NOISE vs. FREQUENCY



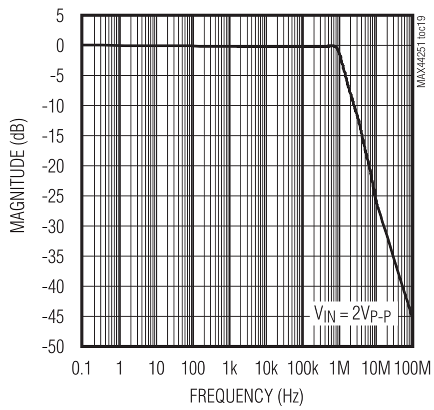
SMALL-SIGNAL RESPONSE



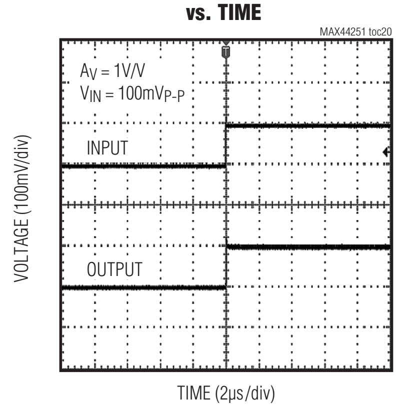
Typical Operating Characteristics (continued)

(V_{DD} = 10V, V_{SS} = 0V, outputs have R_L = 10kΩ to $V_{DD}/2$. T_A = +25°C, unless otherwise specified.)

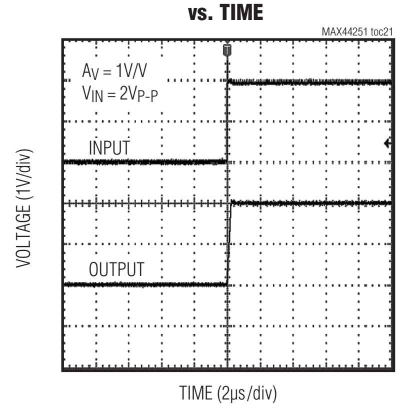
LARGE-SIGNAL RESPONSE



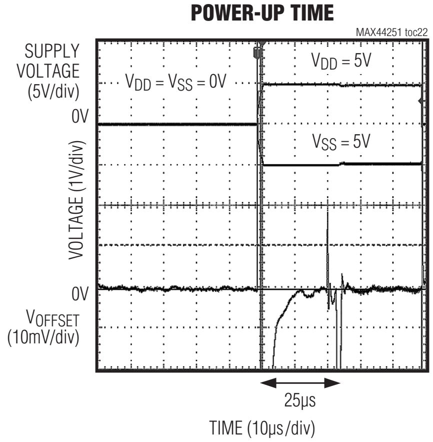
SMALL-SIGNAL STEP RESPONSE vs. TIME



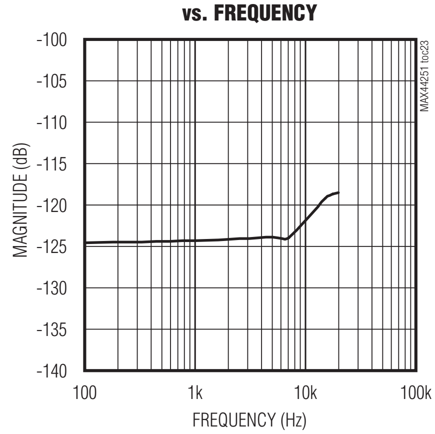
LARGE-SIGNAL STEP RESPONSE vs. TIME



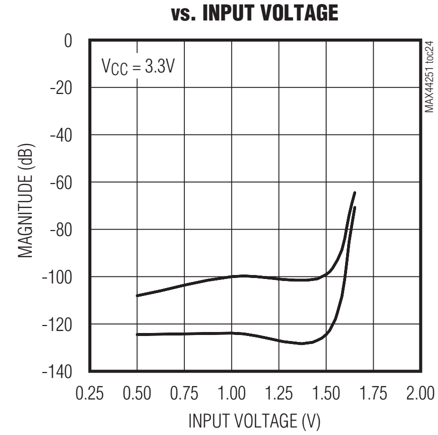
POWER-UP TIME



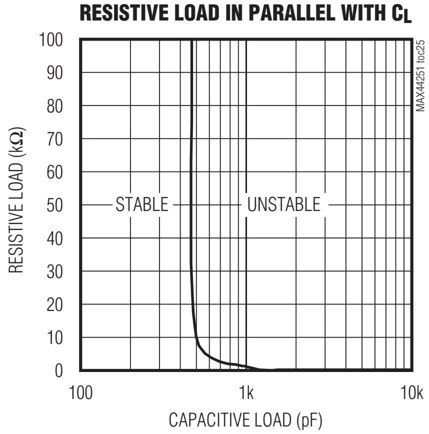
TOTAL HARMONIC DISTORTION vs. FREQUENCY



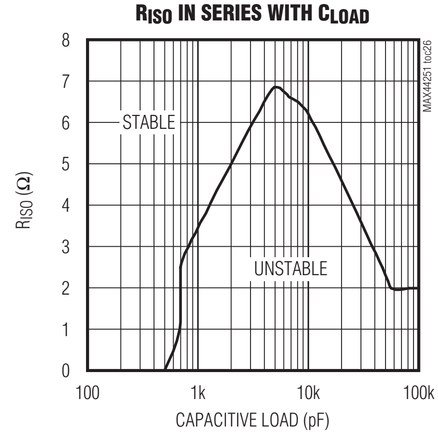
TOTAL HARMONIC DISTORTION vs. INPUT VOLTAGE



STABILITY vs. CAPACITIVE AND RESISTIVE LOAD IN PARALLEL WITH C_L

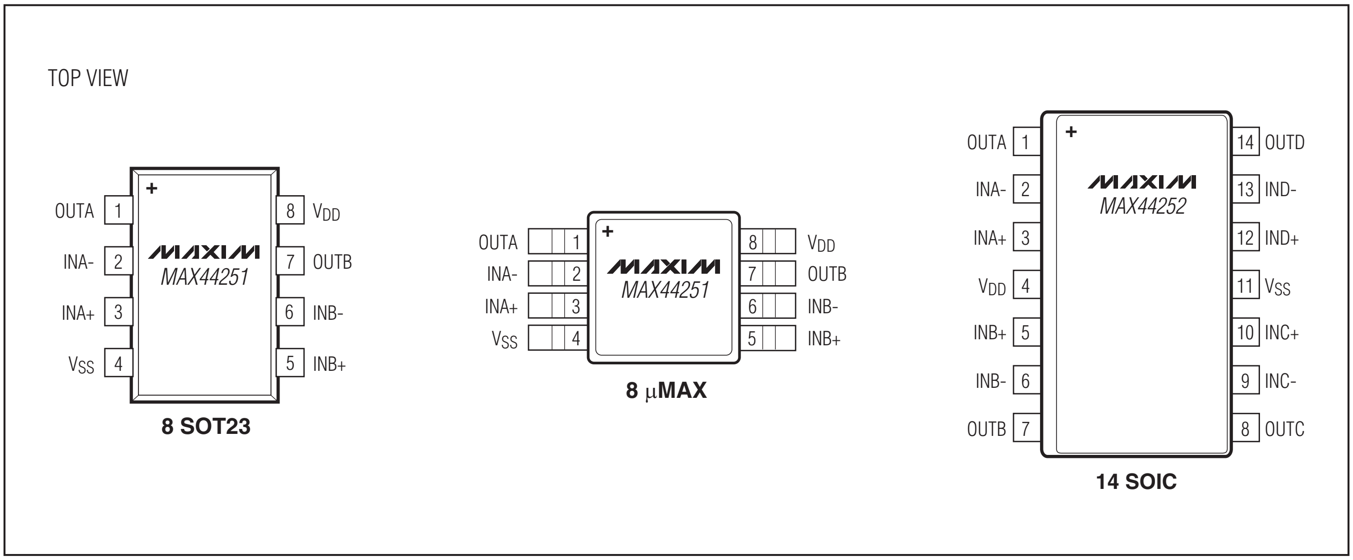


STABILITY vs. CAPACITIVE AND R_{ISO} IN SERIES WITH C_{LOAD}



20V, Ultra-Precision, Low-Noise Op Amps

Pin Configurations



Pin Description

PIN			NAME	FUNCTION
SOT23	µMAX	SOIC		
1	1	1	OUTA	Channel A Output
2	2	2	INA-	Channel A Negative Input
3	3	3	INA+	Channel A Positive Input
4	4	11	V_{SS}	Negative Supply Voltage
5	5	5	INB+	Channel B Positive Input
6	6	6	INB-	Channel B Negative Input
7	7	7	OUTB	Channel B Output
8	8	4	V_{DD}	Positive Supply Voltage
—	—	8	OUTC	Channel C Output
—	—	9	INC-	Channel C Negative Input
—	—	10	INC+	Channel C Positive Input
—	—	12	IND+	Channel D Positive Input
—	—	13	IND-	Channel D Negative Input
—	—	14	OUTD	Channel B Output

Detailed Description

The MAX44251/MAX44252 are high-precision amplifiers that have less than 3μV of typical input-referred offset and low flicker noise. These characteristics are achieved through an autozeroing technique that samples and finds repeating patterns of signal to cancel the input offset voltage and 1/f noise of the amplifier.

Autozero

The ICs feature an autozero circuit that allows the devices to achieve less than 6μV (max) of input offset voltage at room temperature and eliminate the 1/f noise.

Noise Suppression

Flicker noise, inherent in all active devices, is inversely proportional to frequency presented. Charges at the oxide-silicon interface that are trapped-and-released by MOSFET oxide occurs at low frequency more often. For this reason, flicker noise is also called 1/f noise.

Electromagnetic interference (EMI) noise occurs at higher frequency that results in malfunction or degradation of electrical equipment.

The ICs have an input EMI filter to avoid the output getting affected by radio frequency interference. The EMI filter composed of passive devices presents significant higher impedance to higher frequency.

High Supply Voltage Range

The ICs feature 1.15mA current consumption per channel and a voltage supply range from either 2.7V to 20V single supply or ±1.35V to ±10V split supply.

Applications Information

The ICs are ultra-high-precision operational amplifiers with a high supply voltage range designed for load cell, medical instrumentation and precision instrument applications.

These devices are also designed to interface with pressure transducers and are ideal for precision weight scale application as shown in Figure 1.

ADC Buffer Amplifier

The MAX44251/MAX44252's low input offset voltage, low noise, and fast settling time make these amplifiers ideal for ADC buffers. Weigh scales are one application that often require a low-noise, high-voltage amplifier in front of an ADC. Figure 1 details an example of a load cell and amplifier driven from the same ±10V supplies, along with the MAX11211 18-bit delta sigma ADC. Load cells produce a very small voltage change at their outputs, therefore driving the excitation source with a higher voltage produces a wider dynamic range that can be measured at the ADC inputs.

The MAX11211 ADC operates from a single 2.7V to 3.6V analog supply, offers 18-bit noise-free resolution and 0.86mW power dissipation. The MAX11211 also offers > 100dB rejection at 50Hz and 60Hz. This ADC is part of a family of 16-, 18-, 20-, and 24-bit delta sigma ADCs with high precision and < 1mW power dissipation.

The MAX44251/MAX44252's low input offset voltage and low noise allow a gain circuit prior to the MAX11211 without losing any dynamic range at the ADC.

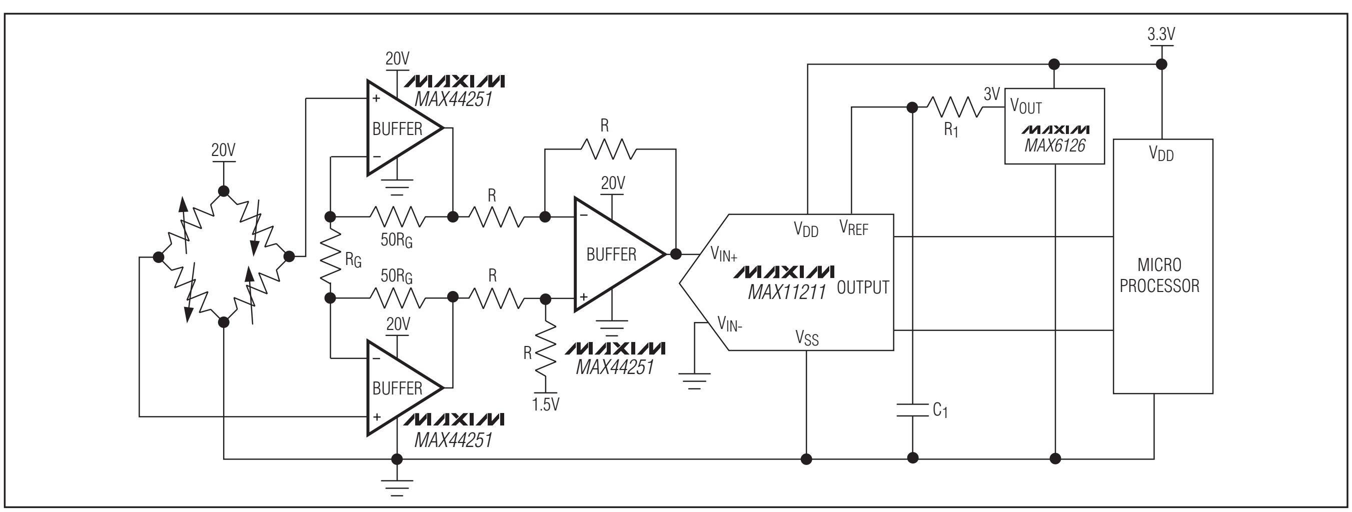


Figure 1. Weight Scale Application Circuit

Error Budget Example

When using the ICs as an ADC buffer in strain gauge application, the temperature drift should be taken into consideration to determine maximum input signal. A typical strain gauge has sensitivity specification of just 2mV/V at rated out load. This means that when the strain gauge load cell is powered with 10V, the full-scale output voltage is 20mV. In this application, both offset voltage and drift are critical parameters that directly affect the accuracy of measurement. Even though offset voltage could be calibrated out, its drift over temperature is still a problem.

The ICs, with a typical offset drift of 5nV/°C, guarantee that the drift over a 10°C range is only 50nV. Setting this equal to 0.5 LSB in a 18-bit system yields a full-scale range of 13mV. With a single 10V supply, an acceptable closed-loop gain of 770V/V provides sufficient gain while maintaining headroom.

Precision Low-Side Current Sensing

The ICs' autozero feature produces ultra-low offset voltage and drift, making them ideal for precision current-sensing applications. Figure 2 shows the ICs in a low-side current-sense configuration. This circuit produces an accurate output voltage, V_{OUT} equal to I_{LOAD} x R_{SENSE} x R_2/R_1.

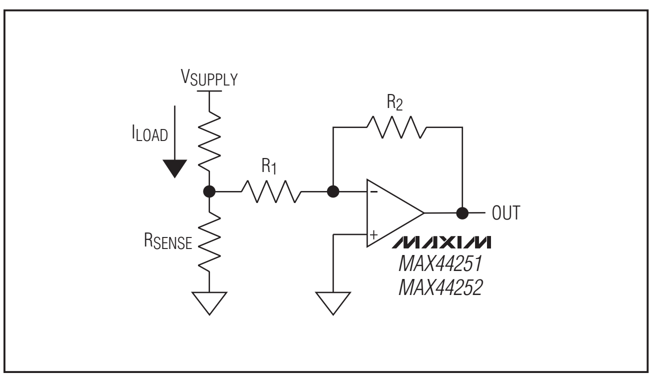


Figure 2. Low-Side Current Sensing

Chip Information

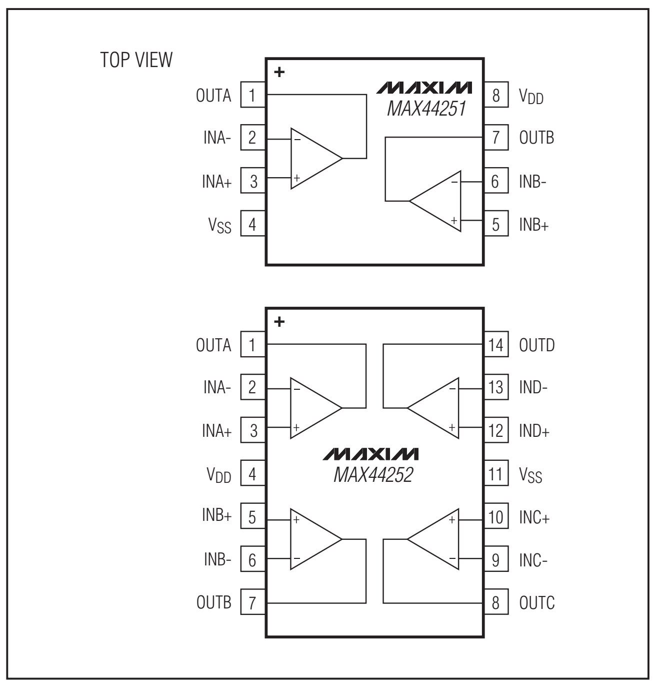
PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44251AKA+	-40°C to +125°C	8 SOT23	AERC
MAX44251AUA+	-40°C to +125°C	8 µMAX	—
MAX44252ASD+*	-40°C to +125°C	14 SOIC	—

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*

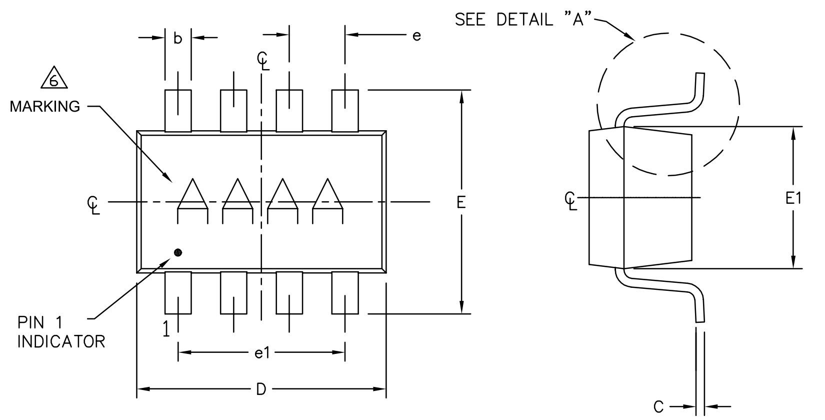
Functional Diagrams



Package Information

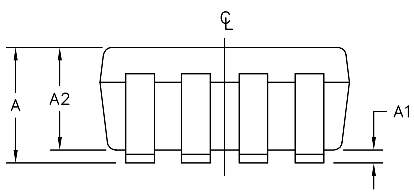
For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

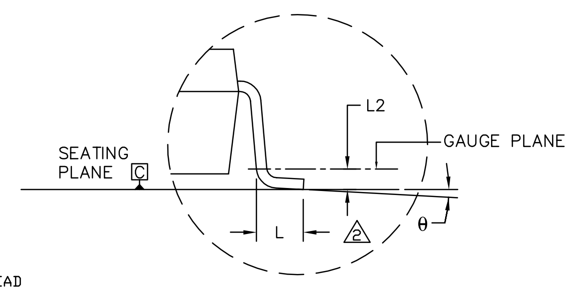
PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN
8 SOT23	K8+5	**21-0078**	**90-0176**
8 µMAX	U8+1	**21-0036**	**90-0092**
14 SOIC	S14M+5	**21-0041**	**90-0096**



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°

PKG CODES:
K8-1, K8-2, K8F-4, K8FH-4, K8-5, K8SN-1; K8CN-2





DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

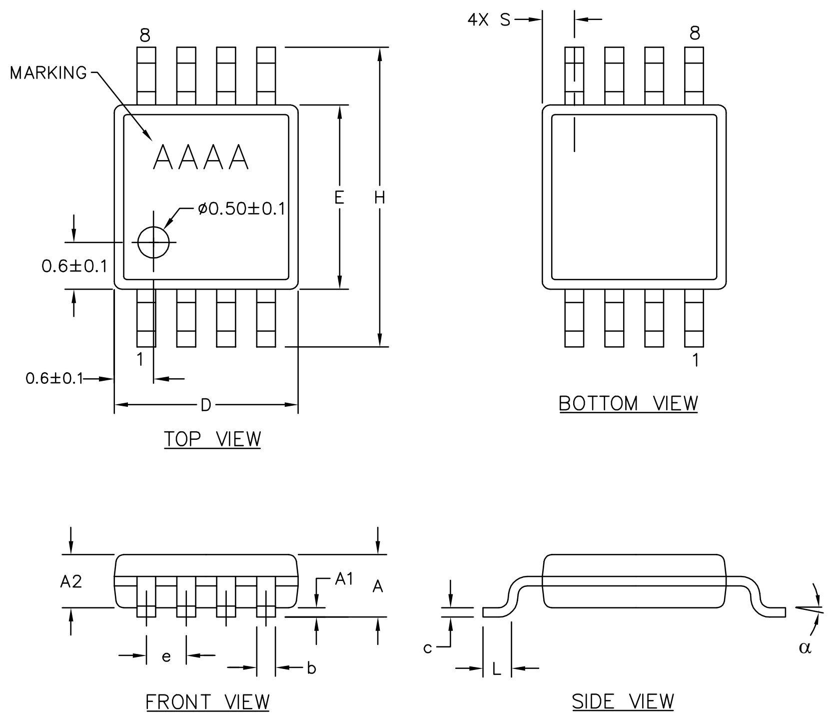
-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	J	1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	
PKG. CODES: U8–1; U8–3; U8CN–1				

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

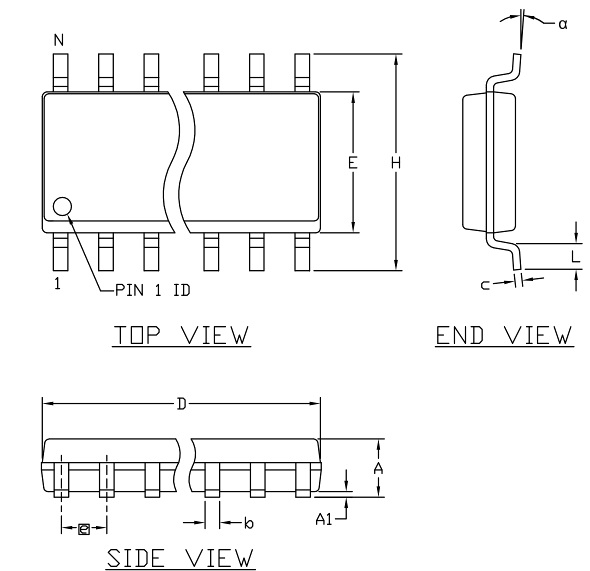
MAXIM

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0036	L	1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



COMMON DIMENSIONS				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
b	.014	.019	0.35	0.49
c	.007	.010	0.19	0.25
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
α	0°	8°	0°	8°

VARIATION A				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.189	.197	4.80	5.00
N	8			
MS012	AA			
PKG. CODE	S8-2, S8-4, S8-5, S8-6F, S8-7F, S8-8F, S8-10F, S8-11F, S8-16F			

VARIATION B				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.337	.344	8.55	8.75
N	14			
MS012	AB			
PKG. CODE	S14-1, S14-4, S14-5, S14-6; S14M-4, S14M-5, S14M-6, S14M-7			

VARIATION C				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.386	.394	9.80	10.00
N	16			
MS012	AC			
PKG. CODE	S16-1, S16-3, S16-5, S16-6, S16-8, S16-7F, S16-9F, S16-10F; S16M-3, S16M-6			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
4. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
5. MEETS JEDEC MS012
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, 8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	C	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/11	Initial release	—

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