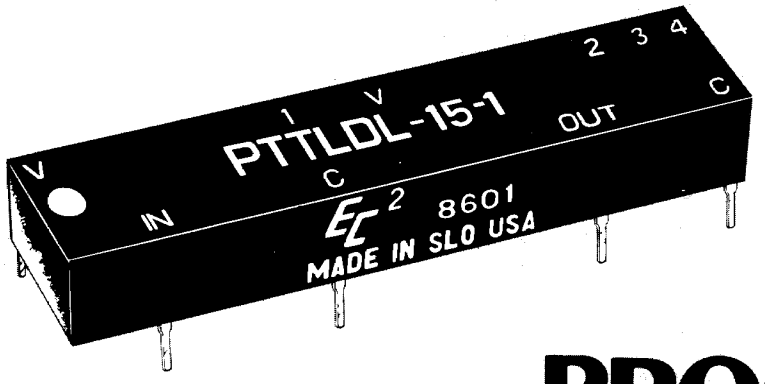
EC²



low profile

T²L COMPATIBLE 4-BIT PROGRAMMABLE LOGIC DELAY LINE

- T²L input and output
- Delays stable and precise
- 32-pin DIP package (.250 high)
- Available in delays up to 765ns
- Available in 18 delay steps with resolution from 1 to 50ns
- Propagation delays fully compensated
- All delays digitally programmable
- 10 T²L fan-out capacity

design notes

The "DIP Series" of Programmable Logic Delay Lines developed by Engineered Components Company have been designed to allow for final delay adjustment during or after installation in a circuit. These Logic Delay Lines incorporate required driving and pick-off circuitry and are contained in a 32-pin DIP package compatible with T²L and DTL circuits. These modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 1 million hours. The design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the required delay.

The Logic Delay Lines are digitally programmable by the presence of either a "1" or a "0" at each of the programming pins. Since the input and the output terminals are fixed and the programming is accomplished only by DC voltage levels, programming may be accomplished by remote switching or permanent termination of the appropriate programming pins of the Logic Delay Line to ground; the Logic Delay Line may also be programmed automatically by computer generated data. MUX set-up time is 4ns typical. When no need exists in the application to change delay time during normal use, the desired delay is most conveniently established by use of a ground pad around each programming pin; programming is accomplished by cutting off those pins which are to remain at state "1" before insertion of the Logic Delay Line into the printed circuit board.

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The PTTLDL is offered in 18 models with time delays to a maximum of 765ns and with step resolution as shown in the Part Number Table. Programming of maximum delay is accomplished in 16 steps in accordance with the Truth Table example shown on page 3. Tolerances on minimum delay, delay change per step and deviation from the programmed delay are shown in the Part Number Table on page 3.

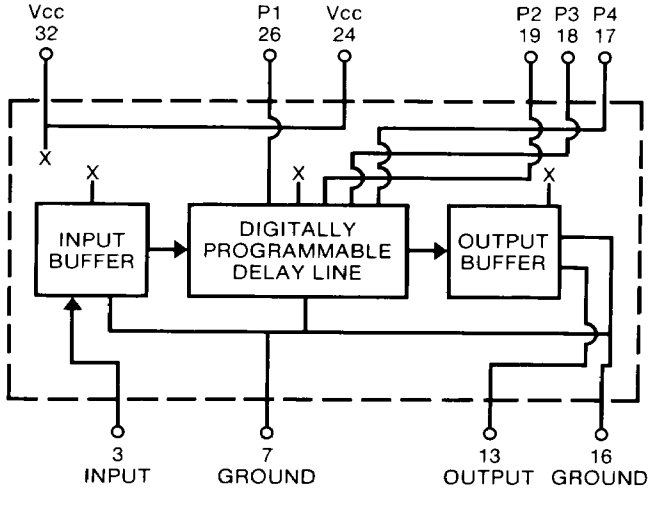
Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum, when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately −300 ppm/°C over the operating temperature range of 0 to +70°C.

The PTTLDL is designed for use with positive input pulses and will reproduce these at the output without inversion. All modules can be driven by a standard Schottky T^2L gate. Output is Schottky T^2L toggle; programming inputs are Schottky T^2L single fan-in. These Logic Delay Lines have the capability of driving up to 10 T^2L loads.

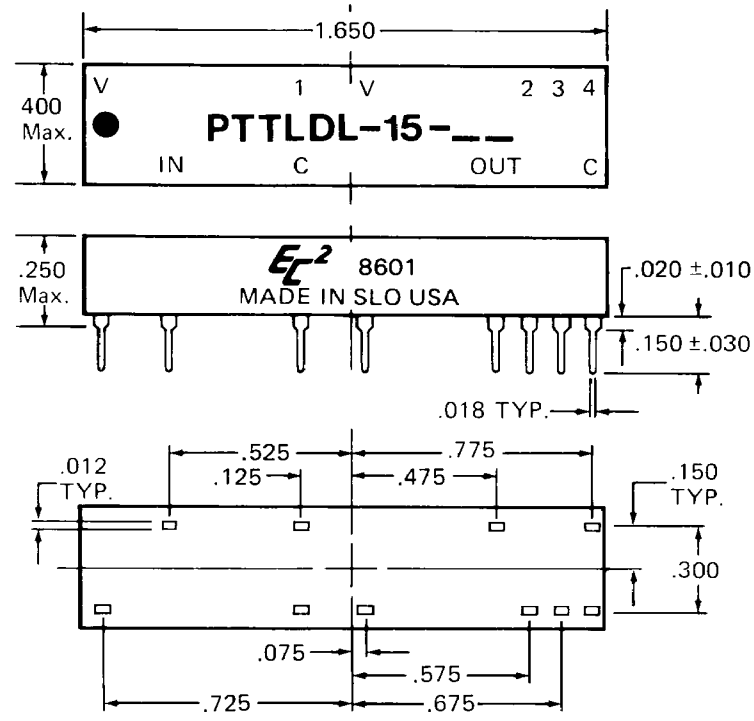
These "DIP Series" Programmable Logic Delay Lines are packaged in a 32-pin DIP housing, molded of flameproof Diallyl Phthalate per MIL-M-14, type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of manufacturer's name, logo (EC^2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vcc supply voltage is maintained at 5.0V DC.
3. All units are tested using a Schottky toggle-type positive input pulse and one Schottky T^2L load at the output.

φ4. Input pulse width used is 40ns for units with delay change of 1 to 5ns/step and 400ns for units with delay change of 6ns/step and greater. Pulse period for all units is 5000ns.

OPERATING SPECIFICATIONS

* V_{cc} supply voltage:	4.75 to 5.25V DC
V_{cc} supply current:	120ma typical
Logic 1 input:	
Voltage	2V min; 5.5V max.
Current	2.4V = 100ua max.
	5.5V = 2ma max.
Logic 0 input:	
Voltage	.8V max.
Current	−4ma max.
Logic 1 Voltage out:	2.4V min.
Logic 0 Voltage out:	.5V max.
Operating temperature range:	0 to 70°C.
Storage temperature:	−55 to +125°C.

* Delays increase approximately 1.5% for a decrease of 5% in supply voltage and decrease approximately 1.5% for an increase of 5% in supply voltage.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)				
Part Number	***Step Zero Delay Time**	**Maximum Delay Time (Nom)**	**Delay Change Per Step**	****Maximum Deviation From Programmed Delay**
PTTLDL-15-1	15 ±.6	30	1 ±.4	±.8
PTTLDL-15-2	15 ±.6	45	2 ±.5	±1.2
PTTLDL-15-3	15 ±.6	60	3 ±.5	±1.6
PTTLDL-15-4	15 ±.6	75	4 ±.6	±1.8
PTTLDL-15-5	15 ±.6	90	5 ±.6	±2.0
PTTLDL-15-6	15 ±.6	105	6 ±.8	±2.4
PTTLDL-15-7	15 ±.6	120	7 ±.8	±2.8
PTTLDL-15-8	15 ±.6	135	8 ±1	±3.2
PTTLDL-15-9	15 ±.6	150	9 ±1	±3.6
PTTLDL-15-10	15 ±.6	165	10 ±1	±4
PTTLDL-15-15	15 ±.6	240	15 ±1.5	±6
PTTLDL-15-20	15 ±.6	315	20 ±2	±8
PTTLDL-15-25	15 ±.6	390	25 ±2	±10
PTTLDL-15-30	15 ±.6	465	30 ±2.5	±12
PTTLDL-15-35	15 ±.6	540	35 ±2.5	±14
PTTLDL-15-40	15 ±.6	615	40 ±3	±16
PTTLDL-15-45	15 ±.6	690	45 ±3	±18
PTTLDL-15-50	15 ±.6	765	50 ±3	±20

TRUTH TABLE EXAMPLES

Programming Pins / Part Number	4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
PTTLDL-15-1		15	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PTTLDL-15-2		15	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
PTTLDL-15-3		15	3	6	9	12	15	18	21	24	27	30	33	36	39	42	45
ETC.																	

* Delay at step zero is referenced to the input pin.

* * All delay times after step zero are referenced to step zero.

ϕ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified delay times for specific applications.