

# M5M467405/465405DJ,DTP -5,-6,-5S,-6S

# M5M467805/465805DJ,DTP -5,-6,-5S,-6S

# M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

**PRELIMINARY**

Some of contents are subject to change without notice.

**DESCRIPTION**

The M5M467405/465405DJ,DTP is a 16777216-word by 4-bit, M5M467805/465805DJ,DTP is a 8388608-word by 8-bit, and M5M465165DJ,DTP is a 4194304-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and are suitable for large-capacity memory systems with high speed and low power dissipation.

**FEATURES**

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M467405DXX-5,5S M5M467805DXX-5,5S	50	13	25	13	84	300
M5M467405DXX-6,6S M5M467805DXX-6,6S	60	15	30	15	104	250
M5M465405DXX-5,5S M5M465805DXX-5,5S	50	13	25	13	84	390
M5M465405DXX-6,6S M5M465805DXX-6,6S	60	15	30	15	104	325

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M465165DXX-5,5S	50	13	25	13	84	420
M5M465165DXX-6,6S	60	15	30	15	104	390

XX=J,TP

- Standard 32 pin SOJ, 32 pin TSOP (M5M467405Dxx/M5M465405Dxx/M5M467805Dxx/M5M465805Dxx)  
Standard 50 pin SOJ, 50 pin TSOP (M5M465165Dxx)
- Single 3.3 ± 0.3V supply
- Low stand-by power dissipation  
1.8mW (Max) ----- LVCMOS input level
- Low operating power dissipation
  - M5M467405Dxx-5,5S / M5M467805Dxx-5,5S ----- 360.0mW (Max)
  - M5M467405Dxx-6,6S / M5M467805Dxx-6,6S ----- 324.0mW (Max)
  - M5M465405Dxx-5,5S / M5M465805Dxx-5,5S ----- 468.0mW (Max)
  - M5M465405Dxx-6,6S / M5M465805Dxx-6,6S ----- 432.0mW (Max)
  - M5M465165Dxx-5,5S ----- 504.0mW (Max)
  - M5M465165Dxx-6,6S ----- 468.0mW (Max)
- Self refresh capability\*  
Self refresh current ----- 400µA (Max)
- EDO mode , Read-modify-write, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode , OE and W to control output buffer impedance
- All inputs, outputs LVTTTL compatible and low capacitance  
\* : Applicable to self refresh version(M5M467405/465405/467805/465805/465165DJ,DTP-5S,-6S:option) only

**ADDRESS**

Part No.	Row Add.	Col. Add.	Refresh	Refresh Cycle	
				Normal	S-version
M5M467405Dxx	A0-A12	A0-A10	RAS Only Ref,Normal R/W	8192/64ms	8192/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465405Dxx	A0-A11	A0-A11	RAS Only Ref,Normal R/W	4096/64ms	4096/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M467805Dxx	A0-A12	A0-A9	RAS Only Ref,Normal R/W	8192/64ms	8192/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465805Dxx	A0-A11	A0-A10	RAS Only Ref,Normal R/W	4096/64ms	4096/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465165Dxx	A0-A11	A0-A9	RAS Only Ref,Normal R/W	4096/64ms	4096/128ms

**APPLICATION**

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT



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#### PIN DESCRIPTION

M5M467405Dxx / M5M465405Dxx

Pin Name	Function
A0-A12	Address Inputs
DQ1-DQ4	Data Inputs / Outputs
$\overline{\text{RAS}}$	Row Address Strobe Input
$\overline{\text{CAS}}$	Column Address Strobe Input
$\overline{\text{W}}$	Write Control Input
$\overline{\text{OE}}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

M5M467805Dxx / M5M465805Dxx

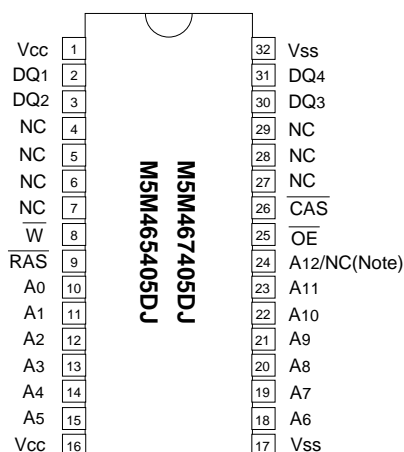
Pin Name	Function
A0-A12	Address Inputs
DQ1-DQ8	Data Inputs / Outputs
$\overline{\text{RAS}}$	Row Address Strobe Input
$\overline{\text{CAS}}$	Column Address Strobe Input
$\overline{\text{W}}$	Write Control Input
$\overline{\text{OE}}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

M5M465165Dxx

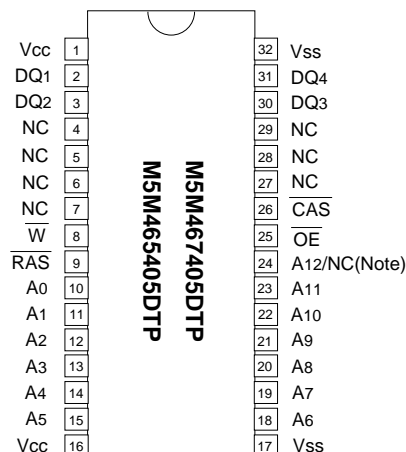
Pin Name	Function
A0-A11	Address Inputs
DQ1-DQ16	Data Inputs / Outputs
$\overline{\text{RAS}}$	Row Address Strobe Input
$\overline{\text{UCAS}}$	Upper byte control Column Address Strobe Input
$\overline{\text{LCAS}}$	Lower byte control Column Address Strobe Input
$\overline{\text{W}}$	Write Control Input
$\overline{\text{OE}}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

XX=J, TP

#### M5M467400/465400DJ, DTP PIN CONFIGURATION (TOP VIEW)



Outline 32P0N (400mil SOJ)



Outline 32P3N (400mil TSOP Normal Bend)

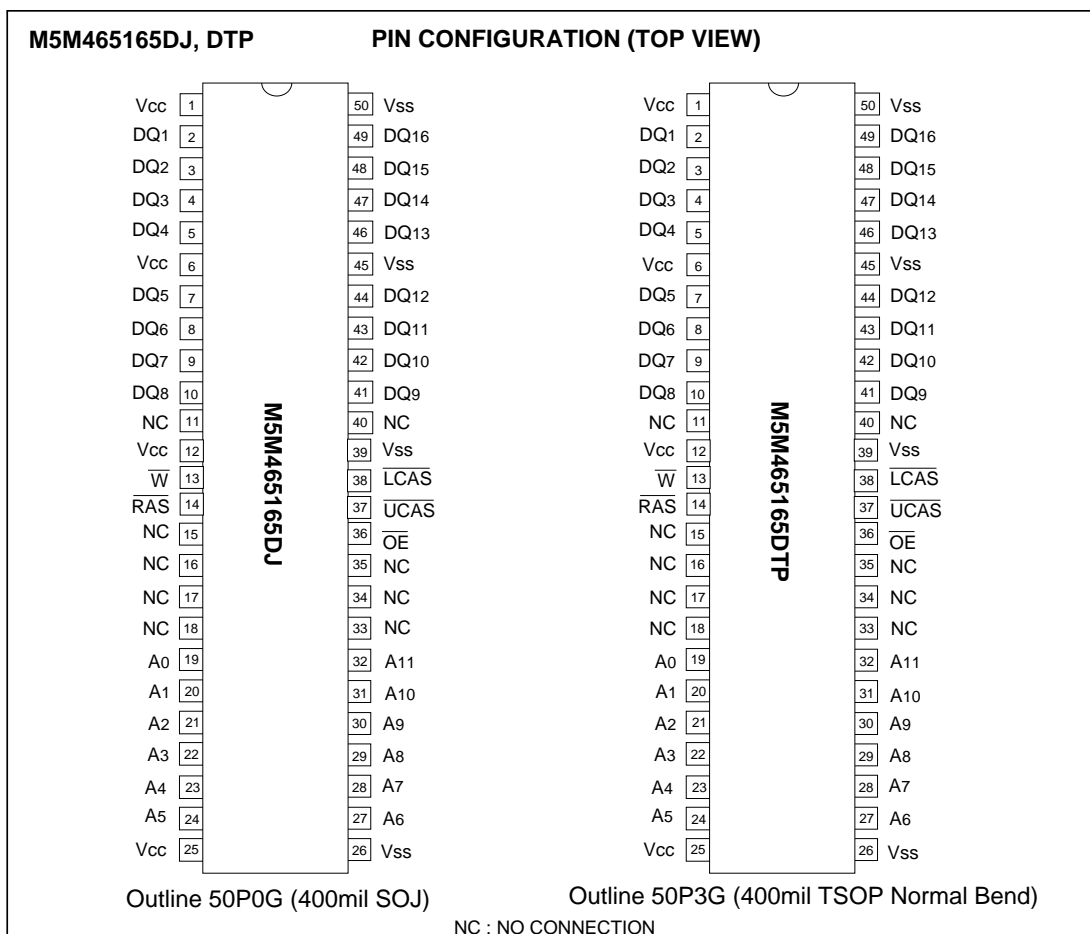
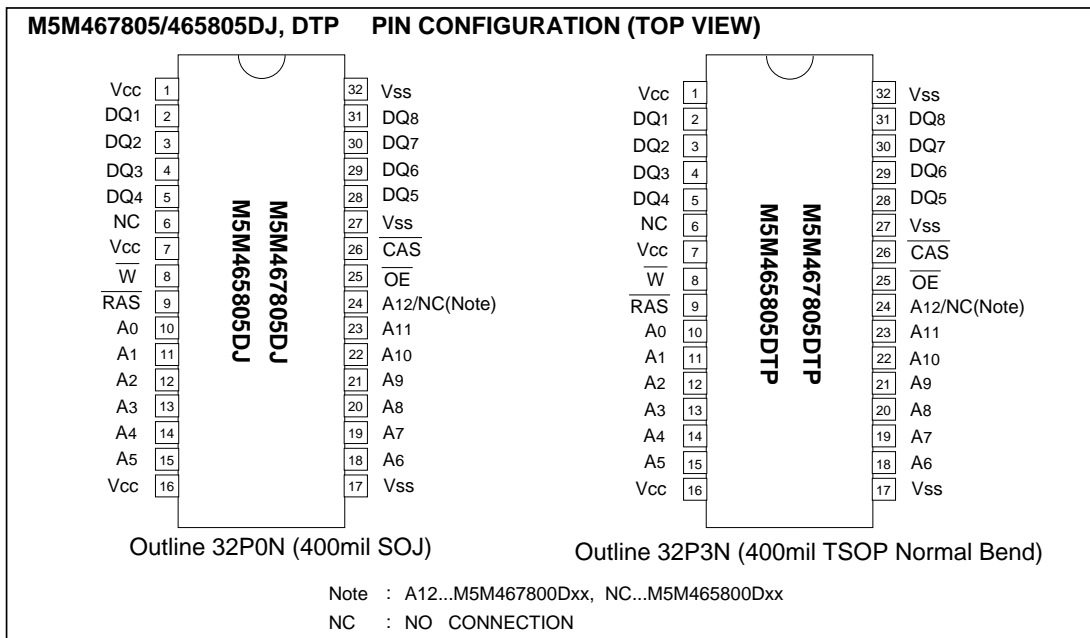
Note : A12...M5M467405Dxx, NC...M5M465405Dxx  
 NC : NO CONNECTION

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## FUNCTION

The M5M467405(805)/465405(805,165)DJ, DTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., EDO mode,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, and delayed-write.

The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

M5M467405Dxx / M5M465405Dxx / M5M467805Dxx / M5M465805Dxx

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	EDO mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	NO	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	NO	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	NO	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

M5M465165Dxx

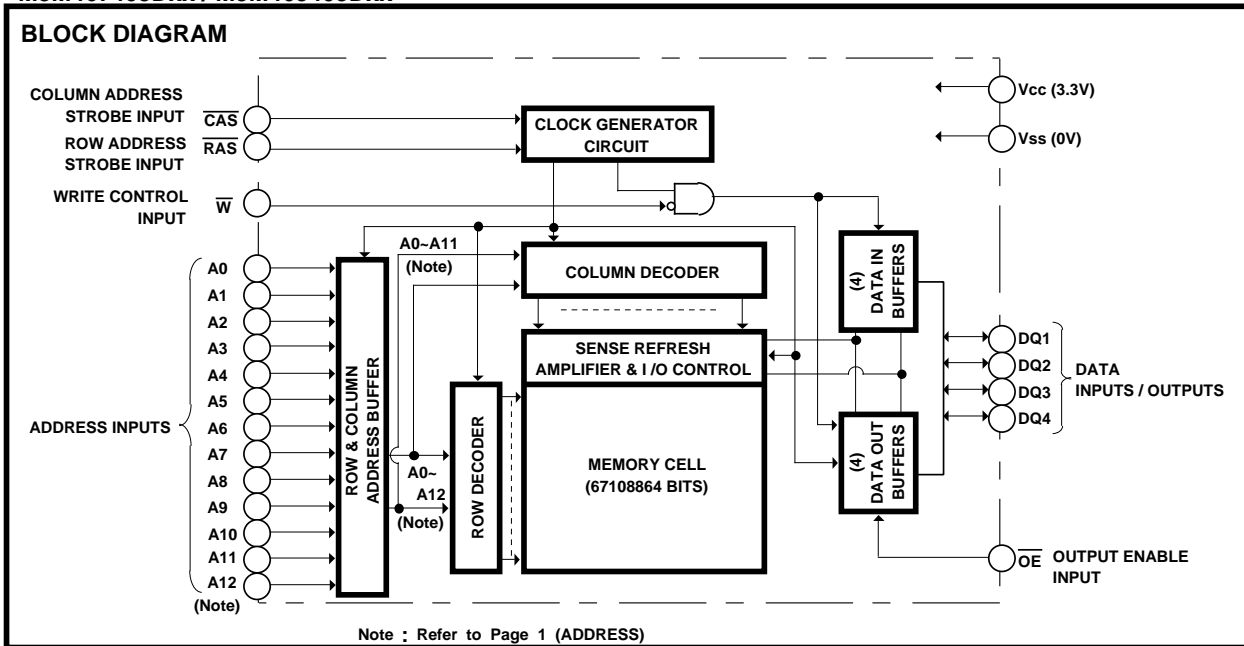
Operation	Inputs						Input/Output		Refresh	Remark	
	$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	DQ1-DQ8			DQ9-DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	APD	APD	VLD	OPN	NO	EDO mode identical
Upper byte read	ACT	NAC	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	
Word read	ACT	ACT	ACT	NAC	ACT	APD	APD	VLD	VLD	NO	
Lower byte write	ACT	ACT	NAC	ACT	NAC	APD	APD	DIN	DNC	NO	
Upper byte write	ACT	NAC	ACT	ACT	NAC	APD	APD	DNC	DIN	NO	
Word write	ACT	ACT	ACT	ACT	NAC	APD	APD	DIN	DIN	NO	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DNC	DNC	VLD	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

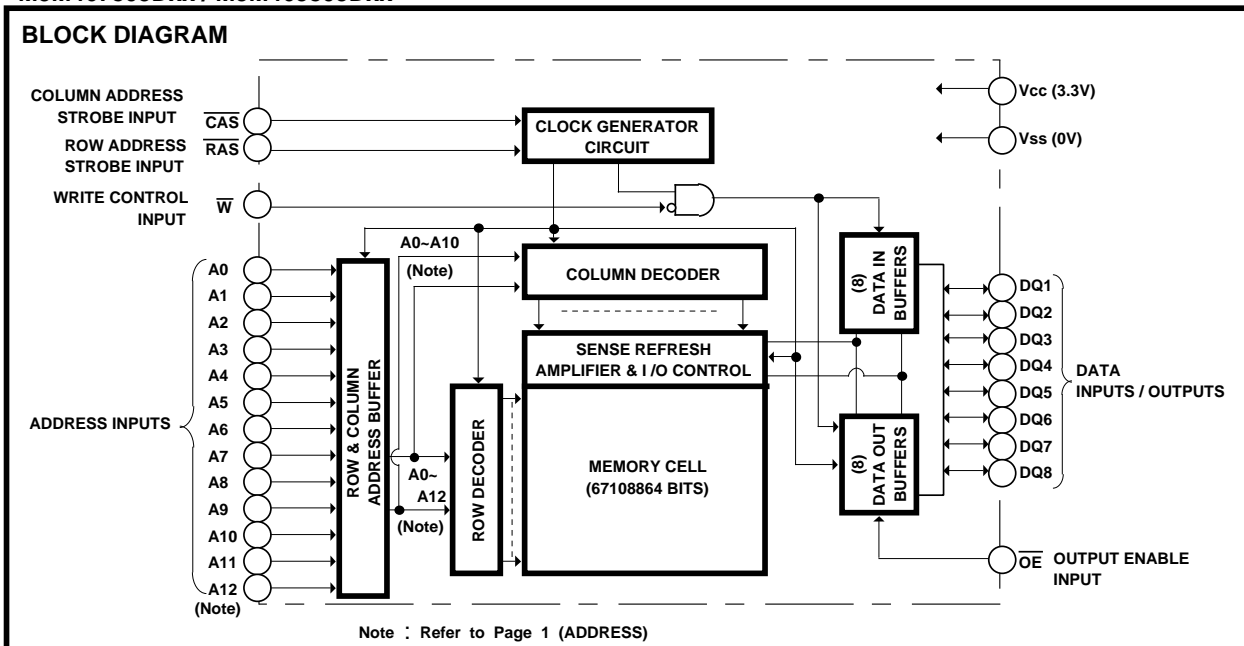
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## M5M467405Dxx / M5M465405Dxx



## M5M467805Dxx / M5M465805Dxx



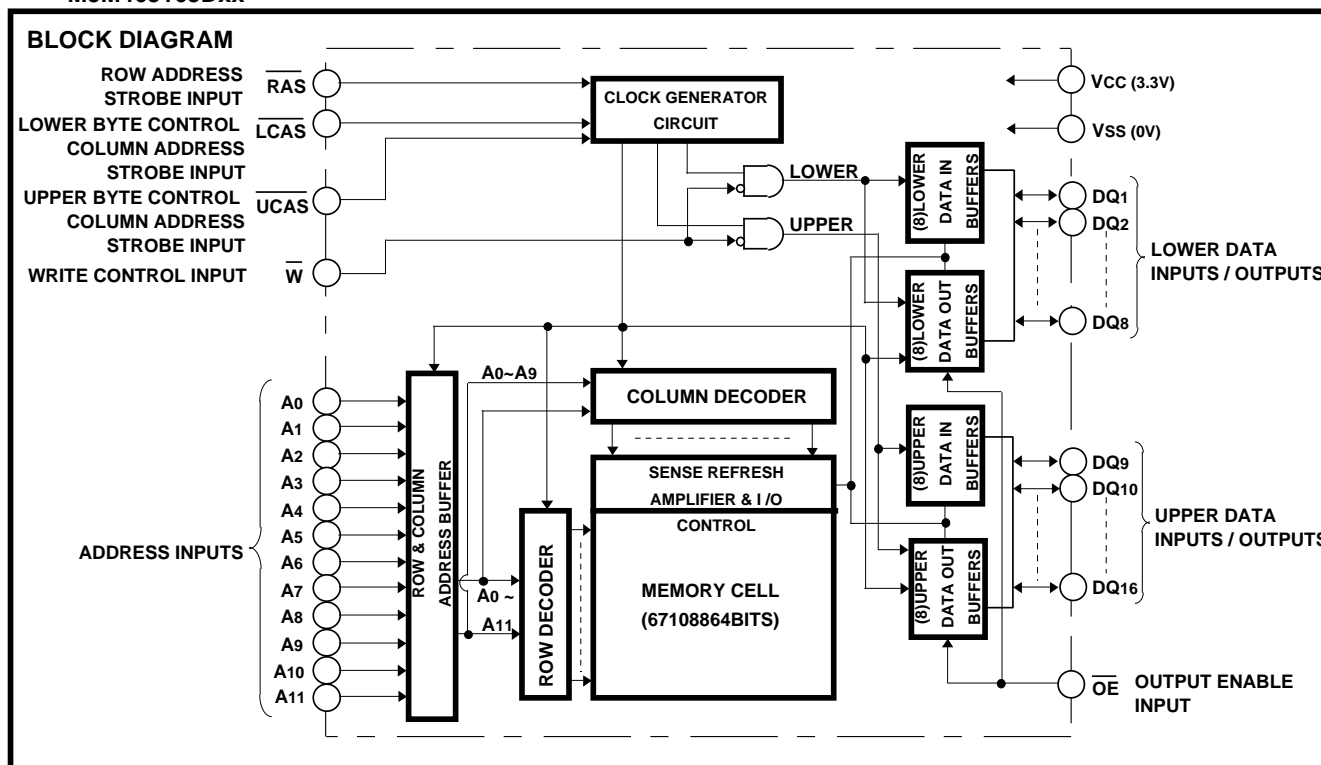
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M5M465165Dxx



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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	With respect to V <sub>SS</sub>	-0.5 ~ 4.6	V
V <sub>I</sub>	Input voltage		-0.5 ~ 4.6	V
V <sub>O</sub>	Output voltage		-0.5 ~ 4.6	V
I <sub>O</sub>	Output current		50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	1000	mW
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

## RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub>=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	3.0	3.3	3.6	V
V <sub>SS</sub>	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	2.0		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V<sub>SS</sub>.

## ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~ 70°C, V<sub>CC</sub>=3.3 ± 0.3V, V<sub>SS</sub>=0V, unless otherwise noted) (Note 2)

### [M5M467405D / M5M467805D]

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> =-2mA	2.4		V <sub>CC</sub>	v	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =2mA	0		0.4	v	
I <sub>OZ</sub>	Off-state output current	Q floating 0V V <sub>OUT</sub> V <sub>CC</sub>	-10		10	μA	
I <sub>I</sub>	Input current	0V V <sub>IN</sub> V <sub>CC</sub> +0.3V, Other input pins=0V	-10		10	μA	
I <sub>CC1 (AV)</sub>	Average supply current from V <sub>CC</sub> operating (Note 3,4,5)	M5M467405D-5,5S M5M467805D-5,5S	RAS, CAS cycling trc=twc=min. output open			100	mA
		M5M467405D-6,6S M5M467805D-6,6S				90	
I <sub>CC2 (AV)</sub>	Average supply current from V <sub>CC</sub> stand-by (Note 6)	M5M467405D-5,5S -6,6S M5M467805D-5,5S -6,6S	RAS= CAS =V <sub>IH</sub> , output open			1	mA
		M5M467405D-5,6 M5M467805D-5,6	RAS= CAS V <sub>CC</sub> -0.2V, output open			0.5	
		M5M467405D-5S,6S M5M467805D-5S,6S				0.3	
I <sub>CC4 (AV)</sub>	Average supply current from V <sub>CC</sub> EDO-Mode (Note 3,4,5)	M5M467405D-5,5S M5M467805D-5,5S	RAS=V <sub>IL</sub> , CAS cycling thPC=min. output open			100	mA
		M5M467405D-6,6S M5M467805D-6,6S				90	
I <sub>CC6 (AV)</sub>	Average supply current from V <sub>CC</sub> CAS before RAS refresh mode (Note 3,5)	M5M467405D-5,5S M5M467805D-5,5S	CAS before RAS refresh cycling trc=min. output open			130	mA
		M5M467405D-6,6S M5M467805D-6,6S				120	

Note 2: Current flowing into an IC is positive, out is negative.

3: I<sub>CC1 (AV)</sub>, I<sub>CC4 (AV)</sub> and I<sub>CC6 (AV)</sub> are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I<sub>CC1 (AV)</sub> and I<sub>CC4 (AV)</sub> are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V<sub>IL</sub> and CAS=V<sub>IH</sub>.

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## ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

### [M5M465405D / M5M465805D]

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> =-2mA	2.4		V <sub>CC</sub>	V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =2mA	0		0.4	V	
I <sub>OZ</sub>	Off-state output current	Q floating 0V V <sub>OUT</sub> V <sub>CC</sub>	-10		10	μA	
I <sub>I</sub>	Input current	0V V <sub>IN</sub> V <sub>CC</sub> +0.3V, Other input pins=0V	-10		10	μA	
I <sub>CC1</sub> (AV)	Average supply current from V <sub>CC</sub> operating (Note 3,4,5)	M5M465405D-5,5S M5M465805D-5,5S	RAS, CAS cycling t <sub>RC</sub> =t <sub>WC</sub> =min. output open			130	mA
		M5M465405D-6,6S M5M465805D-6,6S				120	
I <sub>CC2</sub> (AV)	Average supply current from V <sub>CC</sub> stand-by (Note 6)	M5M465405D-5,5S -6,6S M5M465805D-5,5S -6,6S	RAS= CAS =V <sub>IH</sub> , output open			1	mA
		M5M465405D-5,6 M5M465805D-5,6	RAS= CAS V <sub>CC</sub> -0.2V, output open			0.5	
		M5M465405D-5S,6S M5M465805D-5S,6S				0.3	
I <sub>CC4</sub> (AV)	Average supply current from V <sub>CC</sub> EDO-Mode (Note 3,4,5)	M5M465405D-5,5S M5M465805D-5,5S	RAS=V <sub>IL</sub> , CAS cycling t <sub>HPC</sub> =min. output open			100	mA
		M5M465405D-6,6S M5M465805D-6,6S				90	
I <sub>CC6</sub> (AV)	Average supply current from V <sub>CC</sub> CAS before RAS refresh mode (Note 3,5)	M5M465405D-5,5S M5M465805D-5,5S	CAS before RAS refresh cycling t <sub>RC</sub> =min. output open			130	mA
		M5M465405D-6,6S M5M465805D-6,6S				120	

### [M5M465165D]

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> =-2mA	2.4		V <sub>CC</sub>	V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =2mA	0		0.4	V	
I <sub>OZ</sub>	Off-state output current	Q floating 0V V <sub>OUT</sub> V <sub>CC</sub>	-10		10	μA	
I <sub>I</sub>	Input current	0V V <sub>IN</sub> V <sub>CC</sub> +0.3V, Other input pins=0V	-10		10	μA	
I <sub>CC1</sub> (AV)	Average supply current from V <sub>CC</sub> operating (Note 3,4,5)	M5M465165D-5,5S	RAS, CAS cycling t <sub>RC</sub> =t <sub>WC</sub> =min. output open			140	mA
		M5M465165D-6,6S				130	
I <sub>CC2</sub> (AV)	Average supply current from V <sub>CC</sub> stand-by (Note 6)	M5M465165D-5,5S -6,6S	RAS= CAS =V <sub>IH</sub> , output open			1	mA
		M5M465165D-5,6 M5M465165D-5S,6S	RAS= CAS V <sub>CC</sub> -0.2V, output open			0.5	
						0.3	
I <sub>CC4</sub> (AV)	Average supply current from V <sub>CC</sub> EDO-Mode (Note 3,4,5)	M5M465165D-5,5S	RAS=V <sub>IL</sub> , CAS cycling t <sub>HPC</sub> =min. output open			120	mA
		M5M465165D-6,6S				110	
I <sub>CC6</sub> (AV)	Average supply current from V <sub>CC</sub> CAS before RAS refresh mode (Note 3,5)	M5M465165D-5,5S	CAS before RAS refresh cycling t <sub>RC</sub> =min. output open			140	mA
		M5M465165D-6,6S				130	



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#### CAPACITANCE (Ta=0~70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I(A)</sub>	Input capacitance, address inputs	Vi=Vss f=1MHz Vi=25mVrms			5	pF
C <sub>I(OE)</sub>	Input capacitance, OE input				7	pF
C <sub>I(W)</sub>	Input capacitance, write control input				7	pF
C <sub>I(RAS)</sub>	Input capacitance, RAS input				7	pF
C <sub>I(CAS)</sub>	Input capacitance, CAS input				7	pF
C <sub>I/O</sub>	Input/Output capacitance, data ports				7	pF

#### SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S		M5M46X405D-6,6S		
		Min	Max	Min	Max	
t <sub>CAC</sub>	Access time from CAS (Note 7,8)		13		15	ns
t <sub>RAC</sub>	Access time from RAS (Note 7,9)		50		60	ns
t <sub>AA</sub>	Column address access time (Note 7,10)		25		30	ns
t <sub>CPA</sub>	Access time from CAS precharge (Note 7,11)		28		33	ns
t <sub>OE</sub>	Access time from OE (Note 7)		13		15	ns
t <sub>OH</sub>	Output hold time from CAS	5		5		ns
t <sub>OH</sub>	Output hold time from RAS (Note 13)	5		5		ns
t <sub>CLZ</sub>	Output low impedance time from CAS low (Note 7)	5		5		ns
t <sub>OEZ</sub>	Output disable time after OE high (Note 12)		13		15	ns
t <sub>WEZ</sub>	Output disable time after W high (Note 12)		13		15	ns
t <sub>OFF</sub>	Output disable time after CAS high (Note 12,13)		13		15	ns
t <sub>REZ</sub>	Output disable time after RAS high (Note 12,13)		13		15	ns

Note 6: An initial pause of 500µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS before RAS refresh).

Note the RAS may be cycled during the initial pause. And any eight initialization cycles are required after prolonged periods (greater than 64 ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V<sub>OH</sub>=2.4V(I<sub>OH</sub>=-2mA) / V<sub>OL</sub>=0.4V(I<sub>OL</sub>=2mA) loads and 100pF. The reference levels for measuring of output signals are V<sub>OH</sub>=2.0V and V<sub>OL</sub>=0.8V.

8: Assumes that t<sub>RC</sub> t<sub>RC(max)</sub> and t<sub>ASC</sub> t<sub>ASC(max)</sub> and t<sub>CP</sub> t<sub>CP(max)</sub>.

9: Assumes that t<sub>RC</sub> t<sub>RC(max)</sub> and t<sub>RAD</sub> t<sub>RAD(max)</sub>. If t<sub>RC</sub> or t<sub>RAD</sub> is greater than the maximum recommended value shown in this table, t<sub>RC</sub> will increase by amount that t<sub>RC</sub> exceeds the value shown.

10: Assumes that t<sub>RAD</sub> t<sub>RAD(max)</sub> and t<sub>ASC</sub> t<sub>ASC(max)</sub>.

11: Assumes that t<sub>CP</sub> t<sub>CP(max)</sub> and t<sub>ASC</sub> t<sub>ASC(max)</sub>.

12: t<sub>OEZ(max)</sub>, t<sub>WEZ(max)</sub>, t<sub>OFF(max)</sub> and t<sub>REZ(max)</sub> defines the time at which the output achieves the high impedance state (I<sub>OUT</sub> ± 10 µA) and is not reference to V<sub>OH(min)</sub> or V<sub>OL(max)</sub>.

13: Output is disabled after both RAS and CAS go to high.

# M5M467405/465405DJ,DTP -5,-6,-5S,-6S

# M5M467805/465805DJ,DTP -5,-6,-5S,-6S

# M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and EDO Mode Cycles)

(Ta=0 ~ 70°C, Vcc=3.3 ±0.3V, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S		M5M46X405D-6,6S		
		Min	Max	Min	Max	
tREF	Refresh cycle time		64		64	ms
tREF	Refresh cycle time (S-version only)		128		128	ms
trP	RAS high pulse width	30		40		ns
trCD	Delay time, RAS low to CAS low (Note16)	14	37	14	45	ns
tCRP	Delay time, CAS high to RAS low	5		5		ns
trPC	Delay time, RAS high to CAS low	0		0		ns
tCPN	CAS high pulse width	8		10		ns
tRAD	Column address delay time from RAS low (Note17)	10	25	12	30	ns
tASR	Row address setup time before RAS low	0		0		ns
tASC	Column address setup time before CAS low (Note18)	0	10	0	13	ns
tRAH	Row address hold time after RAS low	8		10		ns
tCAH	Column address hold time after CAS low	8		10		ns
tdZC	Delay time, data to CAS low (Note19)	0		0		ns
tdZO	Delay time, data to OE low (Note19)	0		0		ns
trDD	Delay time, RAS high to data (Note20)	13		15		ns
tcDD	Delay time, CAS high to data (Note20)	13		15		ns
tODD	Delay time, OE high to data (Note20)	13		15		ns
tWED	Delay time, W low to data (Note20)	13		15		ns
tT	Transition time (Note21)	1	50	1	50	ns

Note 14: The timing requirements are assumed  $t_T = 2ns$ .

15:  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals.

16:  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is less than  $t_{RCD(max)}$ , access time is  $t_{RAC}$ . If  $t_{RCD}$  is greater than  $t_{RCD(max)}$ , access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .

17:  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$ ,  $t_{ASC}$ ,  $t_{ASC(max)}$ , access time is controlled exclusively by  $t_{AA}$ .

18:  $t_{ASC(max)}$  is specified as a reference point only. If  $t_{RCD}$ ,  $t_{RCD(max)}$  and  $t_{ASC}$ ,  $t_{ASC(max)}$ , access time is controlled exclusively by  $t_{CAC}$ .

19: Either  $t_{dZC}$  or  $t_{dZO}$  must be satisfied.

20: Either  $t_{rDD}$  or  $t_{cDD}$  or  $t_{ODD}$  or  $t_{WED}$  must be satisfied.

21:  $t_T$  is measured between  $V_{IH(min)}$  and  $V_{IL(max)}$ .

## Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S		M5M46X405D-6,6S		
		Min	Max	Min	Max	
tRC	Read cycle time	84		104		ns
tRAS	RAS low pulse width	50	10000	60	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	ns
tCSH	CAS hold time after RAS low	35		40		ns
trSH	RAS hold time after CAS low	13		15		ns
tRCS	Read Setup time before CAS low	0		0		ns
trCH	Read hold time after CAS high (Note 22)	0		0		ns
trRH	Read hold time after RAS high (Note 22)	0		0		ns
trAL	Column address to RAS hold time	25		30		ns
tCAL	Column address to CAS hold time	13		18		ns
torH	RAS hold time after OE low	13		15		ns
toCH	CAS hold time after OE low	13		15		ns

Note 22: Either  $t_{rCH}$  or  $t_{rRH}$  must be satisfied for a read cycle.

# M5M467405/465405DJ,DTP -5,-6,-5S,-6S

# M5M467805/465805DJ,DTP -5,-6,-5S,-6S

# M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S		M5M46X405D-6,6S		
		Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	84		104		ns
t <sub>RAS</sub>	$\overline{\text{RAS}}$ low pulse width	50	10000	60	10000	ns
t <sub>CAS</sub>	$\overline{\text{CAS}}$ low pulse width	8	10000	10	10000	ns
t <sub>CSH</sub>	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	35		40		ns
t <sub>RSH</sub>	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	13		15		ns
t <sub>WCS</sub>	Write setup time before $\overline{\text{CAS}}$ low (Note 24)	0		0		ns
t <sub>WCH</sub>	Write hold time after $\overline{\text{CAS}}$ low	8		10		ns
t <sub>CWL</sub>	$\overline{\text{CAS}}$ hold time after $\overline{\text{W}}$ low	8		10		ns
t <sub>RWL</sub>	$\overline{\text{RAS}}$ hold time after $\overline{\text{W}}$ low	8		10		ns
t <sub>WP</sub>	Write pulse width	8		10		ns
t <sub>DS</sub>	Data setup time before $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	0		0		ns
t <sub>DH</sub>	Data hold time after $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	8		10		ns

## Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S		M5M46X405D-6,6S		
		Min	Max	Min	Max	
t <sub>RWC</sub>	Read write/read modify write cycle time (Note23)	109		133		ns
t <sub>RAS</sub>	$\overline{\text{RAS}}$ low pulse width	75	10000	89	10000	ns
t <sub>CAS</sub>	$\overline{\text{CAS}}$ low pulse width	38	10000	44	10000	ns
t <sub>CSH</sub>	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	70		82		ns
t <sub>RSH</sub>	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	38		44		ns
t <sub>RCS</sub>	Read setup time before $\overline{\text{CAS}}$ low	0		0		ns
t <sub>CWD</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (Note24)	28		32		ns
t <sub>RWD</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (Note24)	65		77		ns
t <sub>AWD</sub>	Delay time, address to $\overline{\text{W}}$ low (Note24)	40		47		ns
t <sub>OEH</sub>	$\overline{\text{OE}}$ hold time after $\overline{\text{W}}$ low	13		15		ns

Note 23: t<sub>RWC</sub> is specified as t<sub>RWC</sub>(min)=t<sub>RAC</sub>(max)+t<sub>ODD</sub>(min)+t<sub>RWL</sub>(min)+t<sub>RP</sub>(min)+4t.

24: t<sub>WCS</sub>, t<sub>CWD</sub>, t<sub>RWD</sub> and t<sub>AWD</sub> and, t<sub>CPWD</sub> are specified as reference points only. If t<sub>WCS</sub> t<sub>WCS</sub>(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If t<sub>CWD</sub> t<sub>CWD</sub>(min), t<sub>RWD</sub> t<sub>RWD</sub>(min), t<sub>AWD</sub> t<sub>AWD</sub>(min) and t<sub>CPWD</sub> t<sub>CPWD</sub>(min) (for EDO mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied, the DQ (at access time and until  $\overline{\text{CAS}}$  or  $\overline{\text{OE}}$  goes back to V<sub>IH</sub>) is indeterminate.

# M5M467405/465405DJ,DTP -5,-6,-5S,-6S

# M5M467805/465805DJ,DTP -5,-6,-5S,-6S

# M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## EDO Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle,

Read Write Mix Cycle, Hi-Z control by  $\overline{OE}$  or  $\overline{W}$ ) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S		M5M46X405D-6,6S		
		Min	Max	Min	Max	
tHPC	EDO mode read/write cycle time	20		25		ns
tHPRWC	EDO Mode read write / read modify write cycle time	55		66		ns
tDOH	Output hold time from $\overline{CAS}$ low	5		5		ns
tRAS	RAS low pulse width for read write cycle (Note26)	65	100000	77	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note27)	8	13	10	16	ns
tCPRH	RAS hold time after CAS precharge	28		33		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	43		50		ns
tCHOL	Hold time to maintain the data Hi-Z until CAS access	7		7		ns
tOEPE	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		ns
tWPE	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	40		47		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		ns
tHAOD	Delay time, Address to $\overline{OE}$ high after read	25		30		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective EDO mode cycle.

26: tRAS(min) is specified as two cycles of  $\overline{CAS}$  input are performed.

27: tCP(max) is specified as a reference point only. If tCP < tCP(max), access time is controlled exclusively by tCAC.

## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S		M5M46X405D-6,6S		
		Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		ns

Note 28: Eight or more  $\overline{CAS}$  before  $\overline{RAS}$  cycles instead of eight  $\overline{RAS}$  cycles are necessary for proper operation of  $\overline{CAS}$  before  $\overline{RAS}$  refresh mode.

# M5M467405/465405DJ,DTP -5,-6,-5S,-6S

# M5M467805/465805DJ,DTP -5,-6,-5S,-6S

# M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S . The other characteristics and requirements than the below are same as normal devices.

## ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>CC8</sub> (AV)	Average supply current from V <sub>CC</sub> Extended - Refresh cycle (note 5,6)	M5M46X405D-5S,6S M5M46X805D-5S,6S M5M465165D-5S,6S CAS before RAS refresh cycling input high level V <sub>CC</sub> -0.2V input low level 0.2V output = OPEN, t <sub>RC</sub> = 31.25μs t <sub>RAS</sub> = t <sub>RAS</sub> (min) ~ 300ns			500	μA
I <sub>CC9</sub> (AV)	Average supply current from V <sub>CC</sub> Self - Refresh cycle (note 6)	M5M46X405D-5S,6S M5M46X805D-5S,6S M5M465165D-5S,6S RAS = CAS 0.2V output = OPEN			400	μA

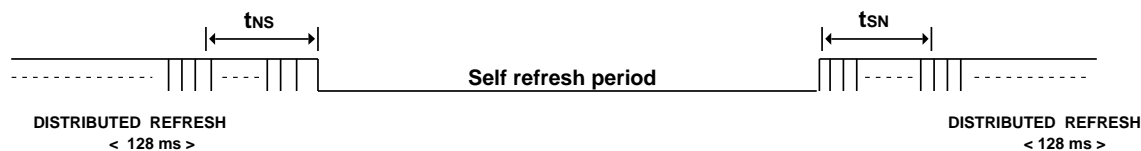
## TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5S		M5M46X405D-6S		
		Min	Max	Min	Max	
t <sub>RASS</sub>	Self Refresh RAS low pulse width	100		100		μs
t <sub>RPS</sub>	Self Refresh RAS high precharge time	84		104		ns
t <sub>CHS</sub>	Self Refresh CAS hold time	- 50		- 50		ns

## SELF REFRESH ENTRY & EXIT CONDITIONS

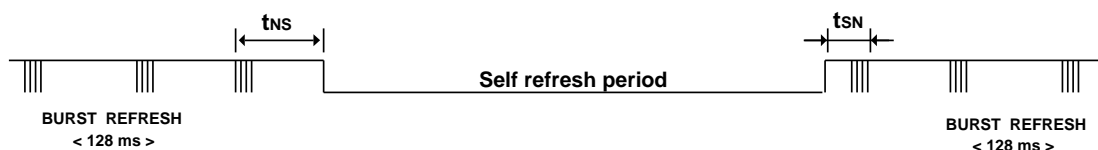
### (1) In case of CBR distributed refresh

The last / first full refresh cycles must be made within t<sub>NS</sub> / t<sub>SN</sub> before / after self refresh , on the condition of t<sub>NS</sub> < 128 ms and t<sub>SN</sub> < 128 ms.



### (2) In case of burst refresh

The last / first full refresh cycles must be made within t<sub>NS</sub> / t<sub>SN</sub> before / after self refresh , on the condition of t<sub>NS</sub> < 16 ms and t<sub>SN</sub> < 16 ms.

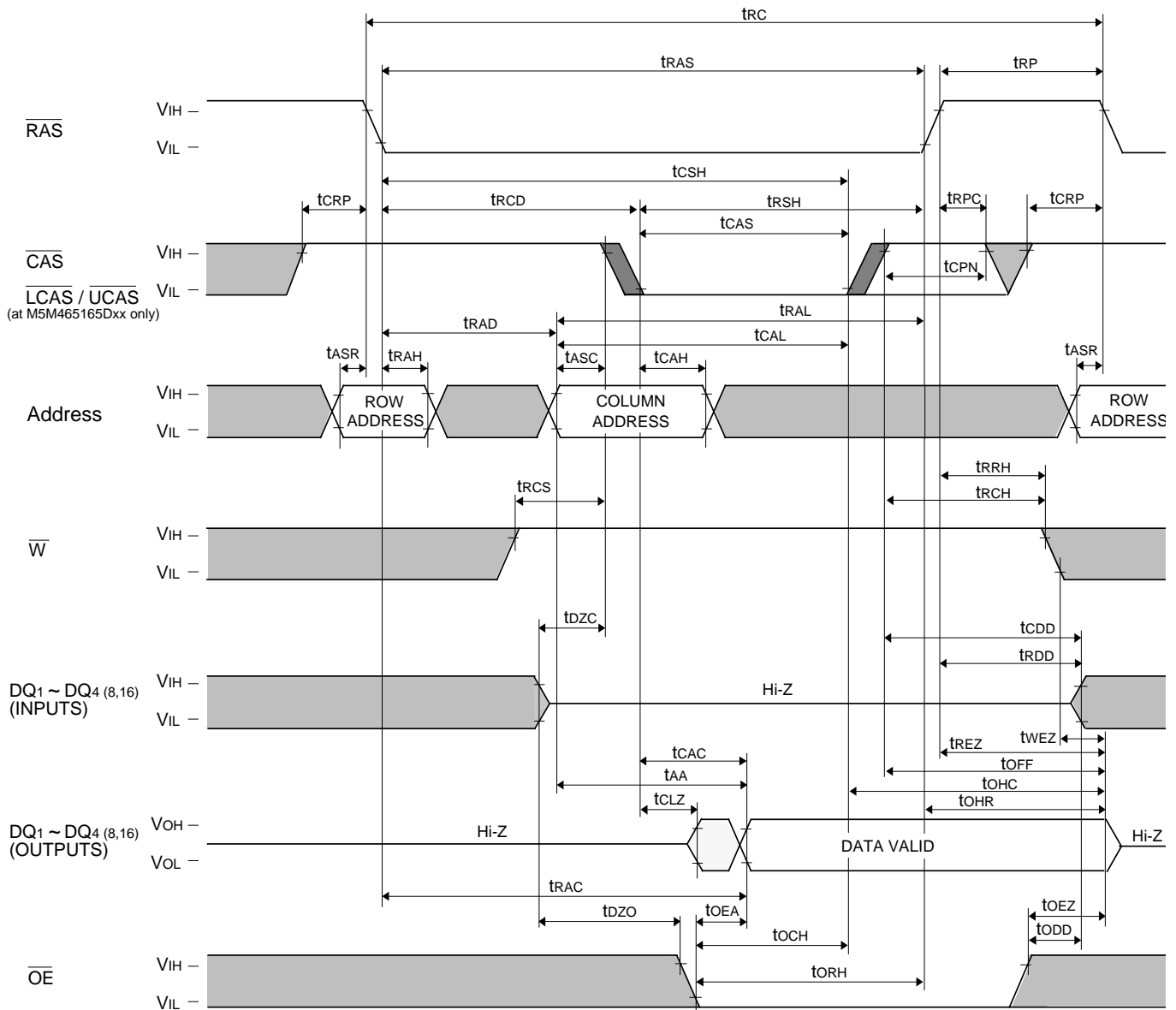


# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## Timing Diagrams (Note 29)

### Read Cycle



Note 29: Indicates the don't care input.  
V<sub>IH</sub>(min) V<sub>IN</sub> V<sub>IH</sub>(max) or V<sub>IL</sub>(min) V<sub>IN</sub> V<sub>IL</sub>(max)

Indicates the invalid output.

Indicates the skew of the two inputs. (at M5M465165Dxx only)





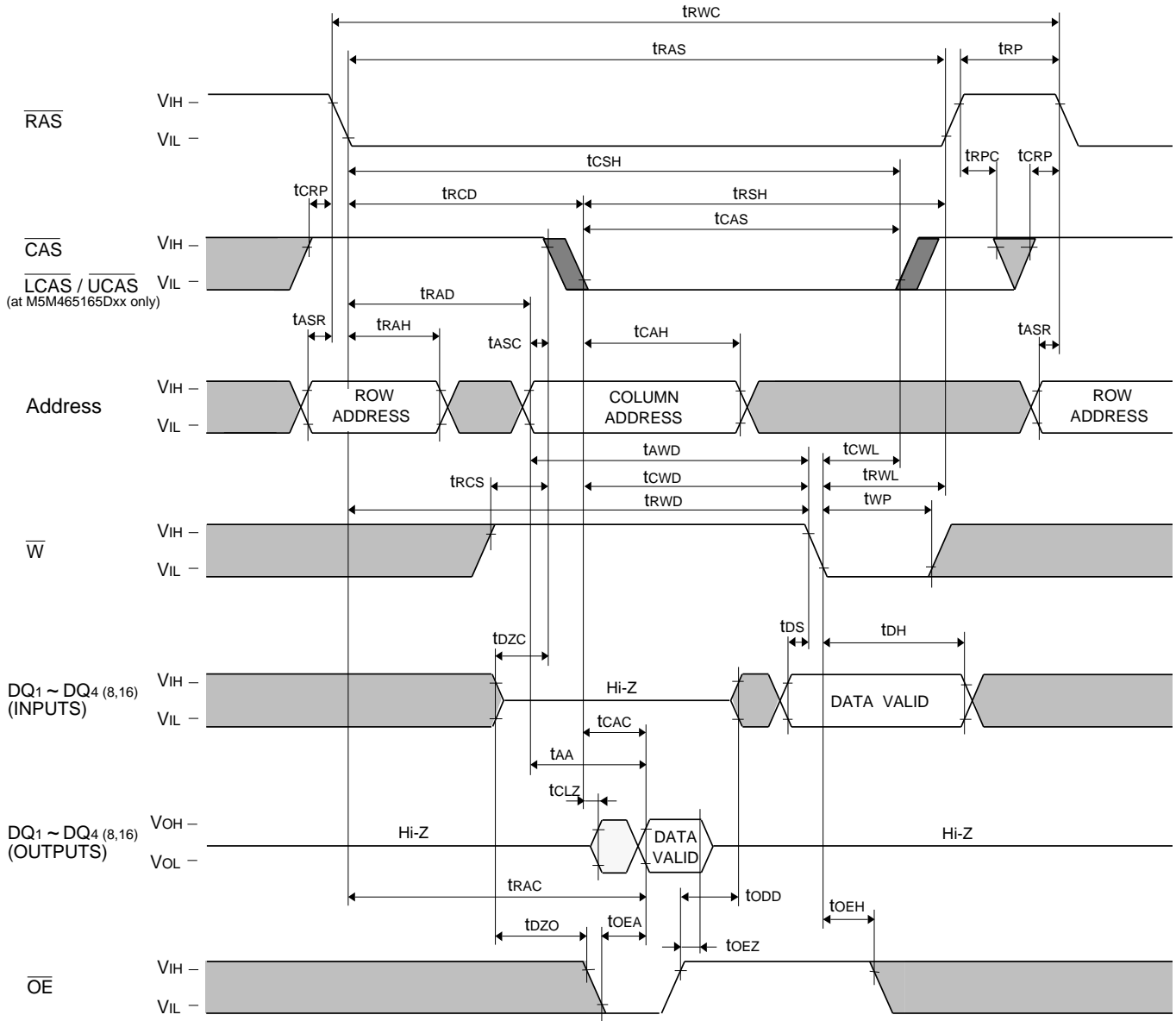




# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## Read-Write, Read-Modify-Write Cycle







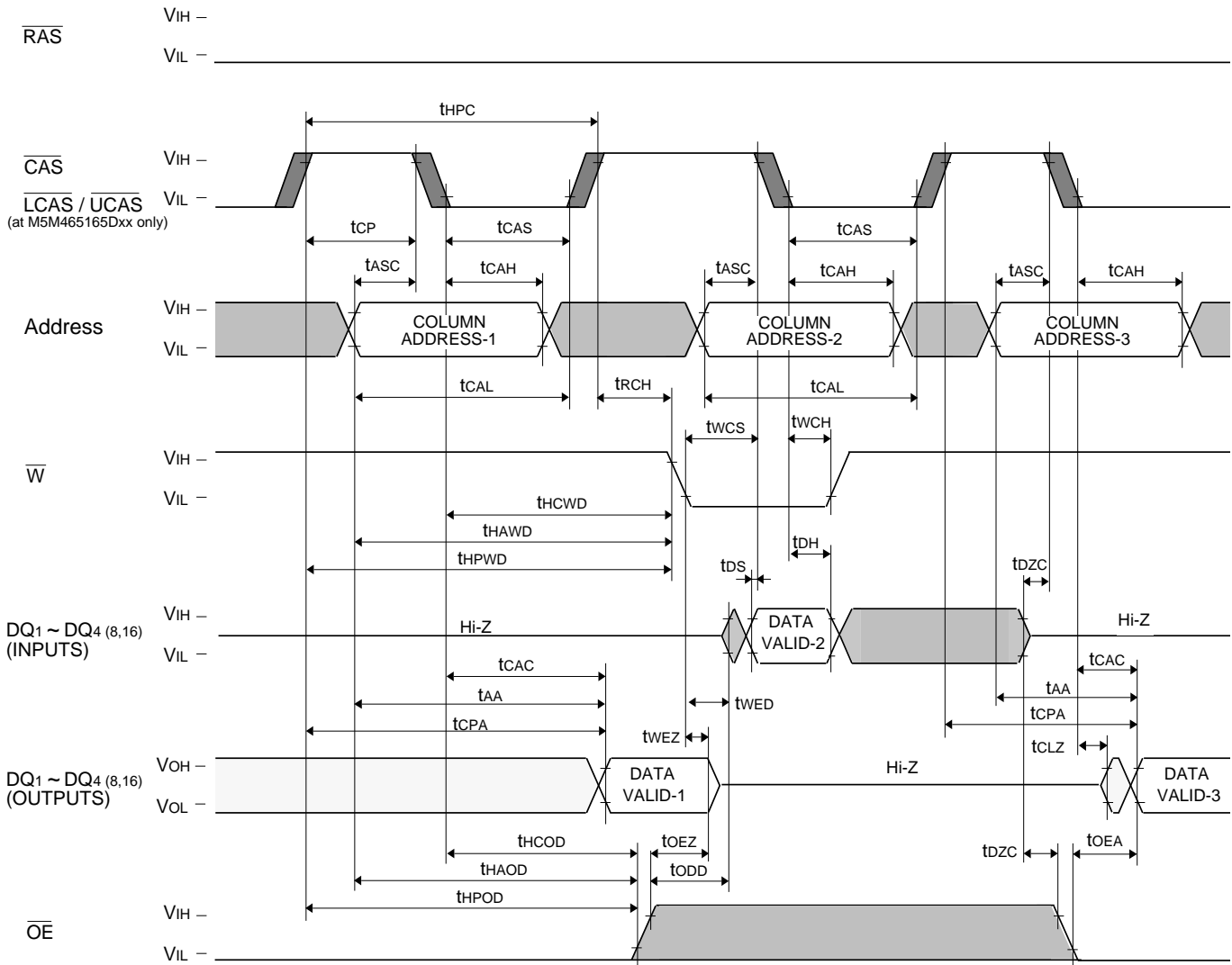




# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## EDO Mode Mix Cycle (2) (Note 30)



Note 30:  $\overline{OE}=L$ ;  $\overline{W}$  Hi-Z control  
 $\overline{OE}=H$ ;  $\overline{OE}$  Hi-Z control





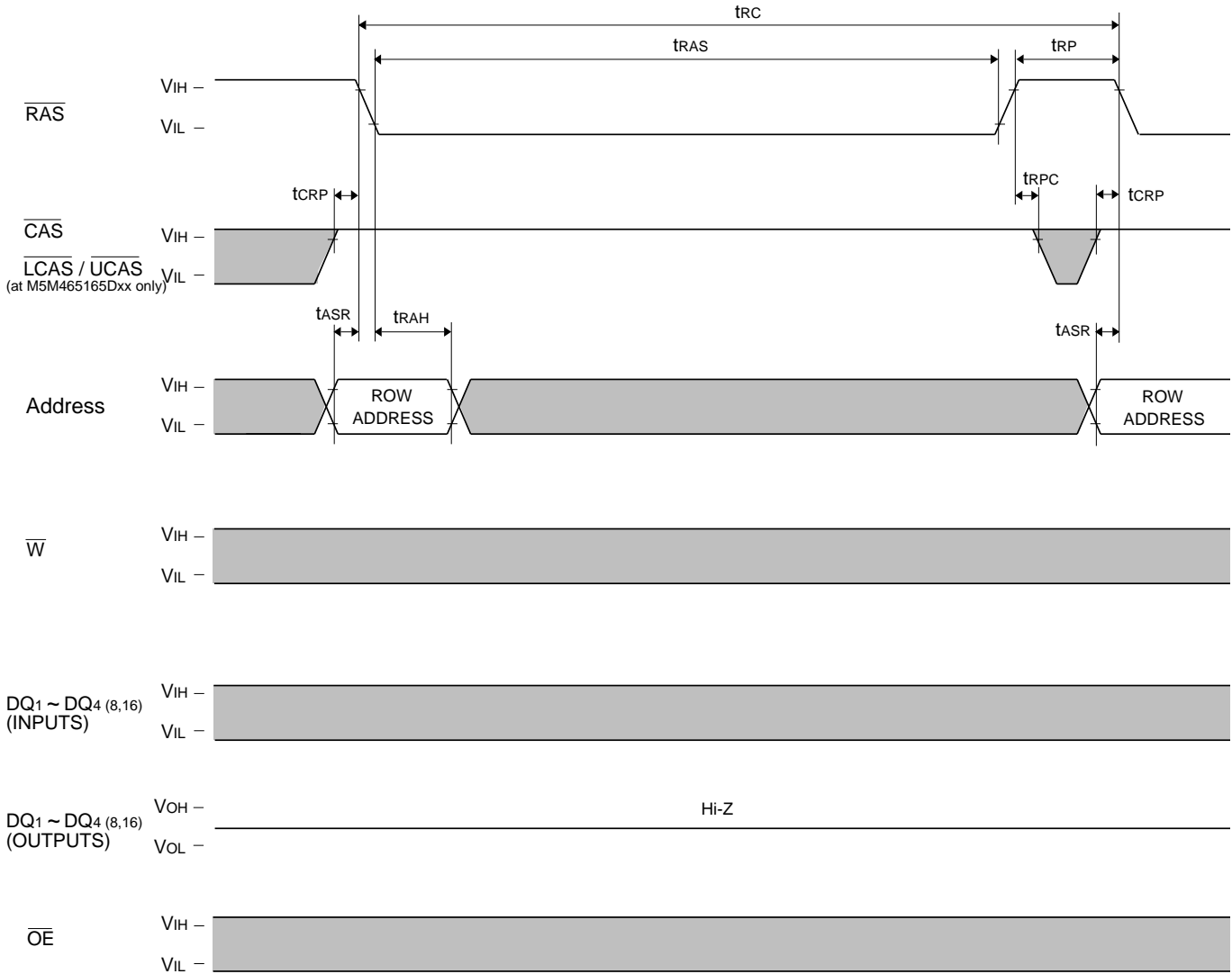




# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

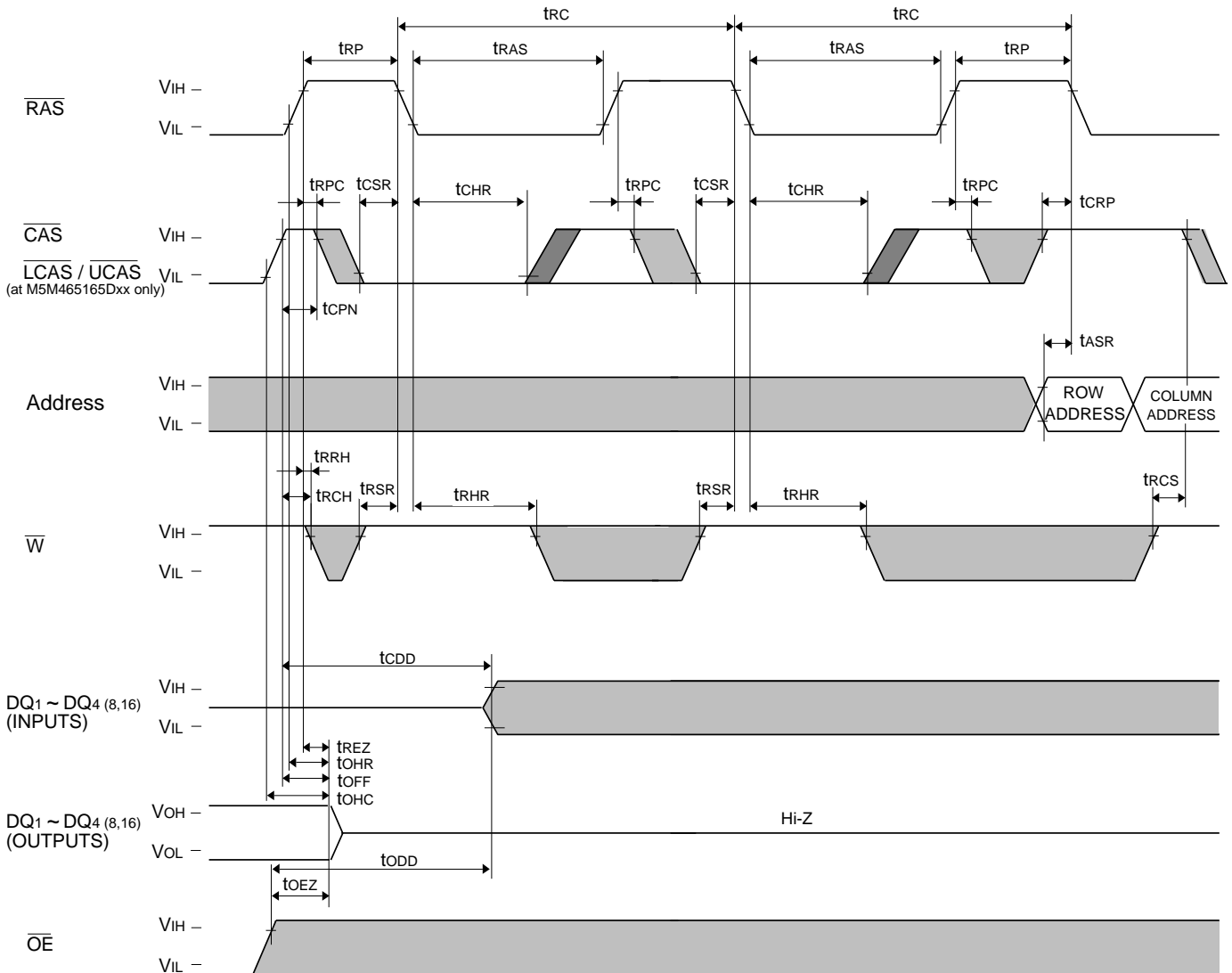
## RAS-only Refresh Cycle



**M5M467405/465405DJ,DTP -5,-6,-5S,-6S**  
**M5M467805/465805DJ,DTP -5,-6,-5S,-6S**  
**M5M465165DJ,DTP -5,-6,-5S,-6S**

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

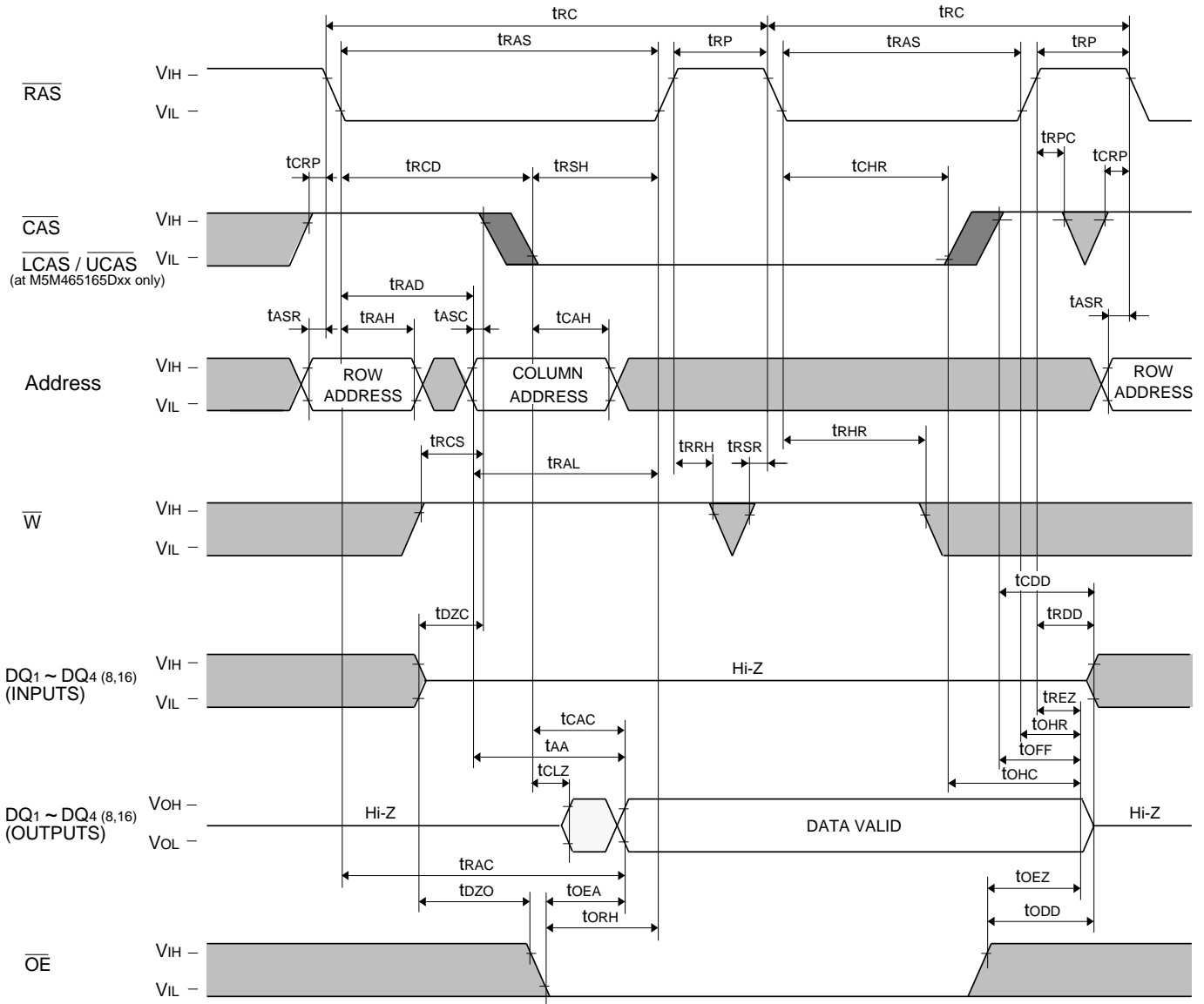
**CAS before RAS Refresh Cycle**



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

### Hidden Refresh Cycle (Read) (Note 31)



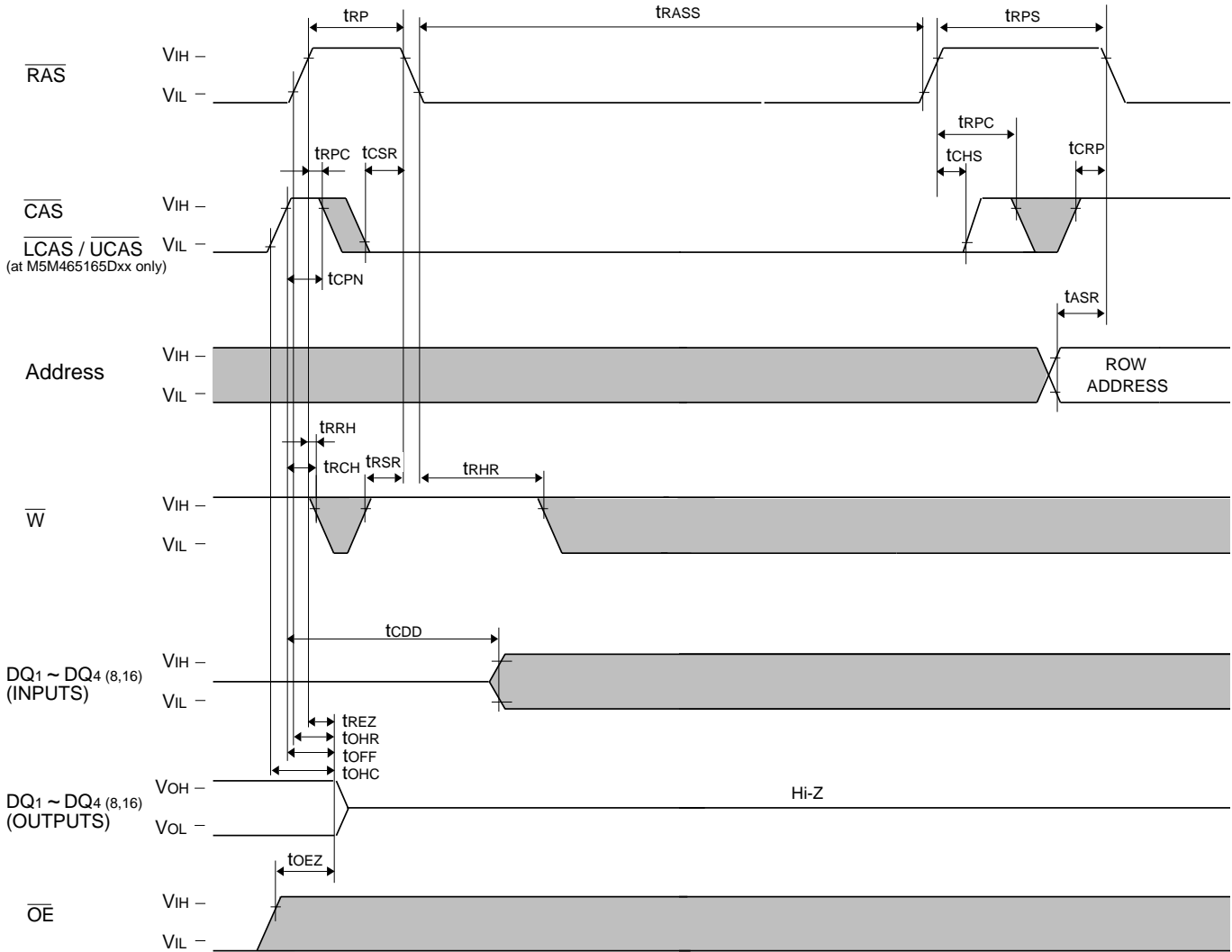
Note 31: Early write, delayed write, read write, or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

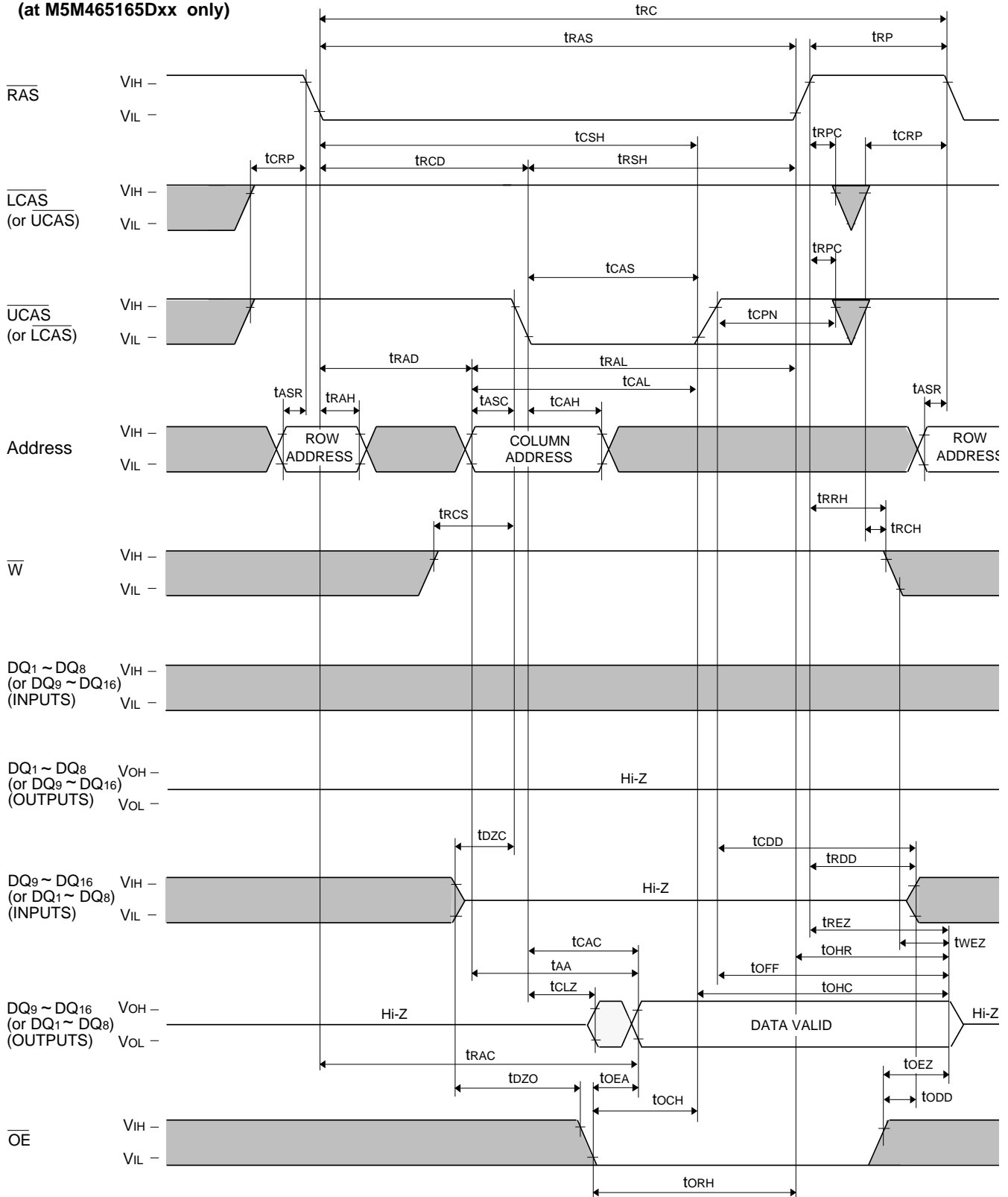
## Self Refresh Cycle



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

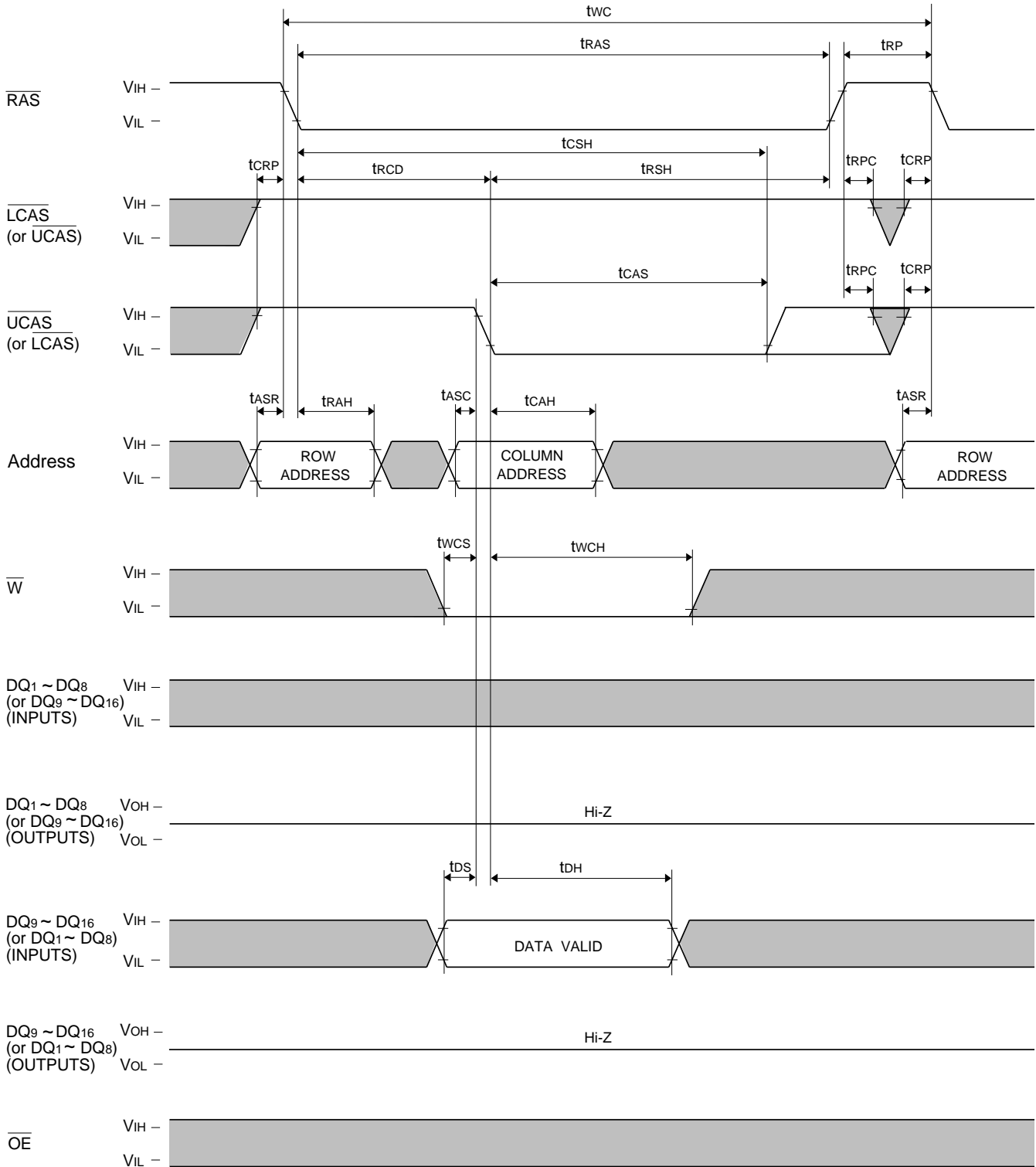
## Upper / (Lower) Byte Read Cycle (at M5M465165Dxx only)



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## Upper / (Lower) Byte Write Cycle (Early Write) (at M5M465165Dxx only)





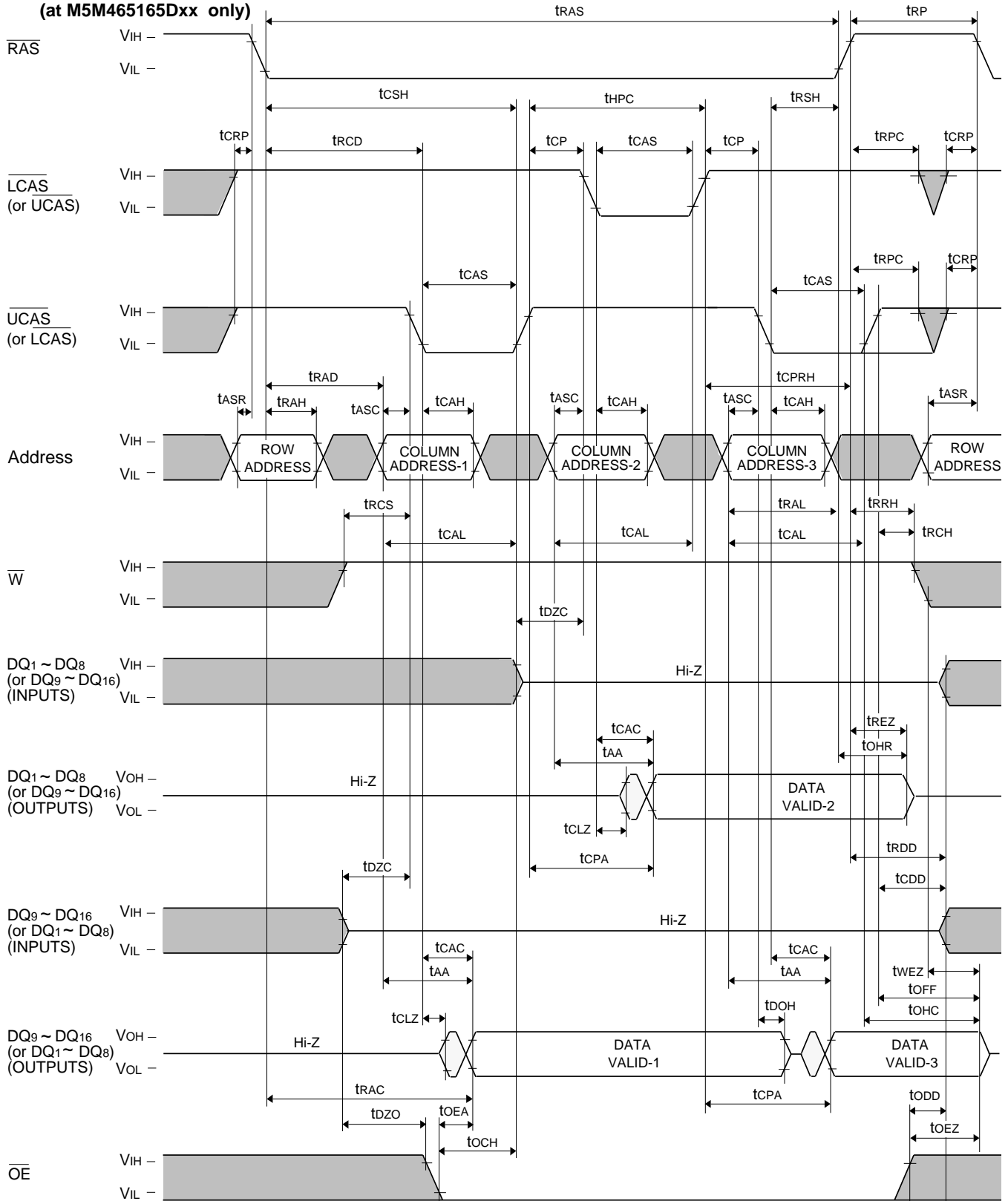




# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

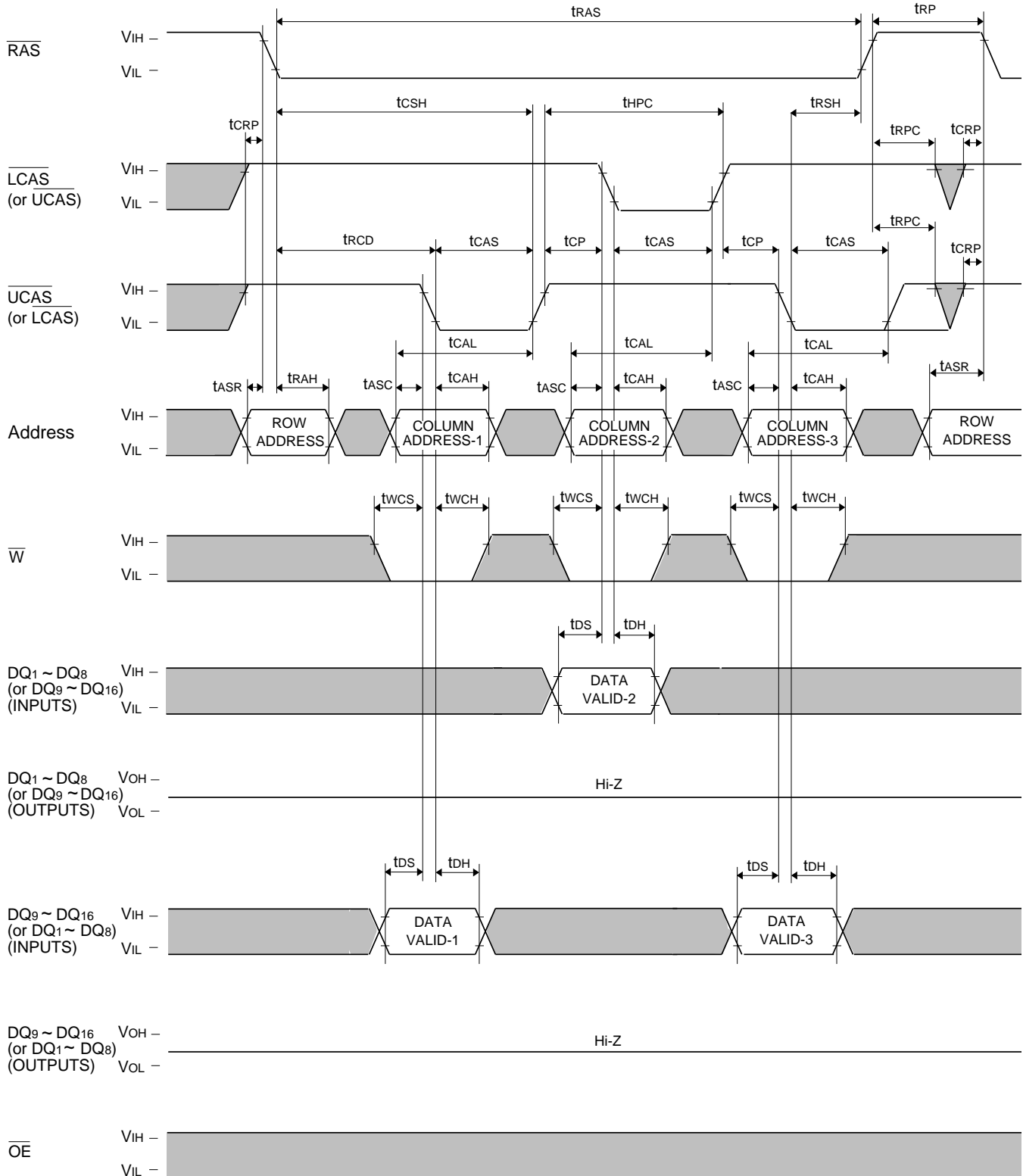
## EDO Mode Byte Read Cycle (at M5M465165Dxx only)



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

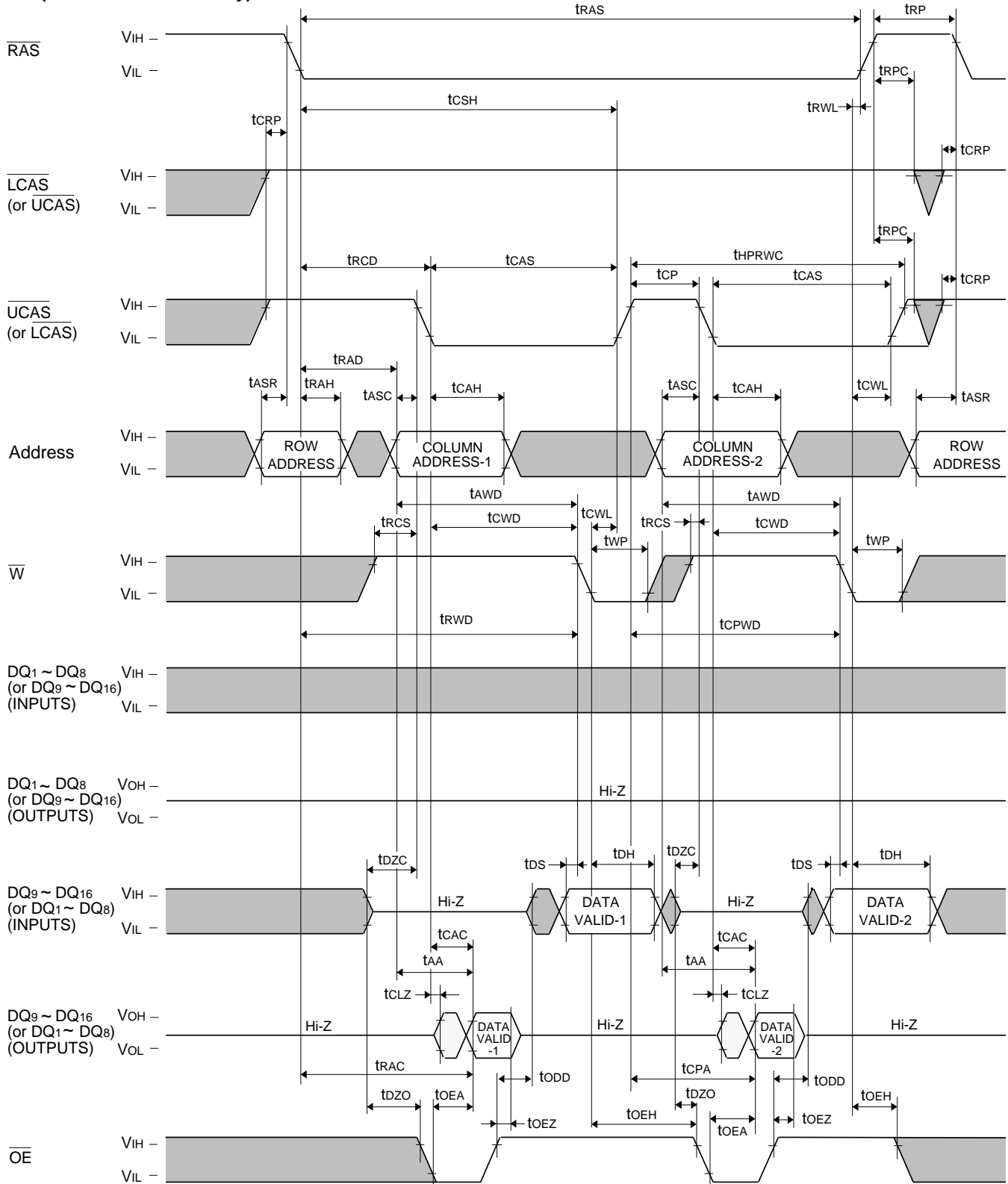
## EDO Mode Byte Write Cycle (Early Write) (at M5M465165Dxx only)



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

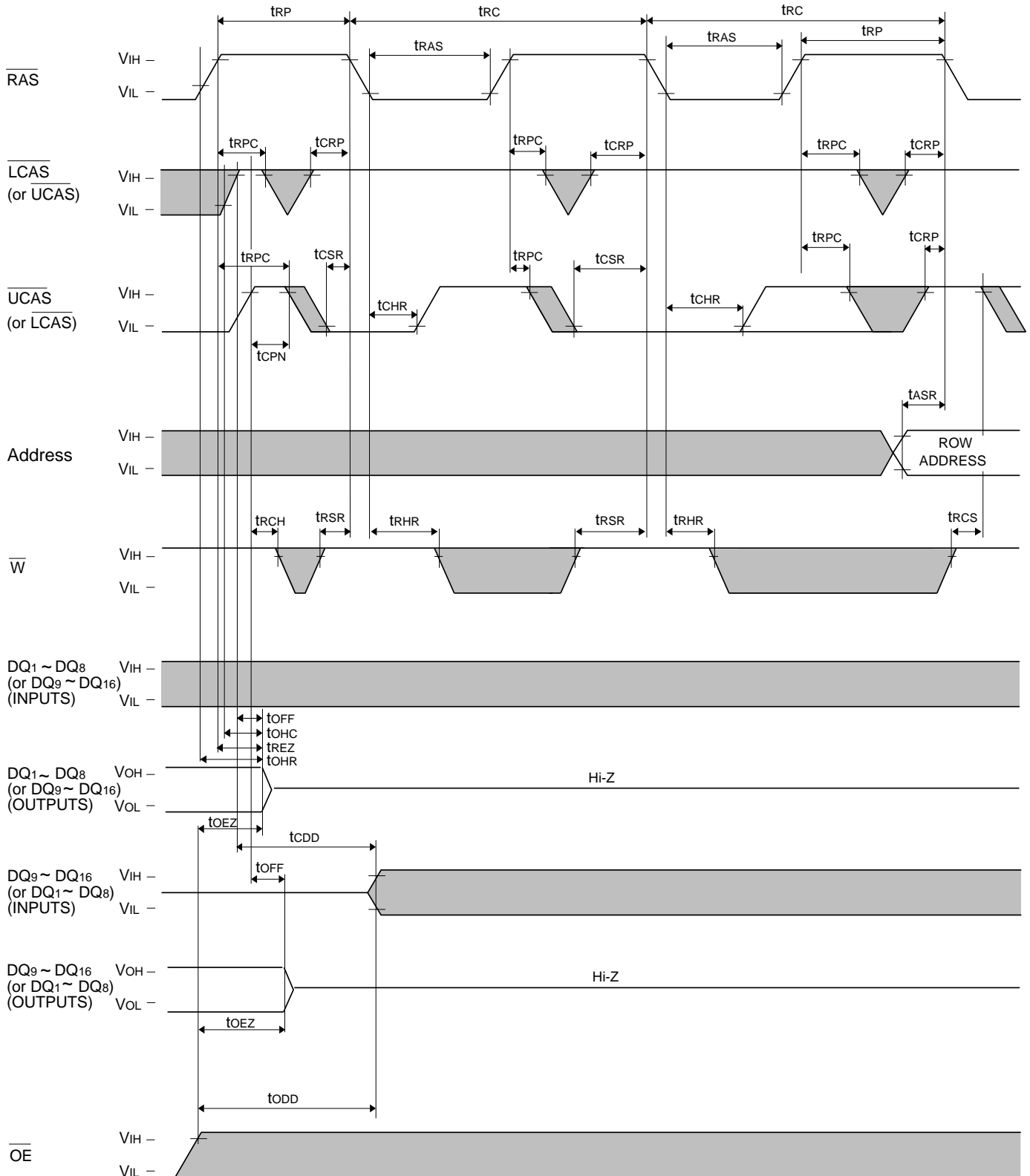
EDO Mode Upper/(Lower) Byte Read-Write, Upper/(Lower) Byte Read-Modify-Write Cycle  
(at M5M465165Dxx only)



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

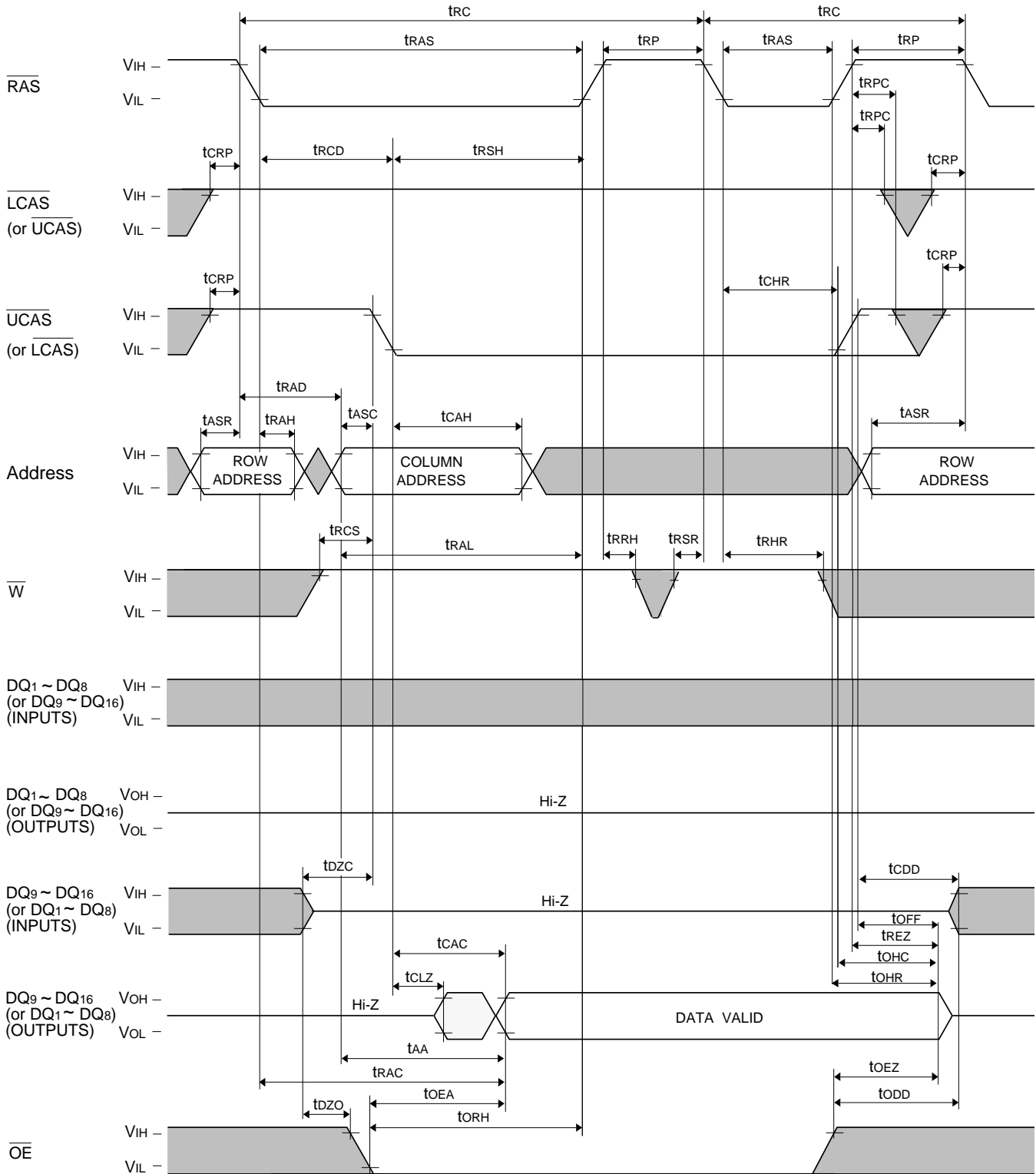
Upper / (Lower) CAS before RAS Refresh Cycle  
(at M5M465165Dxx only)



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

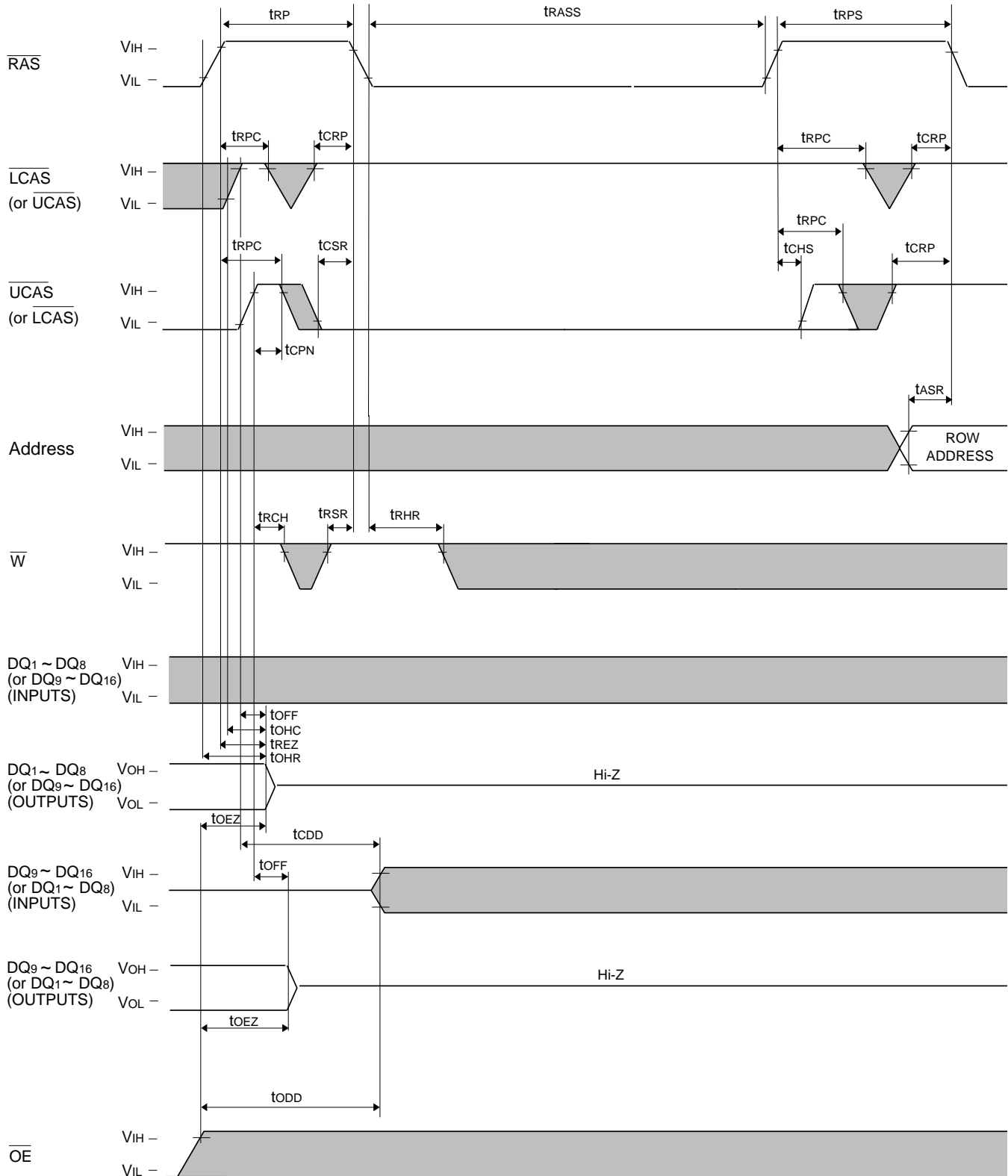
Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 31)  
(at M5M465165Dxx only)



# M5M467405/465405DJ,DTP -5,-6,-5S,-6S M5M467805/465805DJ,DTP -5,-6,-5S,-6S M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

## Byte Self Refresh Cycle (at M5M465165Dxx only)



**M5M467405/465405DJ,DTP -5,-6,-5S,-6S**  
**M5M467805/465805DJ,DTP -5,-6,-5S,-6S**  
**M5M465165DJ,DTP -5,-6,-5S,-6S**

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM  
 EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

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