

Linear Phase, Group Delay Equalized, 8th Order Lowpass Filter

DESCRIPTION

The LTC1264-7M/883 is a clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband and exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency the filter attains 28dB attenuation (vs 12dB for Bessel), while at three times the cutoff frequency the filter attains 55dB attenuation (vs 30dB for Bessel). The cutoff frequency of the LTC1264-7M/883 is tuned via an external TTL or CMOS clock.

The clock-to-cutoff frequency ratio of the LTC1264-7 can be set to 25:1 (pin 10 to V^+) or 50:1 (pin 10 to V^-).

When the filter operates at clock-to-cutoff frequency ratio of 25:1, the input is double-sampled to lower the risk of aliasing.

The LTC1264-7M/883 is optimized for speed. Depending on the operating conditions, cutoff frequencies between 200kHz and 250kHz can be obtained. (Please refer to the

Passband vs Clock Frequency graphs in the LTC1264-7 standard data sheet.)

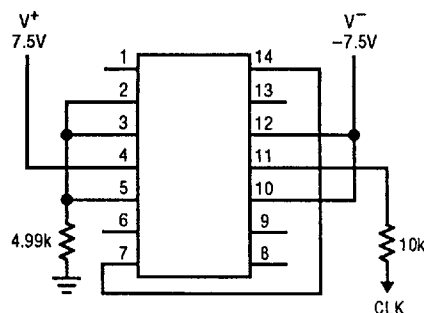
The LTC1264-7M/883 is pin-compatible with the LTC1064-X series.

The device is processed to the requirements of MIL-STD-883 Class B to yield circuits usable in precision military applications.

ABSOLUTE MAXIMUM RATINGS

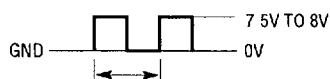
Total Supply Voltage (V^+ to V^-)	16V
Power Dissipation	400mW
Burn-In Voltage	16V
Voltage at Any Input	$(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	-55°C to 125°C
Lead Temperature (Soldering, 10 sec)	300°C

BURN-IN CIRCUIT



NOTES:

1. $T_A = 125^\circ\text{C}$
2. BURN-IN VOLTAGES $V^+ = 7.5\text{V TO } 8\text{V}$
 $V^- = -7.5\text{V TO } -8\text{V}$
3. CLK = SQUARE WAVE,



FREQUENCY = 1kHz $\pm 10\%$

1264-7M/81

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
NC	1	LTC1264-7M/883
V_{IN}	2	
GND	3	PART MARKINGS [†]
V^+	4	
NC	5	LTC1264-7M/883C
LP (A)	6	
R_{IN} (A)	7	
OUT (C)	14	
NC	13	
V^-	12	
f_{CLK}	11	
25/50	10	
V_{OUT}	9	
NC	8	

J PACKAGE
14-LEAD CERAMIC DIP
 $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 65^\circ\text{C/W}$

[†] The suffix letter "C" of the part mark indicates compliance per MIL-STD-883, para 1.2.1.1.

TABLE 1: ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $R_L = 10k$, $f_{CUTOFF} = 100kHz$ or $50kHz$, $f_{CLK} = 2.5MHz$, TTL or CMOS level (maximum clock rise or fall time $\leq 1\mu s$) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS	NOTES	RANGE		SUB-GROUP	UNITS
			MIN	MAX		
Passband Gain	$0.1Hz \leq f \leq 0.25 f_{CUTOFF}$ $f_{TEST} = 25kHz, (f_{CLK}/f_C) = 25:1$		-0.50	0.50	1,2,3	dB
Gain at $0.50 f_{CUTOFF}$ (Note 3)	$f_{TEST} = 50kHz, (f_{CLK}/f_C) = 25:1$	3	-0.50	0.20	1,2,3	dB
	$f_{TEST} = 25kHz, (f_{CLK}/f_C) = 50:1$	3	-0.65	0.30	1,2,3	dB
Gain at $0.75 f_{CUTOFF}$	$f_{TEST} = 75kHz, (f_{CLK}/f_C) = 25:1$		-1.5	0.1	1,2,3	dB
Gain at f_{CUTOFF}	$f_{TEST} = 100kHz, (f_{CLK}/f_C) = 25:1$		-3.7	-1.9	1,2,3	dB
	$f_{TEST} = 50kHz, (f_{CLK}/f_C) = 50:1$		-4.5	-2.3	1,2,3	dB
Gain at $2.0 f_{CUTOFF}$	$f_{TEST} = 200kHz, (f_{CLK}/f_C) = 25:1$		-34	-20	1,2,3	dB
	$f_{TEST} = 100kHz, (f_{CLK}/f_C) = 50:1$		-34	-27	1,2,3	dB
Gain with $f_{CLK} = 20kHz$	$f_{TEST} = 200Hz, (f_{CLK}/f_C) = 50:1$		-0.7	0.1	1	dB
Gain with $f_{CLK} = 400kHz, V_S = \pm 2.375V$	$f_{TEST} = 8kHz, (f_{CLK}/f_C) = 25:1$		-0.2	0.5	1	dB
	$f_{TEST} = 16kHz, (f_{CLK}/f_C) = 25:1$		-3.5	-1.4	1	dB
Gain with $f_{CLK} = 4MHz$	$f_{TEST} = 160kHz, V_{IN} = 1V_{RMS}$ $(f_{CLK}/f_C) = 25:1$			3.0	1,2,3	dB
Phase Factor (F)	$(f_{CLK}/f_C) = 25:1, f \leq f_{CUTOFF}$	1	392	423		
Phase = $180^\circ - F(f/f_C)$	$(f_{CLK}/f_C) = 50:1, f \leq f_{CUTOFF}$	1	374	414	1,2,3	Deg
Phase Nonlinearity	$(f_{CLK}/f_C) = 25:1, f \leq f_{CUTOFF}$	1		± 2.0	1,2,3	%
	$(f_{CLK}/f_C) = 50:1, f \leq f_{CUTOFF}$	1		± 2.0	1,2,3	%
Group Delay (t_d) $t_d = (F/360)(1/f_C)$	$(f_{CLK}/f_C) = 25:1, f \leq f_{CUTOFF}$	2,3	10.9	11.7	1,2,3	μs
	$(f_{CLK}/f_C) = 50:1, f \leq f_{CUTOFF}$	2,3	20.8	22.9	1,2,3	μs
Group Delay Ripple	$(f_{CLK}/f_C) = 25:1, f \leq f_{CUTOFF}$	2		± 2.0	1,2,3	%
	$(f_{CLK}/f_C) = 50:1, f \leq f_{CUTOFF}$	2		± 2.0	1,2,3	%
Input Impedance			30	75	1	k Ω
Output DC Voltage Swing	$V_S = \pm 2.375V$	4	± 1.0		4	V
	$V_S = \pm 5V$	4	± 2.0		4,5,6	V
	$V_S = \pm 7.5V$	4	± 3.0		4,5,6	V
Output DC Offset ($f_{CLK} = 1MHz$)	$25:1, V_S = \pm 5V$			± 220	4	mV
	$50:1, V_S = \pm 5V$			± 220	4	mV
Power Supply Current ($f_{CLK} = 1MHz$)	$V_S = \pm 2.375V$			22	1	mA
				22	2,3	mA
	$V_S = \pm 5V$			25	1	mA
				30	2,3	mA
	$V_S = \pm 7.5V$			30	1	mA
				35	2,3	mA
Power Supply Range			± 2.375	± 7.5	1	V

TABLE 1: ELECTRICAL CHARACTERISTICS

Note 1: Input frequencies, f , are linearly phase shifted through the filter as long as $f \leq f_c$; f_c = cutoff frequency.

Figure 1 curve (A) shows the typical phase response of an LTC1264-7 operating at $f_{CLK} = 2.5\text{MHz}$, $f_c = 100\text{kHz}$. An endpoint straight line, curve (B), depicts the ideal linear phase response of the filter. It is described by: phase shift = $180^\circ - F(f/f_c)$; $f \leq f_c$.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor together with the specified deviation from the ideal straight line allows the calculation of the phase at a given frequency. Note, the maximum phase nonlinearity, Figure 1, occurs at the vicinity of $f = 0.25 f_c$ and $= 0.75 f_c$. Example: The phase shift at 70kHz of the LTC1264-7M/883 shown in Figure 1 is: phase shift = $180^\circ - 407^\circ (70\text{kHz}/100\text{kHz}) \pm \text{nonlinearity} = -104.9^\circ \pm 1\%$ or $-104.9^\circ \pm 1.05^\circ$.

Note 2: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 3: The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_c .

Note 4: The AC swing is typically 9V_{p-p}, 5.6V_{p-p}, 1.8V_{p-p} with $\pm 7.5\text{V}$, $\pm 5\text{V}$, $\pm 2.5\text{V}$ supply respectively. For more information refer to the THD + Noise vs Input graphs in the LTC1264-7 standard data sheet.

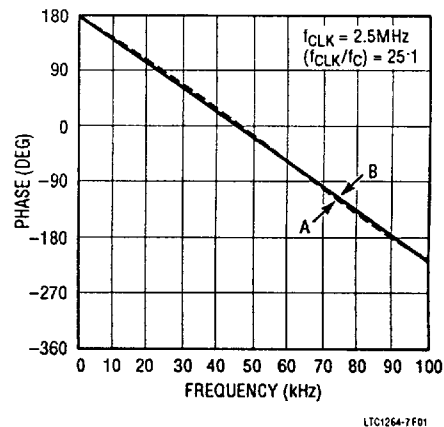


Figure 1. Phase Response in the Passband (Note 1)

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group C and D End Point Electrical Parameters (Method 5005)	1,2,3,4,5,6

* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.