STANDARD MICROSYSTEMS CORPORATION

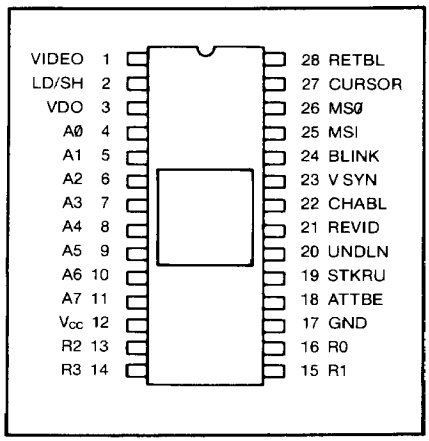
CRT 8021
CRT 8021-003
μPC FAMILY

CRT Video Attributes Controller Video Generator VAC

FEATURES

- ☐ ON CHIP VIDEO SHIFT REGISTER
  Maximum shift register frequency — 20MHz
  Maximum character clock rate — 2.5MHz
- ☐ ON CHIP HORIZONTAL AND VERTICAL RETRACE VIDEO BLANKING
- ☐ ON CHIP GRAPHICS GENERATION
- ☐ ON CHIP ATTRIBUTE LOGIC - CHARACTER, FIELD
  Reverse video
  Character blank
  Character blink
  Underline
  Strike-thru
- ☐ ON CHIP BLINKING CURSOR
- ☐ ON CHIP DATA BUFFER
- ☐ ON CHIP ATTRIBUTE BUFFER
- ☐ +5 VOLT OPERATION
- ☐ TTL COMPATIBLE
- ☐ MOS N-CHANNEL SILICON-GATE COPLAMOS® PROCESS

PIN CONFIGURATION



- ☐ COMPATIBLE WITH CRT 5027/37 VTAC® AND CRT 9007 VPAC

GENERAL DESCRIPTION

The SMC CRT 8021 Video Attributes Controller (VAC) is an n-channel COPLAMOS® MOS/LSI device. It contains wide and thin graphics logic, attributes logic, a data latch, field and character attribute latch, a blinking cursor, and a high speed video shift register. The CRT 8021 VAC is a companion to SMC's CRT 5027/37 VTAC® or CRT 9007 VPAC. The CRT 8021 and a character ROM combined with either a CRT 5027/37 or a CRT 9007 comprises the major circuitry required for the display portion of a CRT video terminal.

The CRT 8021 video output may be connected directly to a CRT monitor video input. The CRT 5027/37 or CRT 9007 blanking output can be connected directly to the CRT 8021 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

A blinking cursor is available on the CRT 8021. There is a separate cursor blink rate which is twice the character blink rate and has a duty cycle of 50/50.

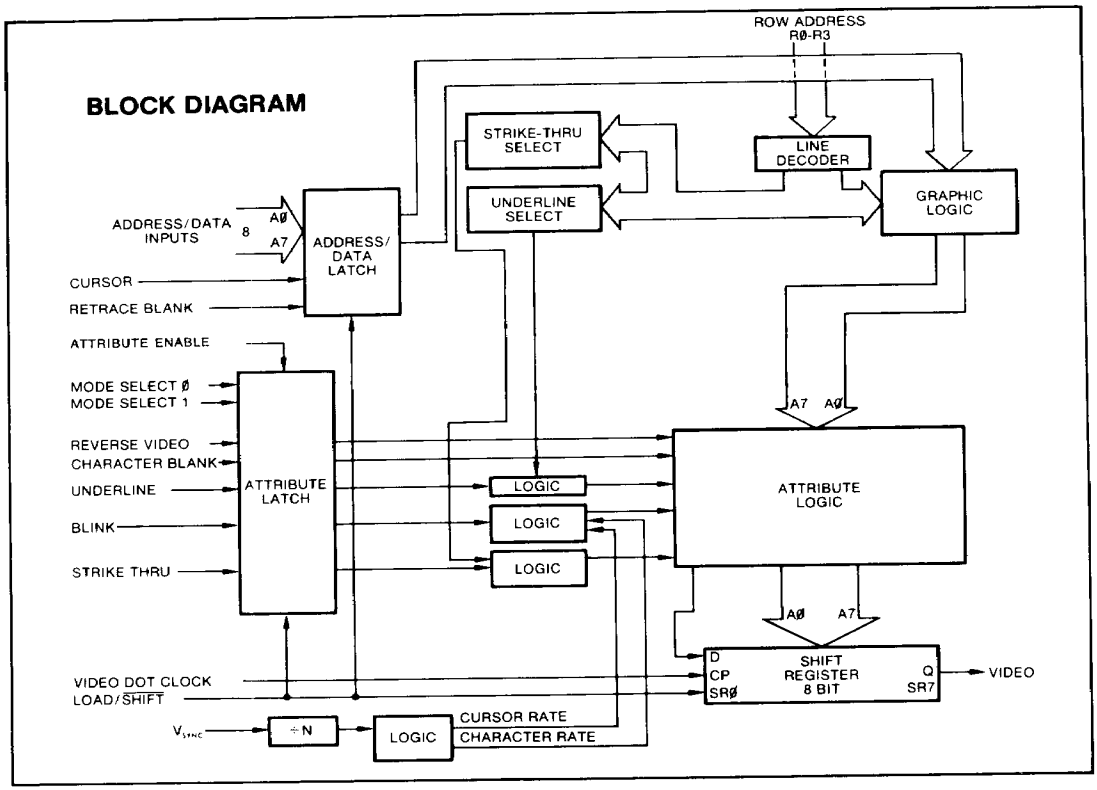
The CRT 8021 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions. These attributes are available in all modes.

The thin graphic mode enables the user to create single line drawings and forms.

In the wide graphic mode the CRT 8021 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing 256 unique graphic symbols. Thus, the CRT 8021 can produce either alphanumeric symbols or various graphic entities depending on the mode selected. The mode can be changed on a per character basis.

The CRT 8021 is available in two versions. The CRT 8021 provides an eight-part graphic entity which fills the character block. The CRT 8021 is designed for seven dot wide, nine or eleven dot high characters in nine by twelve or ten by twelve character blocks.

The CRT 8021-003 provides a six part graphic entity for five by seven or five by nine characters in character blocks of up to seven by ten dots.



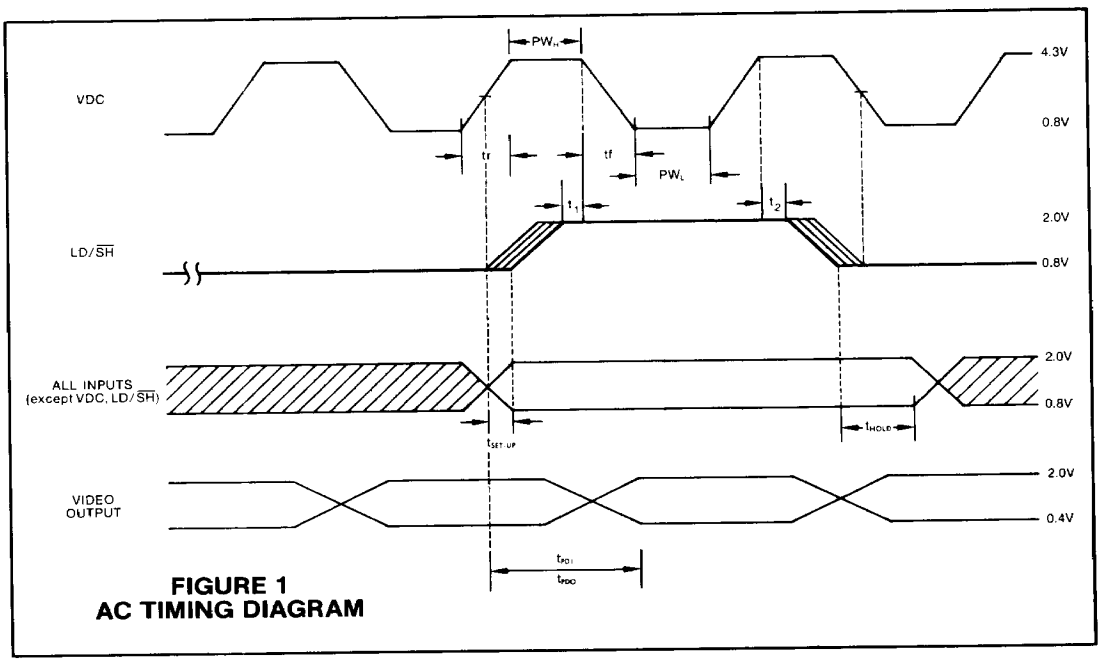


FIGURE 1
AC TIMING DIAGRAM

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See Figure 7
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 0.4$ mA, 74LSXX load
High-level, V_{OH}	2.4			V	$I_{OH} = -20\,\mu A$
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \le V_{IN} \le V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \le V_{IN} \le V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/$\overline{SH}$		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

SYMBOL	PARAMETER	CRT 8021		UNITS
		MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	MHz
PW_H	VDC—High Time	15.0		ns
PW_L	VDC—Low Time	15.0		ns
t_{CY}	LD/$\overline{SH}$ cycle time	400		ns
t_r, t_f	Rise, fall time		10	ns
t_{SET-UP}	Input set-up time	≥0		ns
t_{HOLD}	Input hold time	15		ns
t_{PDI}, t_{PDO}	Output propagation delay	15	50	ns
t_1	LD/$\overline{SH}$ set-up time	10		ns
t_2	LD/$\overline{SH}$ hold time	5		ns

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1	VIDEO	Video Output	O	The video output contains the dot stream for the selected row of the wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs. The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4. When the next Load/$\overline{\text{Shift}}$ pulse appears the next character via the attribute logic, is parallel loaded into the shift register and the cycle repeats.
2	LD/$\overline{\text{SH}}$	Load/$\overline{\text{Shift}}$	I	The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (A0-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 1.
3	VDC	Video Dot Clock	I	Frequency at which video is shifted.
4-11	A0-A7	Address/Data	I	In the External Mode, A0-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Mode A0-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode A0-A2 is used to define the 3 line segments.
12	V_{CC}	Power Supply	PS	+5 volt power supply.
13, 14, 15, 16	R2, R3, R1, R0	Row Address	I	These 4 binary inputs define the row address in the current character block.
17	GND	Ground	GND	Ground
18	ATTBE	Attribute Enable	I	A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select 0, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 1.
19	STKRU	Strike-Thru	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SR0-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). The strike-thru is a double line on rows R5 and R6 for the CRT 8021 and a single line on row R4 for the CRT 8021-003.
20	UNDLN	Underline	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SR0-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). The underline is a single line of R11 for the CRT 8021 and a single line on R8 for the CRT 8021-003.
21	REVID	Reverse Video	I	When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.
22	CHABL	Character Blank	I	When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.
23	V SYNC	V SYNC	I	This input is used as the clock input for the two on-chip blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle).
24	BLINK	Blink	I	When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The character blink rate is 1.875 Hz when V SYNC = 60 Hz.
25 26	MS1 MS0	Mode Select 1 Mode Select 0	I I	These 2 inputs define the three modes of operation of the CRT 8002 as follows: Thin Graphics Mode — In this mode A0-A2, (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 6. Character Mode — In this mode the inputs A0-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3. Wide Graphics Mode — In this mode the inputs A0-A7 will define a graphic entity as described in figure 5. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs R0 to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory. These 3 modes can be intermixed on a per character basis.
27	CURSOR	Cursor	I	When this input is enabled the cursor will be activated. The cursor will be a blinking (at 3.75 Hz when V SYNC = 60 Hz) reverse video block. In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video.
28	RETBL	Retrace Blank	I	When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/$\overline{\text{Shift}}$ pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.

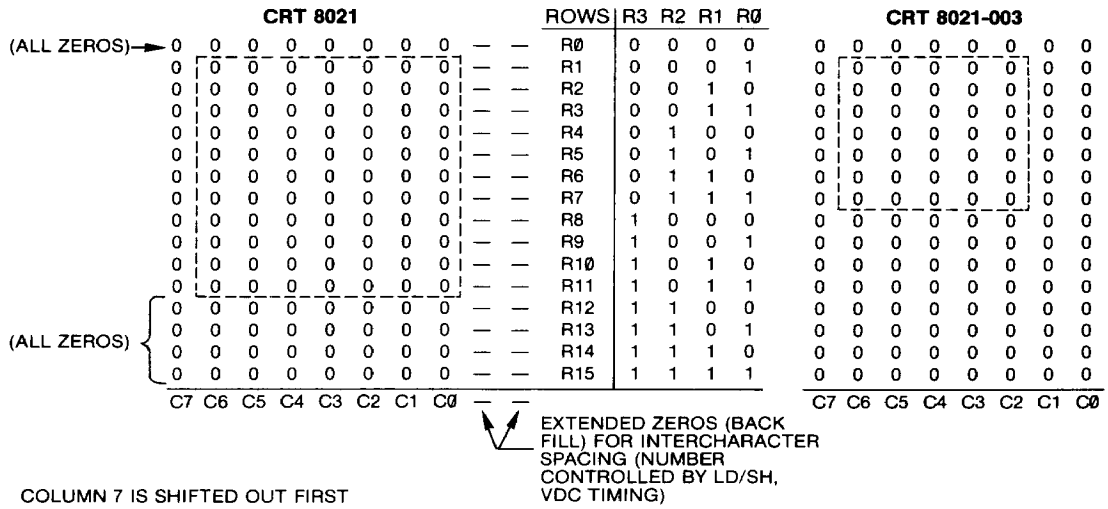
MS1	MS0	MODE
1	0	Thin Graphics
0	1	Character Mode
0	0	Wide Graphics

TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" (S.R.) All
0	0	0	0	0	D (S.R.) All
0	0	0	0	1	"1" (S.R.)*
					D (S.R.) All others
0	0	0	1	X	"0" (S.R.) All
0	0	1	0	0	$\overline{D}$ (S.R.) All
0	0	1	0	1	"0" (S.R.)*
					$\overline{D}$ (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Blink** REVID Block	0	0	0	0	Alternate Normal Video/REVID At Cursor Blink Rate
Blink** REVID Block	0	0	0	1	
Blink** REVID Block	0	0	1	X	
Blink** REVID Block	0	1	0	0	
Blink** REVID Block	0	1	0	1	
Blink** REVID Block	0	1	1	X	

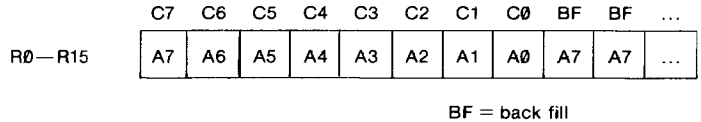
*At Selected Row Decode **At Cursor Blink Rate
Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate

FIGURE 2
TYPICAL CHARACTER MODE BLOCK FORMATS



Note: Dotted line shows typical character display area.

FIGURE 3
CHARACTER MODE
MSØ = 1 MS1= Ø



BF = back fill

FIGURE 4. TYPICAL VIDEO OUTPUT—CHARACTER MODE

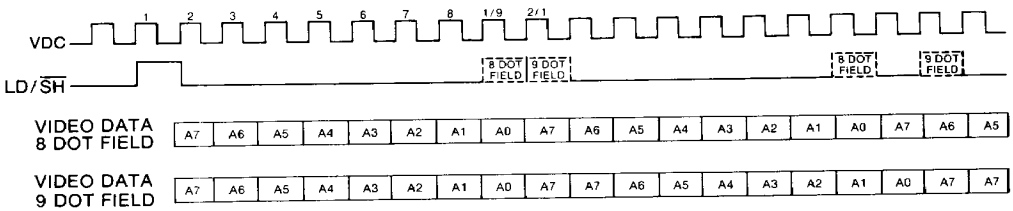
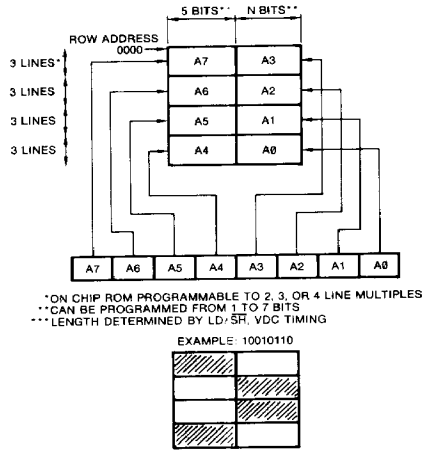
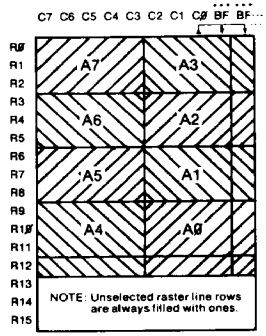


FIGURE 5
WIDE GRAPHICS MODE
MS0 = 0 MS1 = 0



CRT 8021



CRT 8021-003

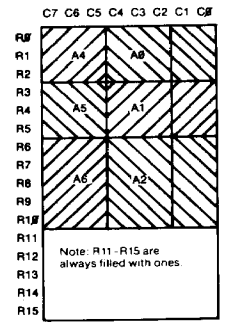
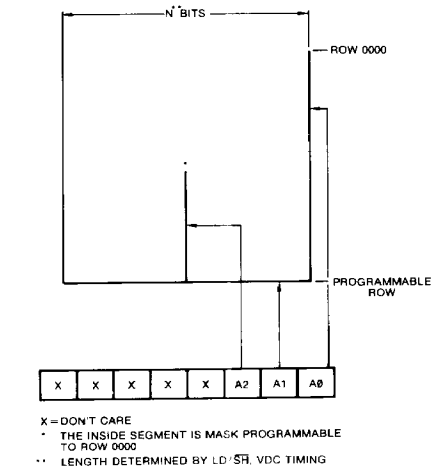
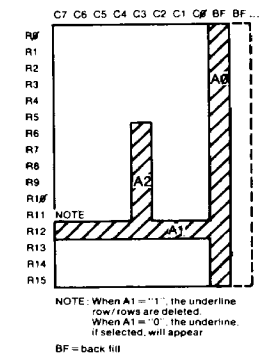


FIGURE 6
THIN GRAPHICS MODE
MS0 = 0 MS1 = 1



CRT 8021



CRT 8021-003

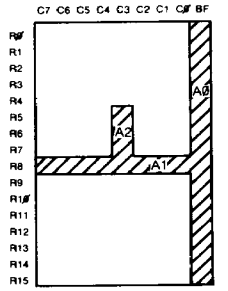


FIGURE 7

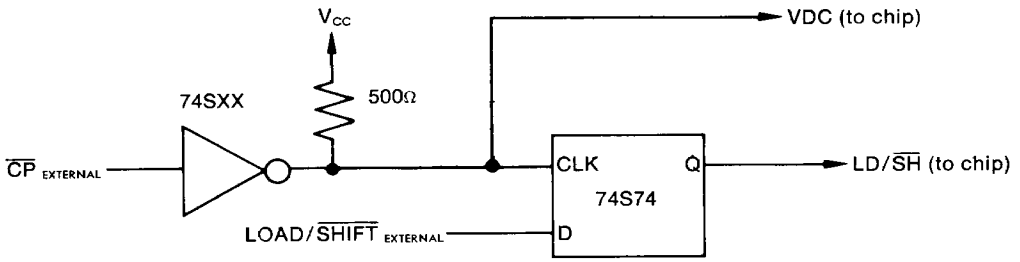
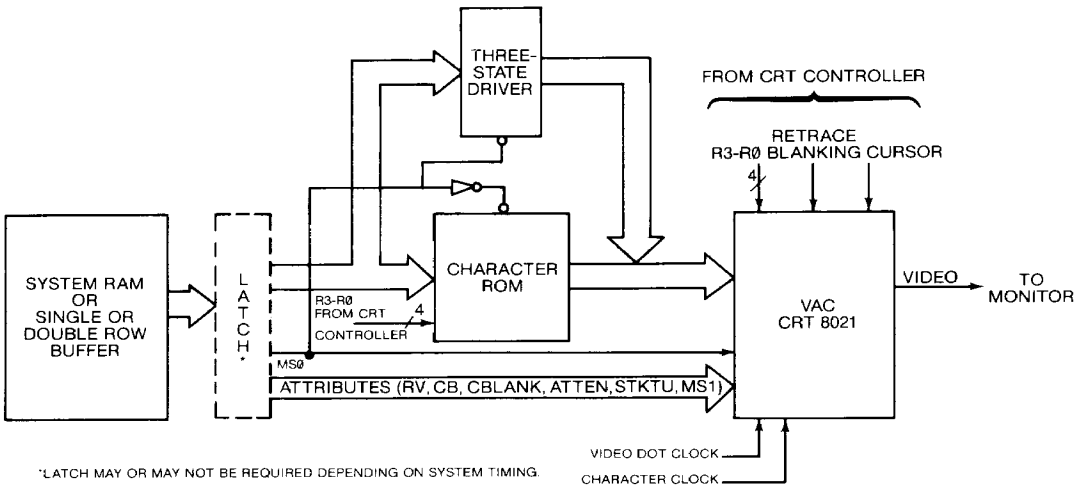


FIGURE 8
TYPICAL CRT 8021 CONFIGURATION FOR COMBINED CHARACTER AND GRAPHICS MODES



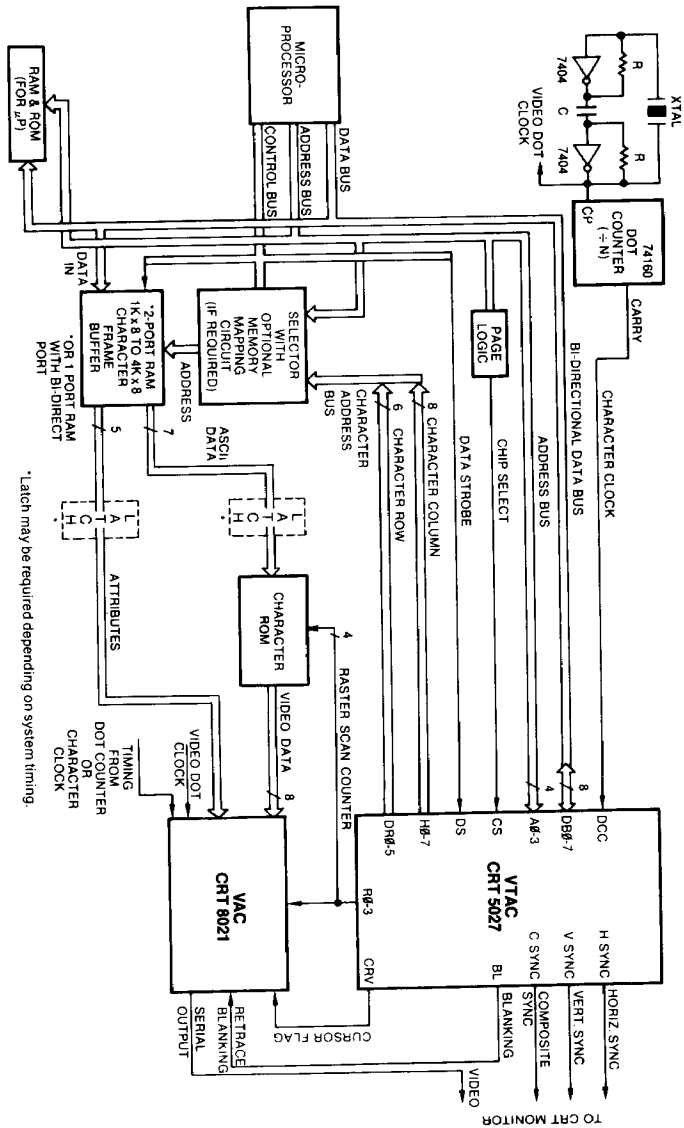


FIGURE 9. CRT 8021 TYPICAL μP CONFIGURATION (CHARACTER MODE ONLY)