National Semiconductor

CGS54C/74C2525 • CGS54CT/74CT2525
CGS54C/74C2526 • CGS54CT/74CT2526
1-to-8 Minimum Skew Clock Driver

The CGS 'C/CT2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The '2525 is designed to distribute a single clock to eight separate receivers with low skew across all outputs during both the t_{PLH} and t_{PHL} transitions. The '2526 is similar to the '2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

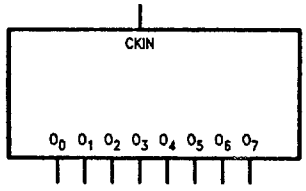
Features

- These CGS devices implement National's FACT™ family
- Ideal for signal generation and clock distribution
- Guaranteed pin to pin and part to part skew
- Multiplexed clock input ('2526)
- Guaranteed 2000V minimum ESD protection
- Symmetric output current drive of 24 mA for I_{OL}/I_{OH}
- 'CT has TTL-compatible inputs
- These products are identical to 74AC/ACT2525 and 2526

Ordering Code: See Section 5

Logic Symbols

'2525



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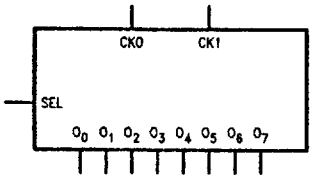
'2526



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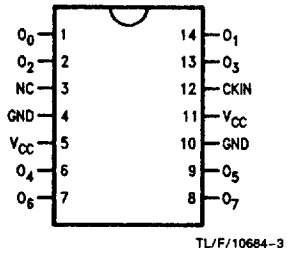
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC

'2525



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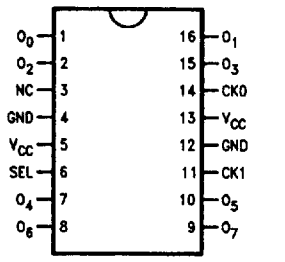
'2526



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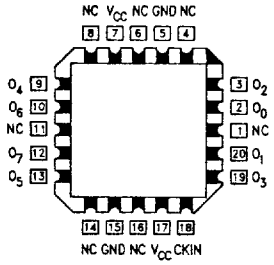
Pin Assignment for LCC

'2525



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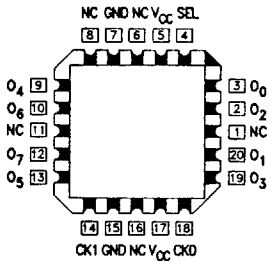
'2526



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Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when either the multiplexed ('2526) or the straight ('2525) clock distribution chip is selected.

Pin Description

Pin Names	Description
CK_{IN}	Clock Input ('2525)
CK_0, CK_1	Clock Inputs ('2526)
O_0–O_7	Outputs
SEL	Clock Select ('2526)

Truth Tables

'2525

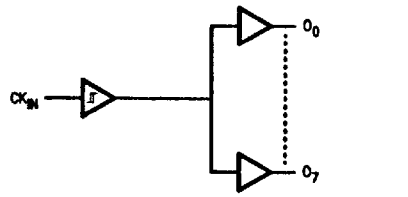
Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'2526

Inputs			Outputs
CK_0	CK_1	SEL	O_1–O_7
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

L = Low Voltage Level
H = High Voltage Level
X = Immaterial

'2525



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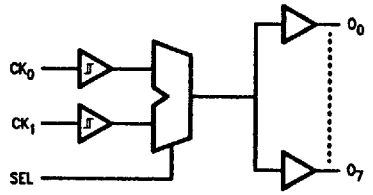
'2526



TL/F/10684–8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+0.2 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = 0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 MA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of CGS circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'C	2.0V to 6.0V
'CT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
CGS74C/CT	−40°C to +85°C
CGS54C/CT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'C Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'CT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for CGS54C/74C Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74C T_A = +25°C	CGS54C T_A = −55°C to +125°C	CGS74C T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		
		5.5		4.86	4.7		I_{OH} −24 mA
					2.46		
					3.76		
					4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.40	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		
		5.5		0.36	0.50		I_{OL} 24 mA
					0.44		
					0.44		
					0.44		24 mA

*All outputs loaded, thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for CGS54C/74C Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	CGS74C $T_A = +25°C$		CGS54C $T_A = -55°C$ to $+125°C$	CGS74C $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for CGS54C @ 25°C is identical to CGS74C @ 25°C.

DC Electrical Characteristics for CGS54CT/74CT Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74CT $T_A = +25°C$		CGS54CT $T_A = -55°C$ to $+125°C$	CGS74CT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded, thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for CGS54CT @ 25°C is identical to CGS74CT @ 25°C

AC Electrical Characteristics

Symbol	Parameter		V_{CC}* (V)	CGS74C $T_A = +25°C$ $C_L = 50$ pF			CGS54C $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74C $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)		3.3 5.0	3.0 3.2	6.5 5.0	11.0 7.8	3.0 2.5	11.0 8.2	3.0 2.9		12.5 8.1	ns
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)		3.3 5.0	3.0 3.6	7.0 5.5	13.0 7.8			3.0 3.3		14.0 8.6	ns
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		3.3 5.0	3.0 4.0	8.0 6.5	14.0 8.5			3.0 3.5		15.0 9.5	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3 5.0		0.3 0.2	1.0 0.7		1.5 1.0			1.0 0.7	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3 5.0		0.3 0.2	1.0 0.7		1.5 1.0			1.0 0.7	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0		1.5 1.0			1.0	ns
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	'C2525 'CT2525 'C2526	5.0			3.5		4.0				ns
		'CT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0		4.0			3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the CLK to Q propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)	5.0	4.6	6.5	9.0			4.0	10.1	ns
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)	5.0	5.8	8.5	11.1			5.1	12.4	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		5.0	5.1	8.5	12.4			4.4		14.1	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0					1.0	ns
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	AC2525 ACT2525 AC2526	5.0			3.5						ns
		ACT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0					3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance ('2525)	820 pF−1.2 x 10^{-18} (f)*	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance ('2526)	820 pF−1.2 x 10^{-18} (f)*	pF	V_{CC} = 5.0V

*f = frequency

Recommended Maximum Power Dissipation (W)

LFPM	T_A = 25°C		T_A = 85°C	
	PDIP	SOIC	PDIP	SOIC
0	1.105	0.858	0.528	0.41
225	1.493	1.055	0.714	0.504
500	1.71	1.210	0.820	0.578