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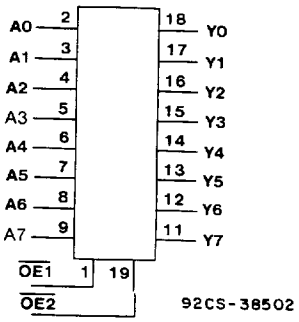
CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Buffer and Line Drivers, 3-State

Type Features:

- *540 Inverting*
- *541 Non-Inverting*
- *Buffered Inputs*
- *3-State Outputs*
- *Bus Line Driving Capability*
- *Typical Propagation Delay = 9 ns @ V_{CC} = 5 V, C_L = 15pF, T_A = 25° C*

The Harris CD54/74HC540 and CD54/74HCT540 are Inverting Octal Buffers and Line Drivers with 3-State Outputs and the capability to drive 15 LSTTL loads. The Harris CD54/74HC541 and CD54/74HCT541 are Non-Inverting Octal Buffers and Line Drivers with 3-State Outputs that can drive 15 LSTTL loads. The Output Enables ($\overline{OE1}$) and ($\overline{OE2}$) control the 3-State Outputs. If either $\overline{OE1}$ or $\overline{OE2}$ is HIGH the outputs will be in the high impedance state. For data output $\overline{OE1}$ and $\overline{OE2}$ both must be LOW.

The CD54HC540, CD54HC541 and CD54HCT540, CD54HCT541 devices are supplied in 20-lead ceramic dual-in-line package (F suffix). The CD54HC540, CD54HC541 and CD54HCT540, CD54HCT541 devices are supplied in 20-lead dual-in-line plastic package (E suffix) and in 20-lead dual-in-line surface mount plastic package (M suffix), and 20 lead dual-in-line shrink small outline plastic package (SM suffix). All types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  -55 to +125°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	An	HC/HCT540	HC/HCT541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5V$) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5V$) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5V$) ..... ±35mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}) ..... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E, F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E, F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

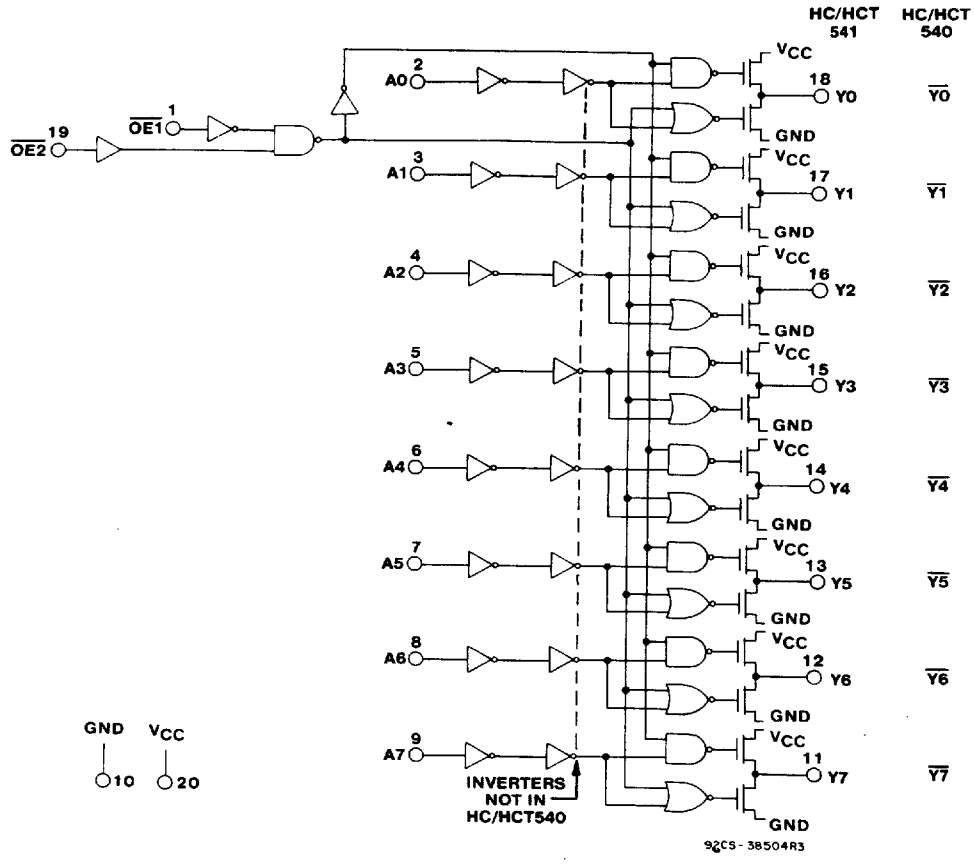


Fig. 1 — Logic diagram for the CD54/74HC/HCT 540 & 541

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC540/CD54HC540 CD74HC541/CD54HC541										CD74HCT540/CD54HCT540 CD74HCT541/CD54HCT541								UNITS
	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)							TEST CONDITIONS		AMBIENT TEMPERATURE (T_A)						
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Tables

CD54/74 HCT 540	
Input	Unit Loads*
A0 — A7	1
$\overline{OE2}$	0.75
$\overline{OE1}$	1.15

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74 HCT 541	
Input	Unit Loads*
A0 — A7	0.4
$\overline{OE2}$	0.75
$\overline{OE1}$	1.15

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r,t_f=6 ns)

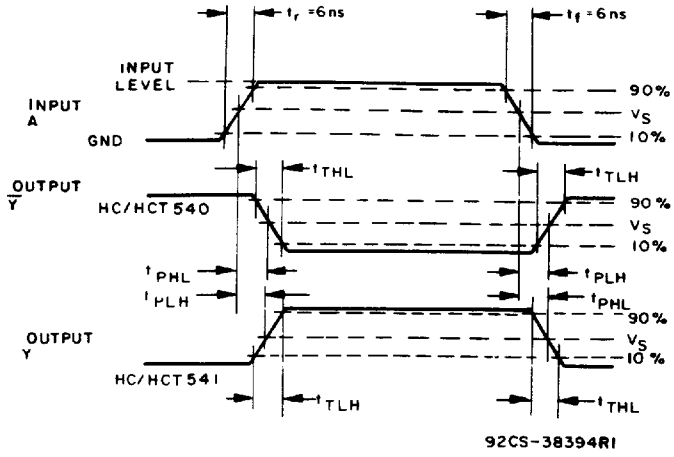
CHARACTERISTIC		C_L (pF)	TYPICAL				UNITS
			540		541		
			HC	HCT	HC	HCT	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	15	9	9	9	11	ns
Output Enable and Disable to Outputs	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	15	13	14	14	14	ns
Power Dissipation Capacitance*	C_{PD}	—	50	55	48	55	pF

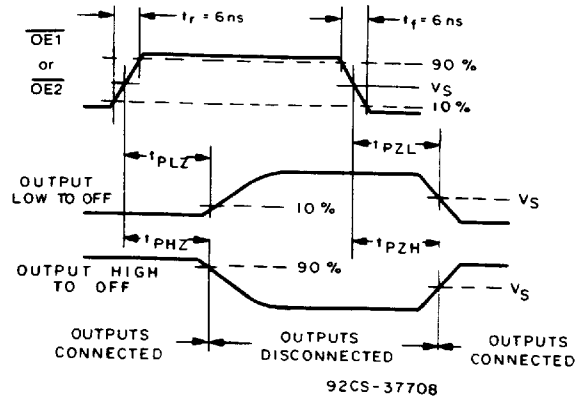
*C_{PD} is used to determine the dynamic power consumption per channel.
$PD = V_{CC}^2 f_i (C_{PD} + C_L)$
f_i = input frequency.
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	AMBIENT TEMPERATURE (T_A)												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		HC		HCT		HC		HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Data to Outputs HC/HCT 540	t_{PLH} t_{PHL}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
		4.5	—	22	—	24	—	28	—	30	—	33	—	36	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Propagation Delay Data to Outputs HC/HCT541	t_{PLH} t_{PHL}	2	—	115	—	—	—	145	—	—	—	175	—	—	ns
		4.5	—	23	—	28	—	29	—	35	—	35	—	42	
		6	—	20	—	—	—	25	—	—	—	30	—	—	
Propagation Delay Output Enable and Disable to Outputs	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
		4.5	—	32	—	35	—	40	—	44	—	48	—	53	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541





	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 — Transition times and propagation delay times.

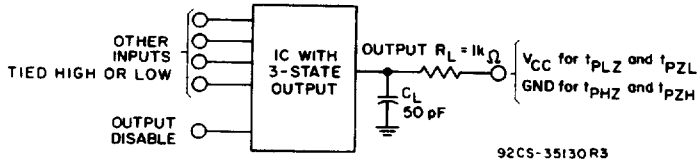
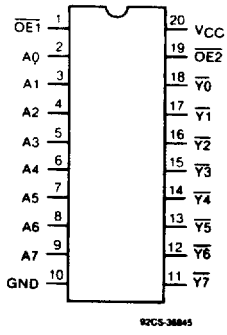
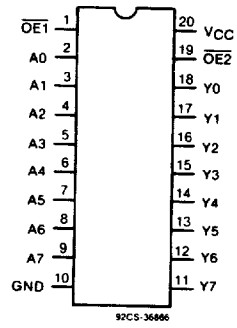


Fig. 4 — Three-state propagation delay test circuit.



CD54/74HC, HCT540 Types
TERMINAL ASSIGNMENT



CD54/74HC, HCT541 Types
TERMINAL ASSIGNMENT