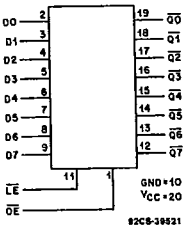
# CD54AC563/3A
# CD54ACT563/3A

T-46-07-11

## Octal Transparent Latch, 3-State Inverting

The RCA CD54AC563/3A and CD54ACT563/3A are octal transparent 3-state latches that utilize the new RCA ADVANCED CMOS LOGIC technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD54AC563/3A and CD54ACT563/3A are supplied in 20-lead dual-in-line ceramic packages (F suffix).




FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

### Package Specifications
See Section 11, Fig. 13

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### Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | |
| 3-State Leakage Current $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5• | — | ±10• | μA |
| Quiescent Supply Current (MSI) $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8• | — | 160• | μA |

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

**ACT INPUT LOADING TABLE**

| INPUT | UNIT LOAD* |
|---|---|
| $\overline{OE}$ | 0.87 |
| Dn | 0.5 |
| $\overline{LE}$ | 0.8 |

*Unit load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

### Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

| Static | STATIC BURN-IN I | | | STATIC BURN-IN II | | |
|---|---|---|---|---|---|---|
| | OPEN | GROUND | $V_{CC}$ (6V) | OPEN | GROUND | $V_{CC}$ (6V) |
| CD54AC/ACT563 | 12-19 | 1-11 | 20 | 12-19 | 10 | 1-9,11,20 |
| **Dynamic** | OPEN | GROUND | 1/2 $V_{CC}$ (3V) | $V_{CC}$ (6V) | OSCILLATOR 50 kHz | OSCILLATOR 25 kHz |
| CD54AC/ACT563 | — | 1,10 | 12-19 | 20 | 11 | 2-9 |

NOTE: Each pin except $V_{CC}$ and Gnd will have a resistor of 2k-47k ohms.

# CD54AC563/3A
# CD54ACT563/3A

**SWITCHING CHARACTERISTICS: AC Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF** (Worst Case)

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | -55 to +125°C | | UNITS |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Propagation Delays: Data to Qn | $t_{PLH}$<br>$t_{PHL}$ | 1.5<br>3.3*<br>5† | —<br>2.9<br>1.9 | 140<br>20<br>11.3• | ns |
| $\overline{LE}$ on Qn | $t_{PLH}$<br>$t_{PHL}$ | 1.5<br>3.3<br>5 | —<br>3.4<br>2.2 | 164<br>23<br>13.1• | ns |
| Output Enable and Disable Times | $t_{PZL}$<br>$t_{PZH}$<br>$t_{PLZ}$<br>$t_{PHZ}$ | 1.5<br>3.3<br>5 | —<br>4.1<br>2.6 | 181<br>25.3<br>14.5• | ns |
| Power Dissipation Capacitance | $C_{PD}$§ | — | 90 Typ. | | pF |
| Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ | 5 | 4 Typ. @ 25°C | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ | 5 | 1 Typ. @ 25°C | | V |
| Input Capacitance | $C_I$ | — | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | pF |

**SWITCHING CHARACTERISTICS: ACT Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF** (Worst Case)

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | -55 to +125°C | | UNITS |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Propagation Delays Data to Qn | $t_{PLH}$<br>$t_{PHL}$ | 5† | 1.8 | 12.7• | ns |
| $\overline{LE}$ to Qn | $t_{PLH}$<br>$t_{PHL}$ | 5 | 2.6 | 14.5• | ns |
| Output Enable and Disables Times | $t_{PZL}$<br>$t_{PZH}$<br>$t_{PLZ}$<br>$t_{PHZ}$ | 5 | 2.6 | 14.5• | ns |
| Power Dissipation Capacitance | $C_{PD}$§ | — | 108 Typ. | | pF |
| Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ | 5 | 4 Typ. @ 25°C | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ | 5 | 1 Typ. @ 25°C | | V |
| Input Capacitance | $C_I$ | — | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | pF |

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§$C_{PD}$ is used to determine the dynamic power consumption per latch.
For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where $f_i$ = input frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage

(Limits with black dots (•) are tested 100%.)