

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS
524,288-WORD BY 8-BIT FULL CMOS STATIC RAM

DESCRIPTION

The TC55V040AFT/ATR is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 0.5 μ A standby current (at $V_{DD}=3V$, $T_a=25^{\circ}C$, maximum) when chip enable ($\overline{CE1}$) is asserted high or ($CE2$) is asserted low. There are three control inputs. $\overline{CE1}$ and $CE2$ are used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to $85^{\circ}C$, the TC55V040AFT/ATR can be used in environments exhibiting extreme temperature conditions. The TC55V040AFT/ATR is available in normal and reverse pinout plastic 40-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.6V
- Power down features using $\overline{CE1}$ and $CE2$
- Data retention supply voltage of 1.5 to 3.6V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to $85^{\circ}C$
- Standby current (maximum)

3.6V	7 μ A
3.0V	5 μ A

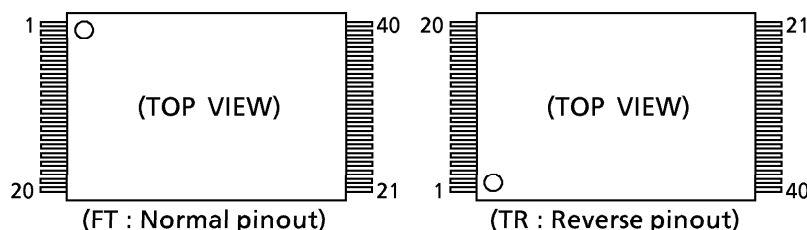
- Access Times (maximum):

	TC55V040AFT/ATR	
	-55	-70
Access Time	55 ns	70 ns
$\overline{CE1}$ Access Time	55 ns	70 ns
$CE2$ Access Time	55 ns	70 ns
\overline{OE} Access Time	30 ns	35 ns

- Package:

TSOP I 40-P-1014-0.50 (FT) (Weight:0.32g typ)
TSOP I 40-P-1014-0.50A (TR) (Weight:0.32g typ)

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A18	Address Inputs
$\overline{CE1}$, $CE2$	Chip Enable Input
R/W	Read / Write Control Input
\overline{OE}	Output Enable Input
I/O1 to I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground
NC	No Connection

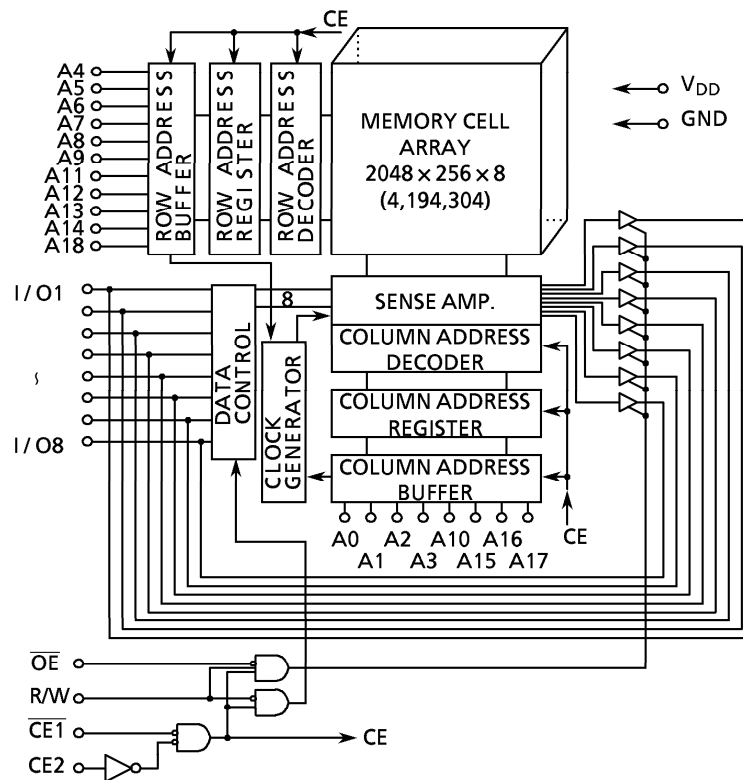
(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Pin Name	A16	A15	A14	A13	A12	A11	A9	A8	R/W	CE2	NC	NC	A18	A7	A6	A5	A4	A3	A2	A1
Pin No.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Pin Name	A0	$\overline{CE1}$	GND	\overline{OE}	I/O1	I/O2	I/O3	I/O4	NC	V_{DD}	V_{DD}	I/O5	I/O6	I/O7	I/O8	A10	NC	NC	GND	A17

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BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE1}$	CE2	\overline{OE}	R/W	I/O1 to I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	x	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	H	High-Z	I _{DDO}
Standby	H	x	x	x	High-Z	I _{DDS}
	x	L	x	x	High-Z	I _{DDS}

Note: x = don't care. H = logic high. L = logic low.

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 4.6	V
V _{IN}	Input Voltage	- 0.3 to 4.6	V
V _{I/O}	Input/Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg}	Storage Temperature	- 55 to 150	°C
T _{opr}	Operating Temperature	- 40 to 85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	2.3 to 3.6V			UNIT
		MIN	TYP	MAX	
V _{DD}	Power Supply Voltage	2.3	3.0	3.6	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	-	V _{DD} × 0.22	V
V _{DH}	Data Retention Supply Voltage	1.5	-	3.6	V

DC CHARACTERISTICS (Ta = -40° to 85°C, V_{DD} = 2.3 to 3.6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT			
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}	-	-	± 1.0	μA			
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5 V	-0.5	-	-	mA			
I _{OL}	Output Low Current	V _{OL} = 0.4 V	2.1	-	-	mA			
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 V to V _{DD}	-	-	± 1.0	μA			
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} and I _{OUT} = 0 mA Other Input = V _{IH} /V _{IL}	V _{DD} = 3.0V ± 10%	Tcycle	55ns	-	-	60	mA
I _{DDO2}					70ns	-	-	50	
		1μs	-	-	10				
		CE1 = 0.2 V and CE2 = V _{DD} - 0.2 V and R/W = V _{DD} - 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} - 0.2 V/0.2 V	V _{DD} = 3.0V ± 10%	Tcycle	55ns	-	-	55	
				70ns	-	-	45		
				1μs	-	-	5		
I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}			-	-	2	mA	
I _{DDS2} (Note)		CE1 = V _{DD} - 0.2 V or CE2 = 0.2 V V _{DD} = 1.5 to 3.6 V	V _{DD} = 3.0 V ± 10%	Ta = 25°C	-	-	0.6	μA	
	Ta = -40 to 85°C			-	-	6			
	V _{DD} = 3.3 V ± 0.3 V		Ta = 25°C	-	-	0.7			
			Ta = -40 to 85°C	-	-	7			
	V _{DD} = 3.0 V		Ta = 25°C	-	0.05	0.5			
Ta = -40 to 85°C		-	-	1					
			Ta = -40 to 85°C	-	-	5			

Note: In standby mode with CE1 ≥ V_{DD} - 0.2V, these limits are assured for the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = - 40° to 85°C, V_{DD} = 2.7 to 3.6V)

READ CYCLE

SYMBOL	PARAMETER	TC55V040AFT/ATR				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	55	–	70	–	ns
t _{ACC}	Address Access Time	–	55	–	70	
t _{CO1}	Chip Enable (CE1) Access Time	–	55	–	70	
t _{CO2}	Chip Enable (CE2) Access Time	–	55	–	70	
t _{OE}	Output Enable Access Time	–	30	–	35	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable High to Output High-Z	–	25	–	30	
t _{ODO}	Output Enable High to Output High-Z	–	25	–	30	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V040AFT/ATR				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	55	–	70	–	ns
t _{WP}	Write Pulse Width	45	–	50	–	
t _{CW}	Chip Enable to End of Write	50	–	60	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	25	–	30	
t _{OEW}	R/W High to Output Active	0	–	0	–	
t _{DS}	Data Setup Time	25	–	30	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

Output load: 30 pF + 1TTL Gate
 Input pulse level: 0.4 V, 2.4 V
 Timing measurements: V_{DD} × 0.5
 Reference level: V_{DD} × 0.5
 t_R, t_F: 5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = - 40° to 85°C, VDD = 2.3 to 3.6V)

READ CYCLE

SYMBOL	PARAMETER	TC55V040AFT/ATR				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	–	85	–	ns
t _{ACC}	Address Access Time	–	70	–	85	
t _{CO1}	Chip Enable (CE1) Access Time	–	70	–	85	
t _{CO2}	Chip Enable (CE2) Access Time	–	70	–	85	
t _{OE}	Output Enable Access Time	–	35	–	45	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable High to Output High-Z	–	30	–	35	
t _{ODO}	Output Enable High to Output High-Z	–	30	–	35	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

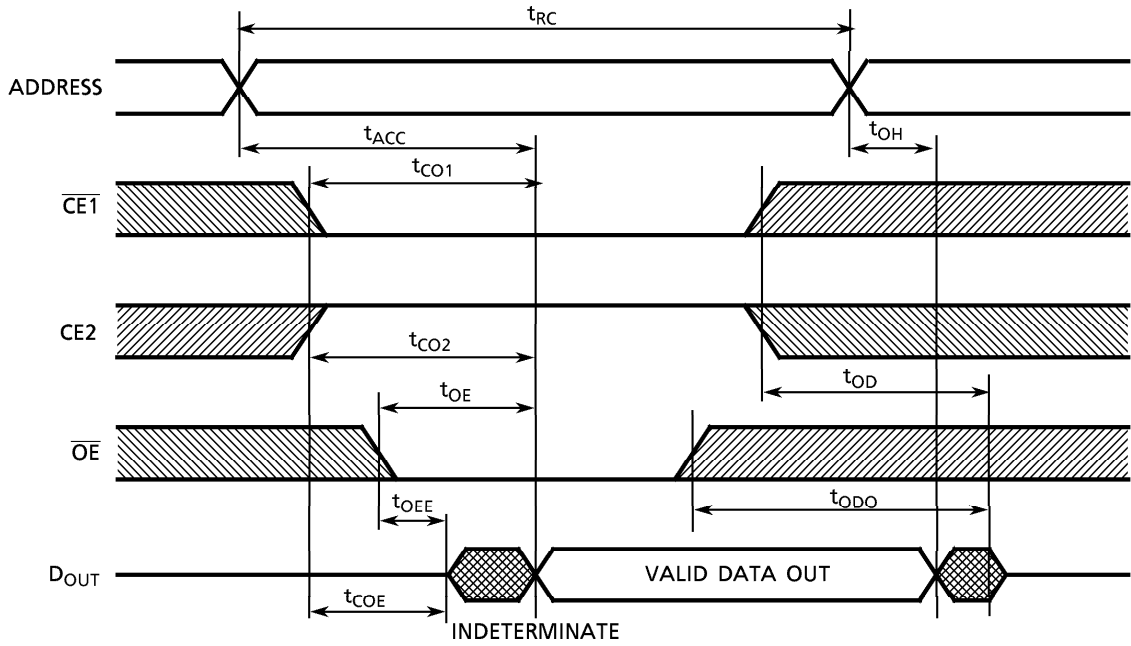
SYMBOL	PARAMETER	TC55V040AFT/ATR				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	–	85	–	ns
t _{WP}	Write Pulse Width	50	–	55	–	
t _{CW}	Chip Enable to End of Write	60	–	70	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	30	–	35	
t _{OEW}	R/W High to Output Active	0	–	0	–	
t _{DS}	Data Setup Time	30	–	35	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

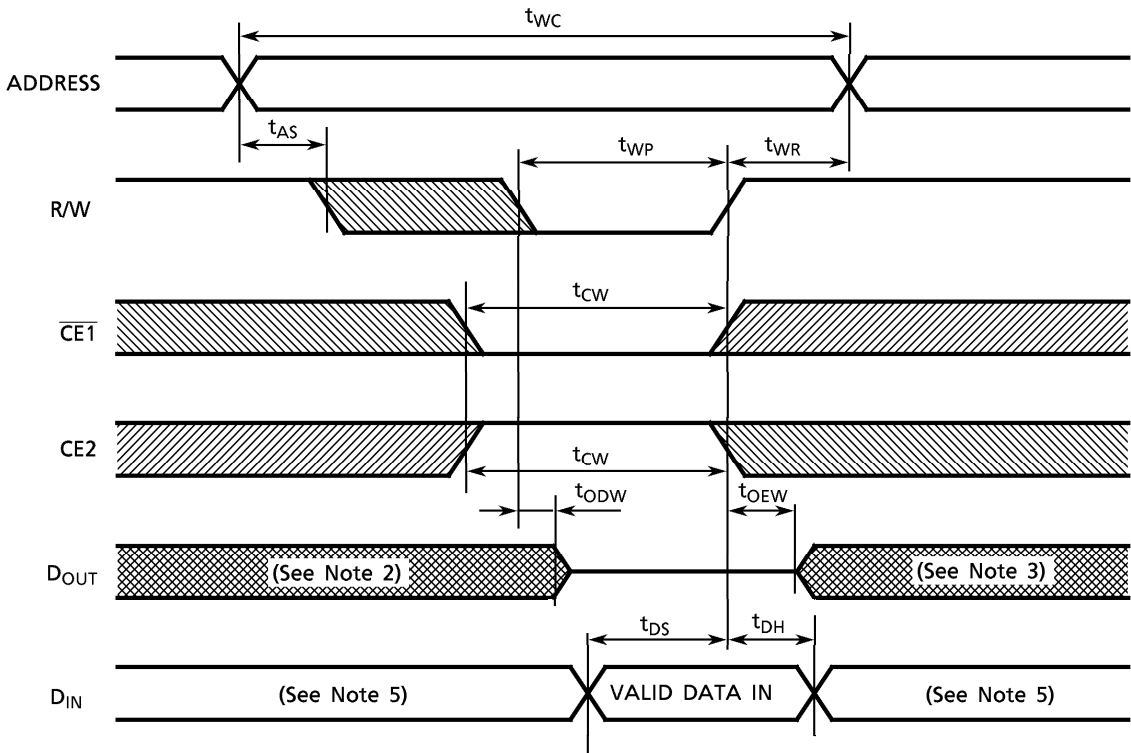
Output load: 30 pF + 1TTL Gate
 Input pulse level: V_{DD} – 0.2V, 0.2V
 Timing measurements: V_{DD} × 0.5
 Reference level: V_{DD} × 0.5
 t_R, t_F: 5 ns

TIMING DIAGRAMS

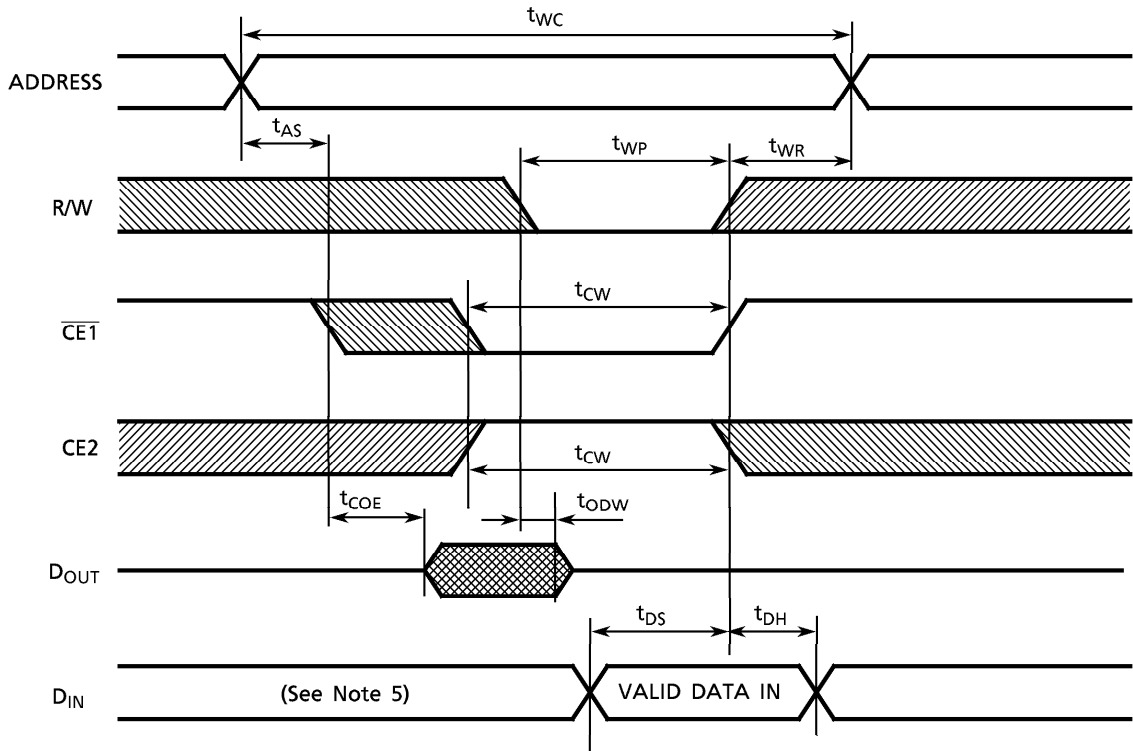
READ CYCLE (See Note 1)



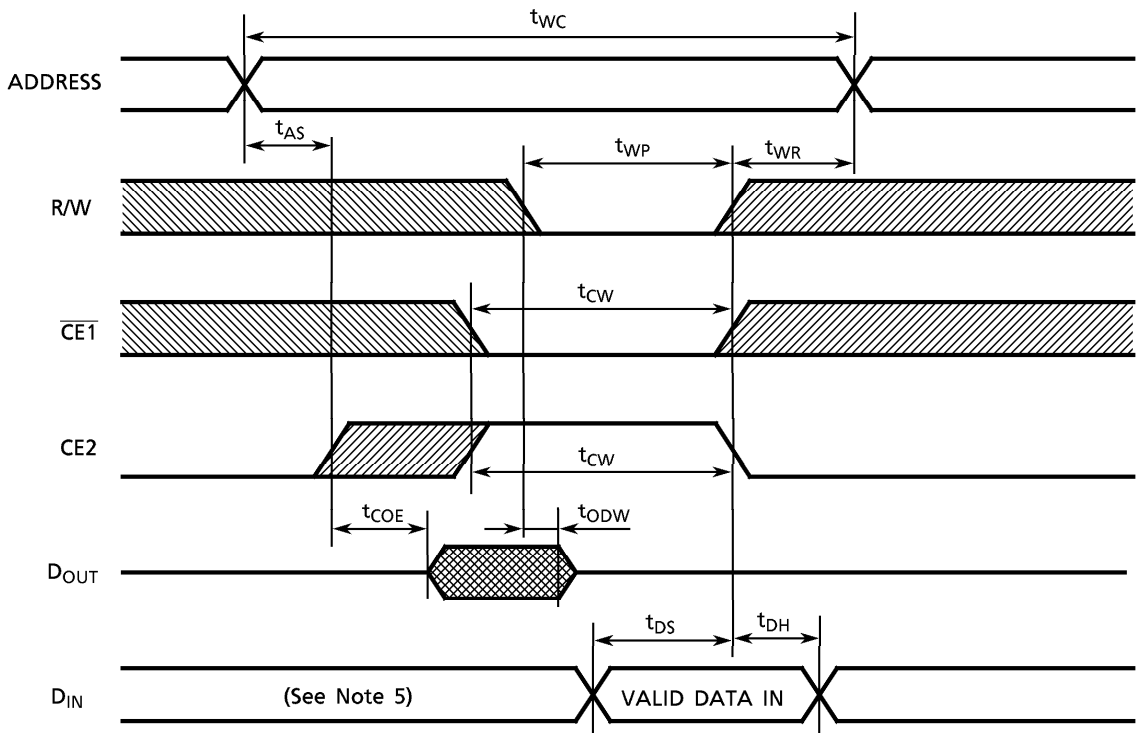
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (CE1 CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



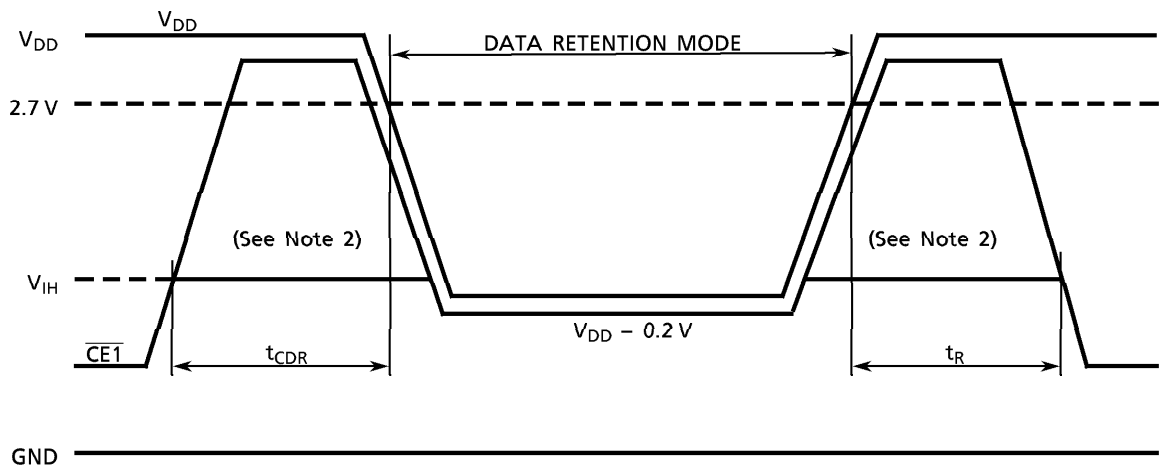
- Note:
- (1) R/W remains HIGH for the read cycle.
 - (2) If $\overline{CE1}$ goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
 - (3) If $\overline{CE1}$ goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
 - (4) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
 - (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

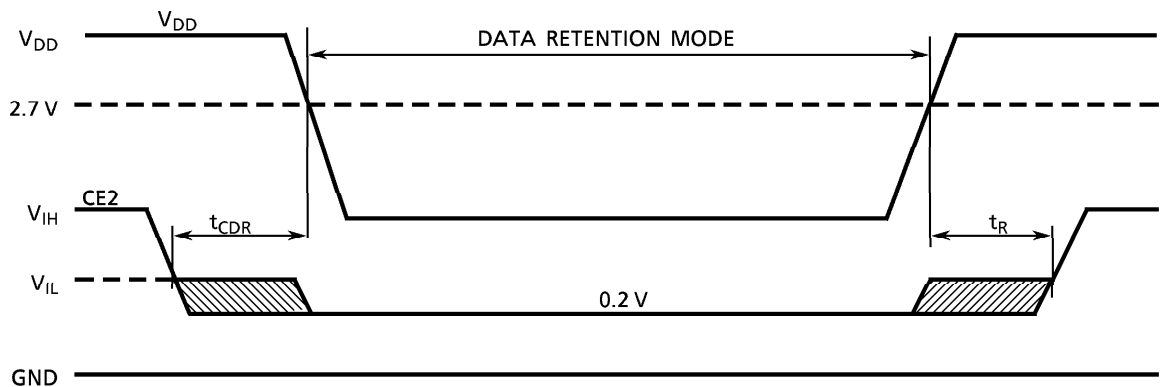
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V_{DH}	Data Retention Supply Voltage		1.5	-	3.6	V	
I_{DSS2}	Standby Current	$V_{DH} = 3.0\text{ V}$	$T_a = -40^\circ\text{ to }40^\circ\text{C}$	-	-	1	μA
			$T_a = -40^\circ\text{ to }85^\circ\text{C}$	-	-	5	
		$V_{DH} = 3.6\text{ V}$	$T_a = -40^\circ\text{ to }85^\circ\text{C}$	-	-	7	
t_{CDR}	Chip Deselect to Data Retention Mode Time		0	-	-	nS	
t_R	Recovery Time		t_{RC} (See Note)	-	-	nS	

Note: Read cycle time

$\overline{CE1}$ CONTROLLED DATA RETENTION MODE (See Note 1)



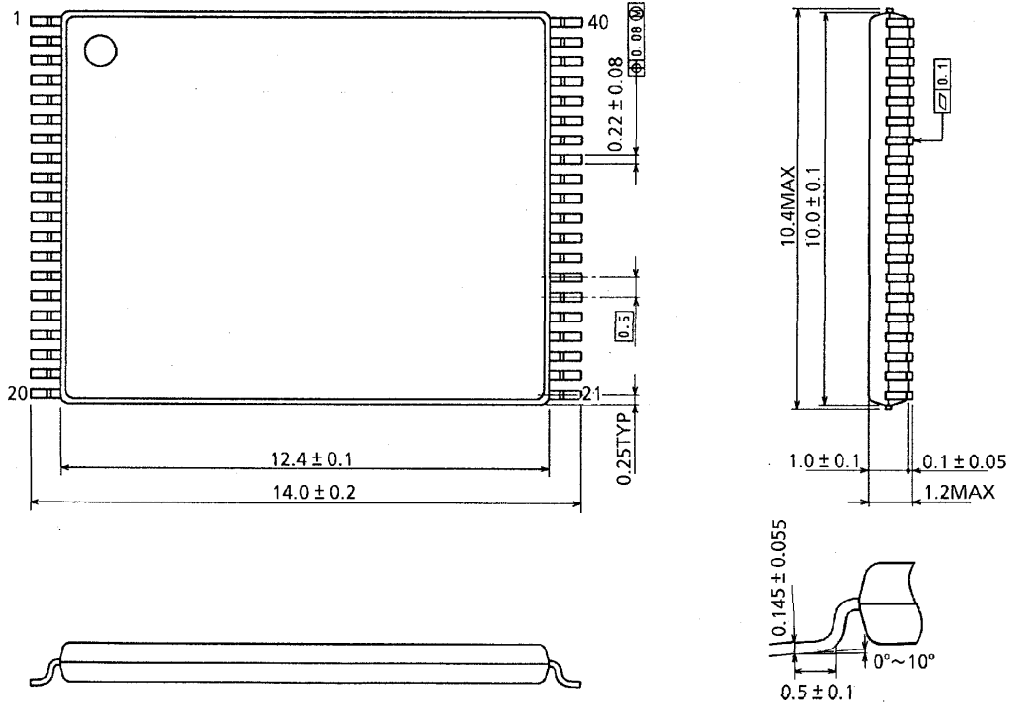
CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



- Note:
- (1) In $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current mode is entered when $\text{CE2} \leq 0.2 \text{ V}$ or $\text{CE2} \geq V_{\text{DD}} - 0.2 \text{ V}$.
 - (2) When $\overline{\text{CE1}}$ is operating at the V_{IH} level (2.2 V), the operating current is given by I_{DDSI} during the transition of V_{DD} from 3.6 to 2.4 V.
 - (3) In CE2 controlled data retention mode, minimum standby current mode is entered when $\text{CE2} \leq 0.2 \text{ V}$.

PACKAGE DIMENSIONS (TSOP I 40-P-1014-0.50)

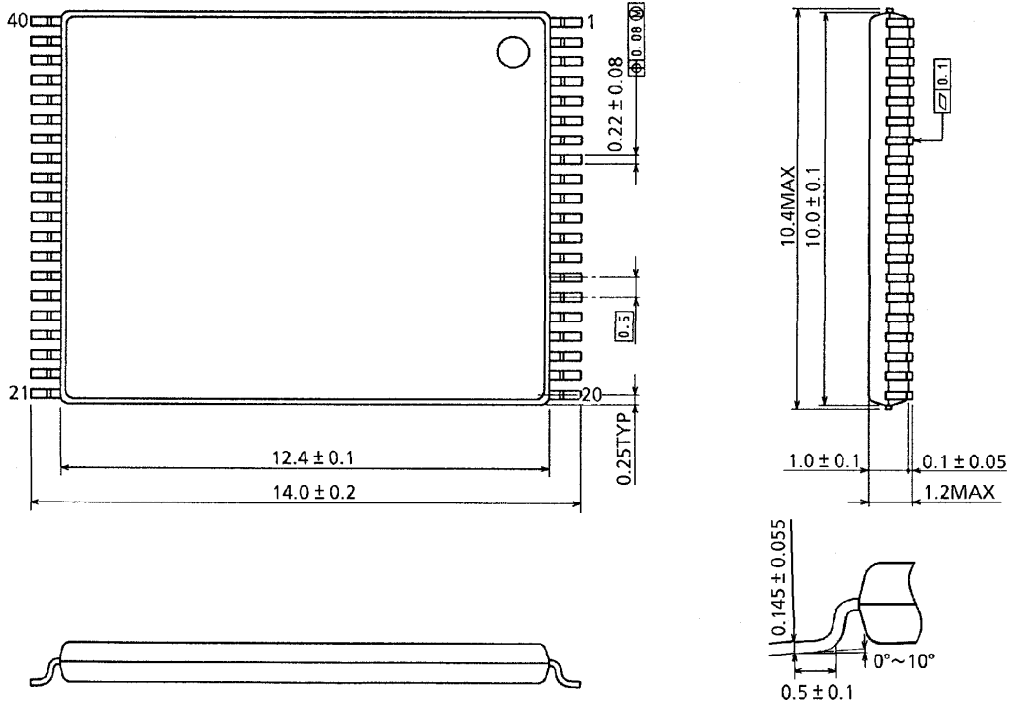
Units in mm



Weight: 0.32 g (typ)

PACKAGE DIMENSIONS (TSOP I 40-P-1014-0.5A)

Units in mm



Weight: 0.32 g (typ)