

SSM6L05FU

Power Management Switch
High Speed Switching Applications

- Small package
- Low on resistance Q1: $R_{on} = 0.8 \Omega$ (max) (@ $V_{GS} = 4$ V)
 Q2: $R_{on} = 3.3 \Omega$ (max) (@ $V_{GS} = -4$ V)
- Low gate threshold voltage

Q1 Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	20	V
Gate-Source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	400	mA
	Pulse	I_{DP}	800	

Q2 Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	-20	V
Gate-Source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	-200	mA
	Pulse	I_{DP}	-400	

Absolute Maximum Ratings (Q1, Q2 common) ($T_a = 25^\circ\text{C}$)

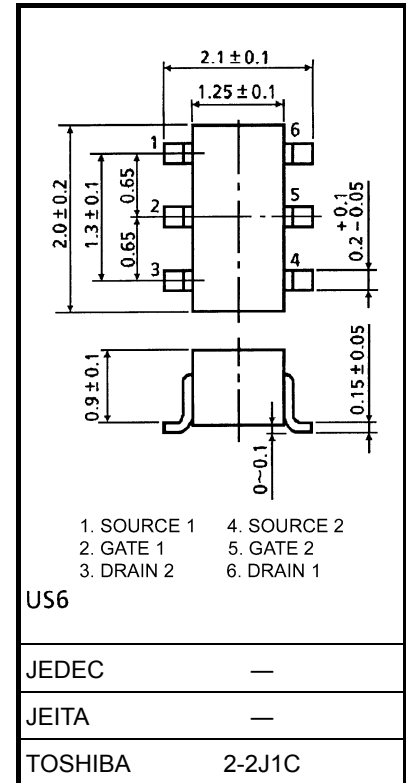
Characteristics	Symbol	Rating	Unit
Drain power dissipation ($T_a = 25^\circ\text{C}$)	P_D (Note 1)	300	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55~150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32 mm² × 6)

Unit: mm



US6

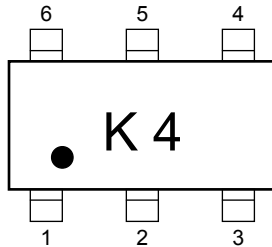
JEDEC	—
JEITA	—
TOSHIBA	2-2J1C

Weight: 6.8 mg (typ.)

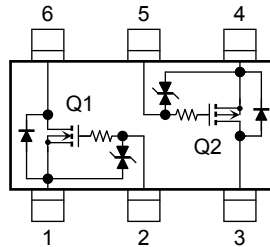
Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Marking



Equivalent Circuit (top view)



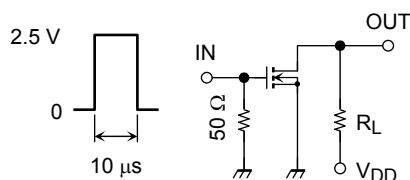
Q1 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0$	—	—	± 1	μA
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0$	20	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0$	—	—	1	μA
Gate threshold voltage	V_{th}	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.6	—	1.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 200\text{ mA}$ (Note2)	350	—	—	mS
Drain-Source ON resistance	$R_{DS(ON)}$	$I_D = 200\text{ mA}, V_{GS} = 4\text{ V}$ (Note2)	—	0.6	0.8	Ω
		$I_D = 200\text{ mA}, V_{GS} = 2.5\text{ V}$ (Note2)	—	0.85	1.2	
Input capacitance	C_{iss}	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	22	—	pF
Reverse transfer capacitance	C_{rss}		—	9	—	pF
Output capacitance	C_{oss}		—	21	—	pF
Switching time	Turn-on time	t_{on}	$V_{DD} = 3\text{ V}, I_D = 100\text{ mA},$		—	ns
	Turn-off time	t_{off}	$V_{GS} = 0 \sim 2.5\text{ V}$			

Note2: Pulse test

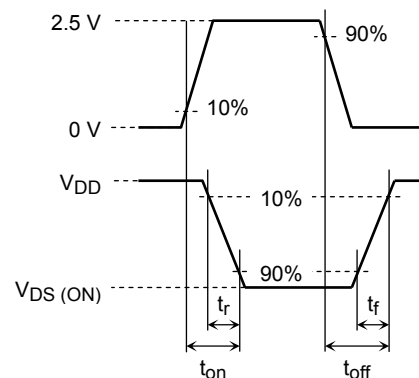
Switching Time Test Circuit (Q1: Nch MOS FET)

(a) Test circuit

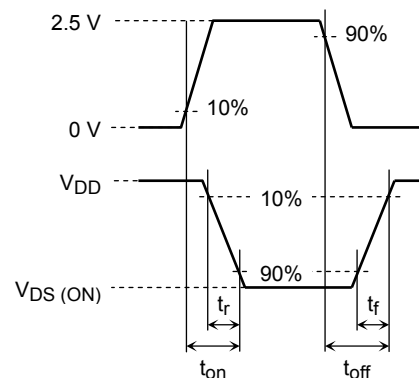


$V_{DD} = 3\text{ V}$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5\text{ ns}$
 ($Z_{out} = 50\ \Omega$)
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}



(c) V_{OUT}



Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = 100 \mu A$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(OFF)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration for using the device.

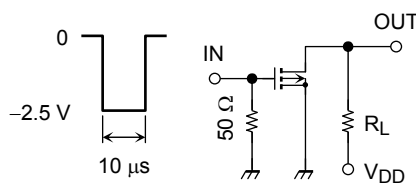
Q2 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 12 V, V_{DS} = 0$	—	—	± 1	μA
Drain-Source breakdown voltage		$V_{(BR)DSS}$	$I_D = -1 mA, V_{GS} = 0$	-20	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = -20 V, V_{GS} = 0$	—	—	-1	μA
Gate threshold voltage		V_{th}	$V_{DS} = -3 V, I_D = -0.1 mA$	-0.6	—	-1.1	V
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -3 V, I_D = -50 mA$ (Note2)	100	—	—	mS
Drain-Source ON resistance		$R_{DS(ON)}$	$I_D = -100 mA, V_{GS} = -4 V$ (Note2)	—	2.1	3.3	Ω
			$I_D = -50 mA, V_{GS} = -2.5 V$ (Note2)	—	3.2	4.0	
Input capacitance		C_{iss}	$V_{DS} = -3 V, V_{GS} = 0, f = 1 MHz$	—	27	—	pF
Reverse transfer capacitance		C_{rss}		—	7	—	pF
Output capacitance		C_{oss}		—	21	—	pF
Switching time	Turn-on time	t_{on}	$V_{DD} = -3 V, I_D = -50 mA,$ $V_{GS} = 0 \sim -2.5 V$	—	70	—	ns
	Turn-off time	t_{off}		—	70	—	

Note2: Pulse test

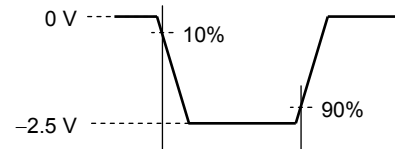
Switching Time Test Circuit (Q2: Pch MOS FET)

(a) Test circuit

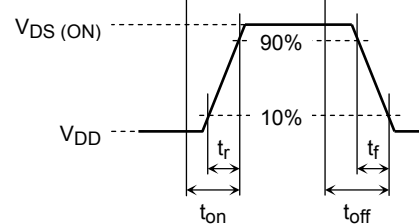


$V_{DD} = -3 V$
Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 ns$
($Z_{out} = 50 \Omega$)
Common Source
 $T_a = 25^\circ C$

(b) V_{IN}



(c) V_{OUT}

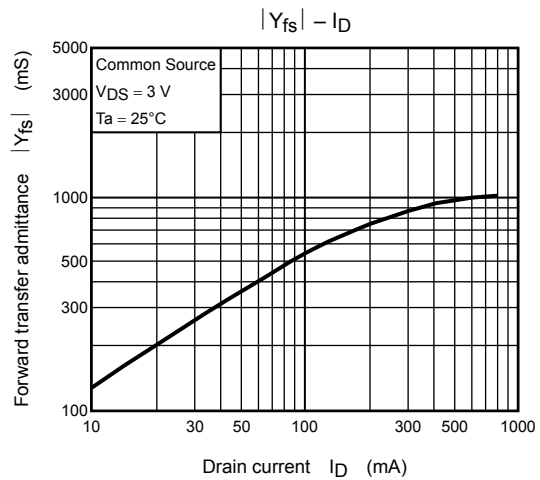
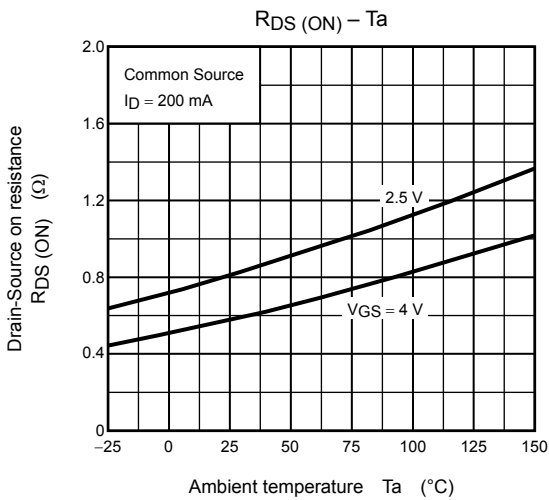
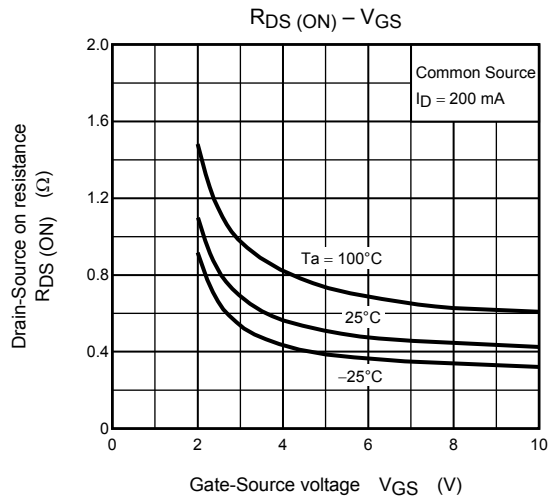
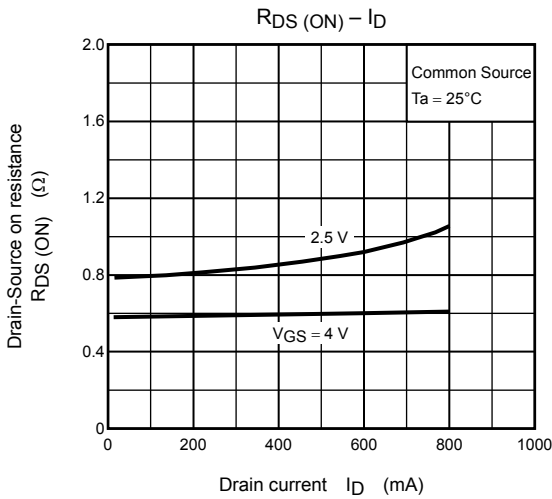
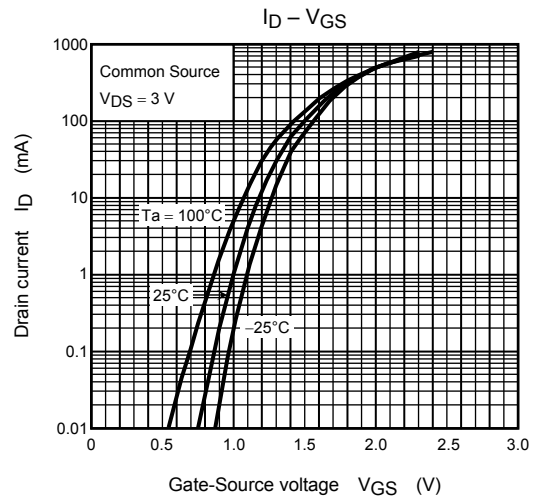
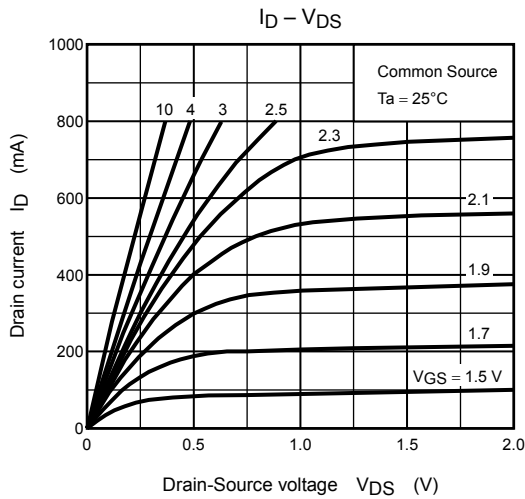


Precaution

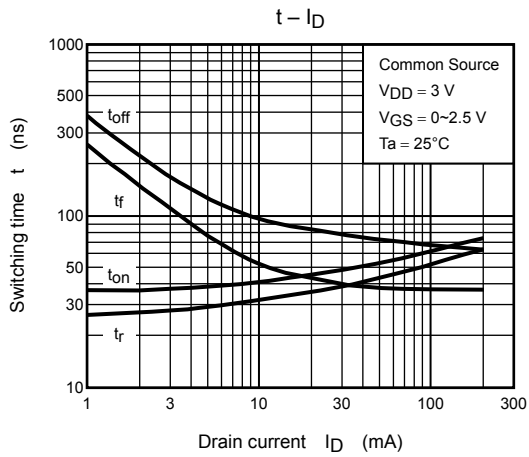
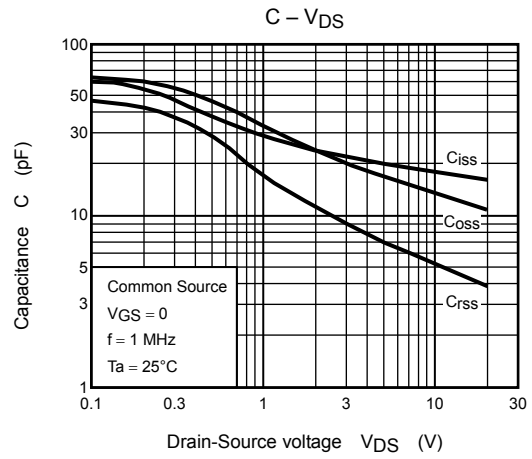
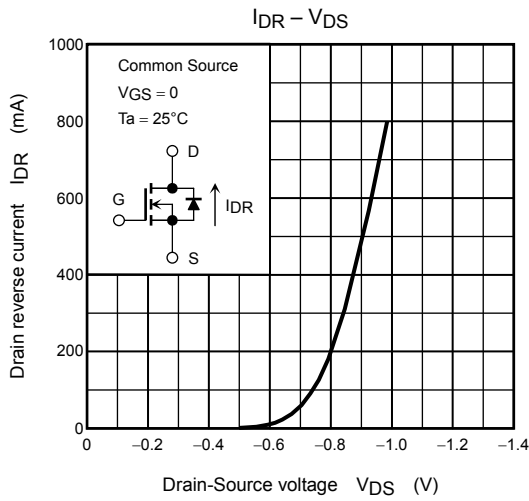
V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = -100 \mu A$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(OFF)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration for using the device.

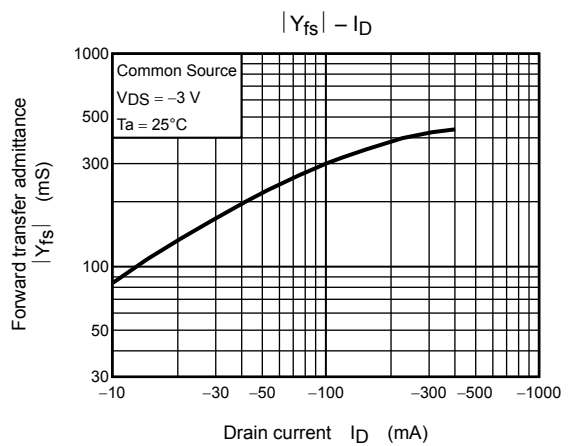
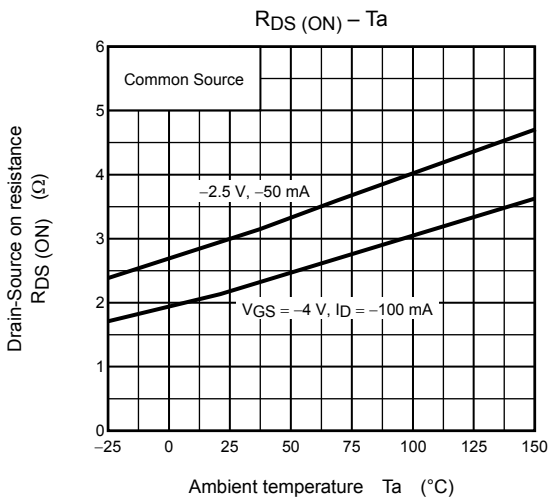
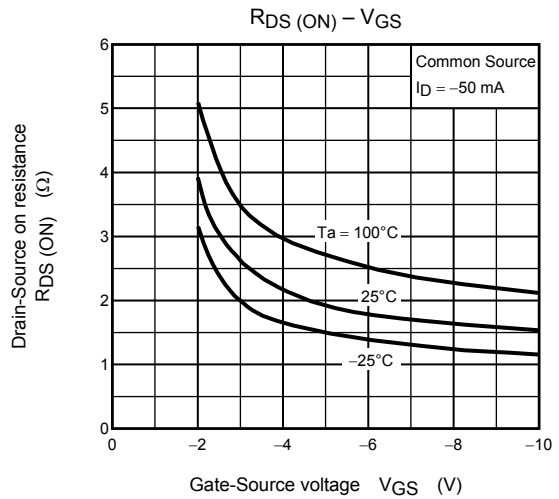
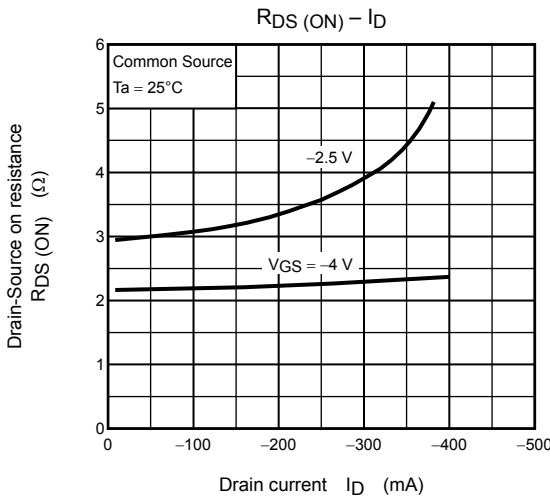
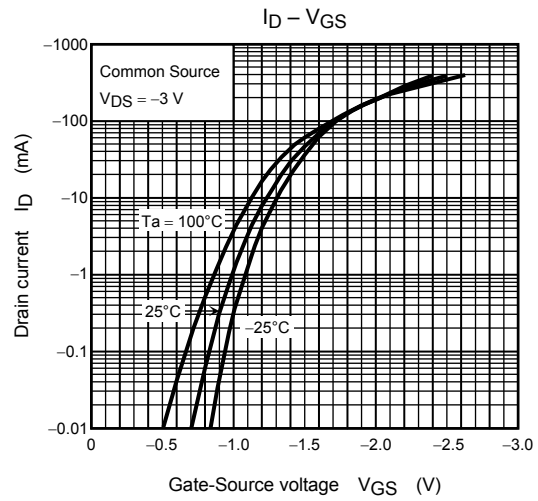
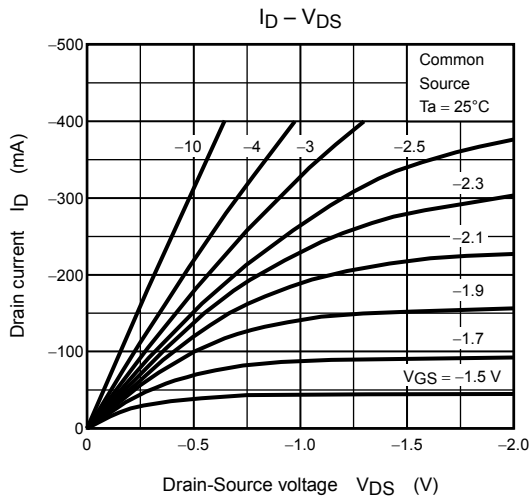
Q1 (Nch MOS FET)



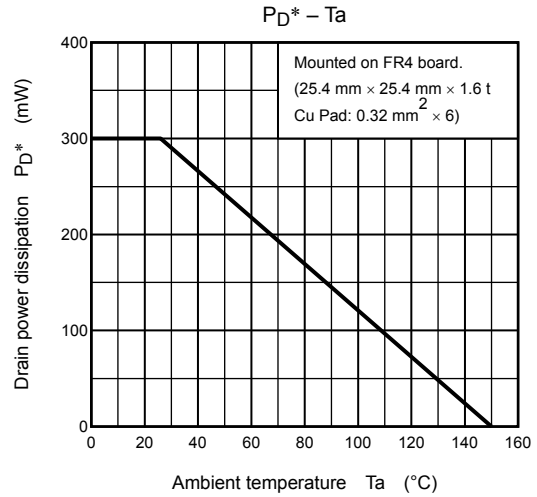
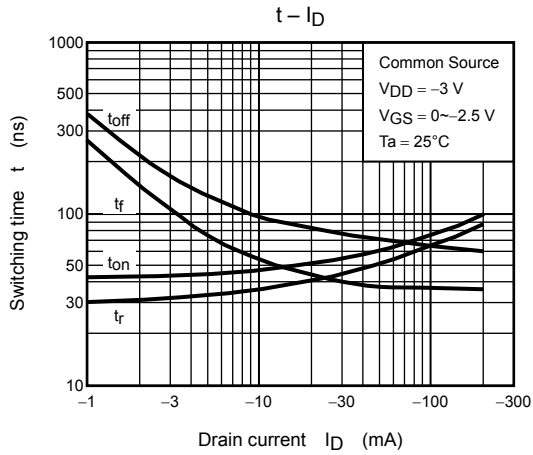
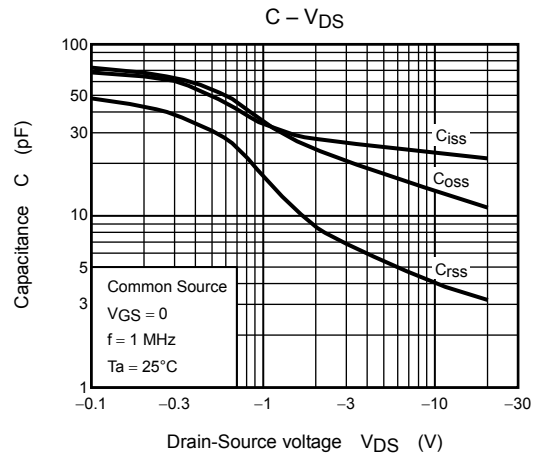
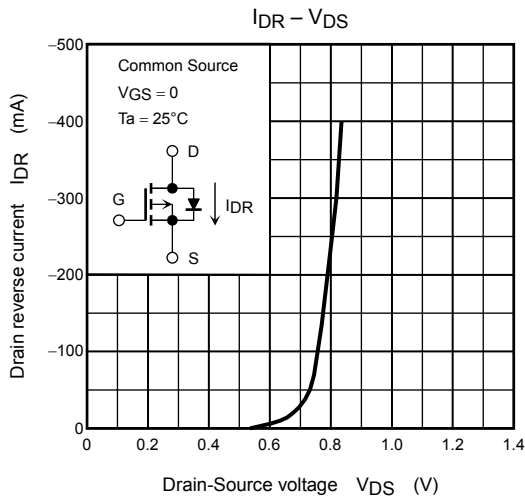
Q1 (Nch MOS FET)



Q2 (Pch MOS FET)



Q2 (Pch MOS FET)



*: Total rating

RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

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