Integrated Device Technology, Inc.

16K x 32 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4031

T-46-23-14

FEATURES:

- High density 512K static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line Package)
- Ultra-fast access time: 8ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

PIN CONFIGURATION[1]

		1	GND	
PD0	2	3	PD1	PD0 –GND
I/O0	4	5	I/O8	PD1 –OPEN
I/O1	6	7	I/O9	
I/O2	8	9	I/O10	
I/O3	10	11	I/O11	
VCC	12	13	A0	
A7	14	15	A1	
A8	16	17	A2	
A9	18	19	I/O12	
I/O4	20	21	I/O13	
I/O5	22	23	I/O14	
I/O6	24	25	I/O15	
I/O7	26	27	GND	
$\overline{WE}$	28	29	NC	
NC	30	31	$\overline{CS}_2$	
$\overline{CS}_1$	32			
		33	$\overline{CS}_4$	
$\overline{CS}_3$	34	35	NC	
NC	36	37	$\overline{OE}$	
GND	38	39	I/O24	
I/O16	40	41	I/O25	
I/O17	42	43	I/O26	
I/O18	44	45	I/O27	
I/O19	46	47	A3	
A10	48	49	A4	
A11	50	51	A5	
A12	52	53	VCC	
A13	54	55	A6	
I/O20	56	57	I/O28	
I/O21	58	59	I/O29	
I/O22	60	61	I/O30	
I/O23	62	63	I/O31	
GND	64			

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ZIP
TOP VIEW

NOTE:
1. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the depth of the module. If PD0 reads GND and PD1 reads Open, then the module has 16K depth.

DESCRIPTION:

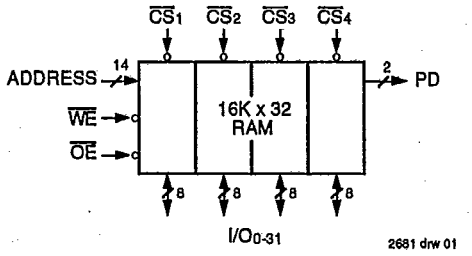
The IDT7MP4031 is a 16K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 16K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high performance, high reliability BiCEMOS™ or CEMOS™ technology. The IDT7MP4031 is available with access time as fast as 8ns with minimal power consumption.

The IDT7MP4031 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line Package). The dual row configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MP4031 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 16K depth.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

I/O0–31	Data Input/Output
A0–13	Addresses
$\overline{CS}_{1-4}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD0–1	Depth Identification
VCC	Power
GND	Ground

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CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	70	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	15	pF

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NOTE:
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}[2]	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

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NOTES:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.
2. I/O pins must not exceed Vcc +0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. I/O pins must not exceed VCC +0.5V.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	7MP4031S Max.	7MP4031B Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	5	10	µA
I_{LO}	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	—	V

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Symbol	Parameter	Test Conditions	7MP4031B 8 - 15ns Max.	7MP4031S 20 - 35ns Max.	Unit
I_{CC}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	1600	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC} = Max. f = f_{MAX}, Outputs Open	—	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ – 0.2V; f = 0, $V_{IN} > V_{CC}$ – 0.2V or < 0.2V	—	160	mA

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

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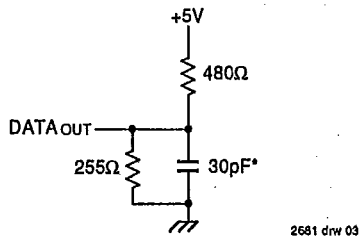

*Including scope and jig.

Figure 1. Output Load

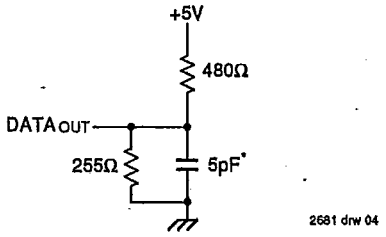

Figure 2. Output Load
(for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ and tOW)

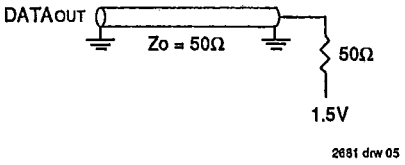

Figure 3. Alternate Output Load

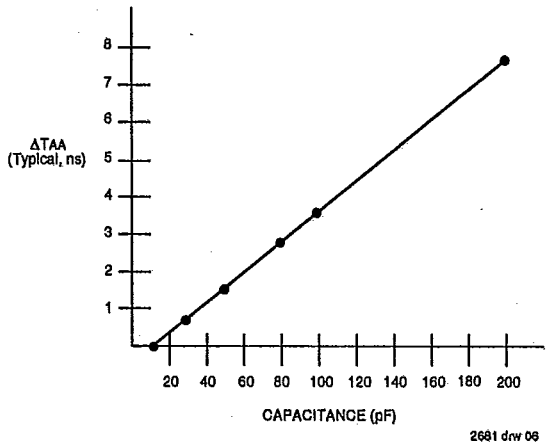

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4031BxxZ -8[2] Min.	-8[2] Max.	-10[2] Min.	-10[2] Max.	-12 Min.	-12 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	ns
t_{ACS}	Chip Select Access Time	—	8	—	10	—	12	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	1	—	1	—	1	—	ns
t_{OE}	Output Enable to Output Valid	—	4	—	5	—	6	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	1	—	1	—	1	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	3	—	3	—	3	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t_{CW}	Chip Select to End of Write	8	—	8	—	9	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	9	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	3	—	3	—	3	ns
t_{OW}	Data to Write Time Overlap	5	—	5	—	6	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	3	—	3	—	3	—	ns

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NOTES:
1. This parameter is guaranteed, but not tested.
2. Preliminary specifications only.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MP4031BxxZ		7MP4031SxxZ						
		-15		-20		-25		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	7	—	8	—	10	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	14	—	17	—	20	—	30	—	ns
t_{CW}	Chip Select to End of Write	14	—	17	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	14	—	17	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	17	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	6	—	7	—	7	—	10	ns
t_{DW}	Data to Write Time Overlap	10	—	10	—	13	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed, but not tested.

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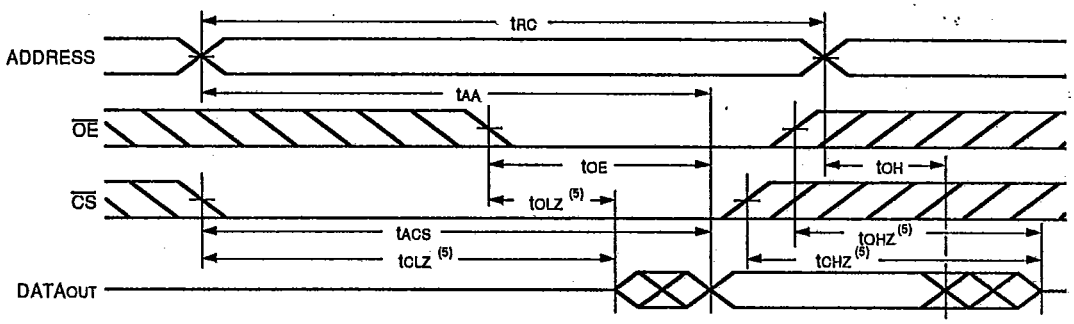
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



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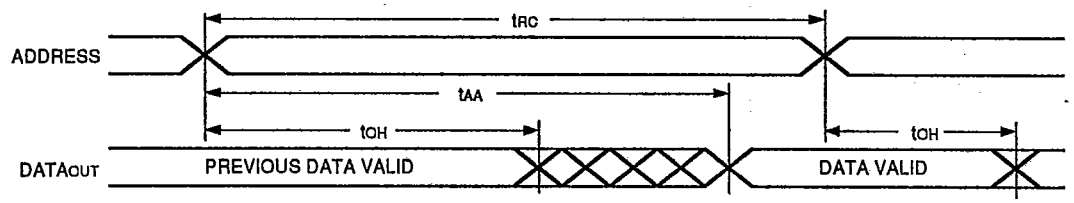
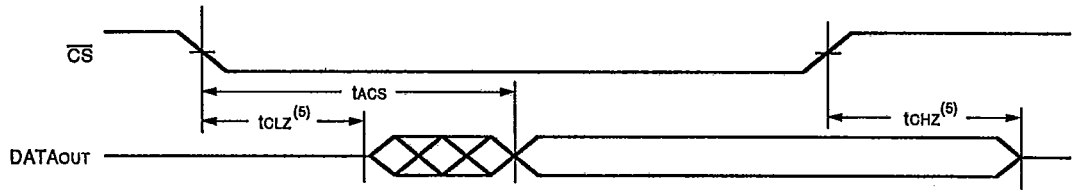
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2681 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



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NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

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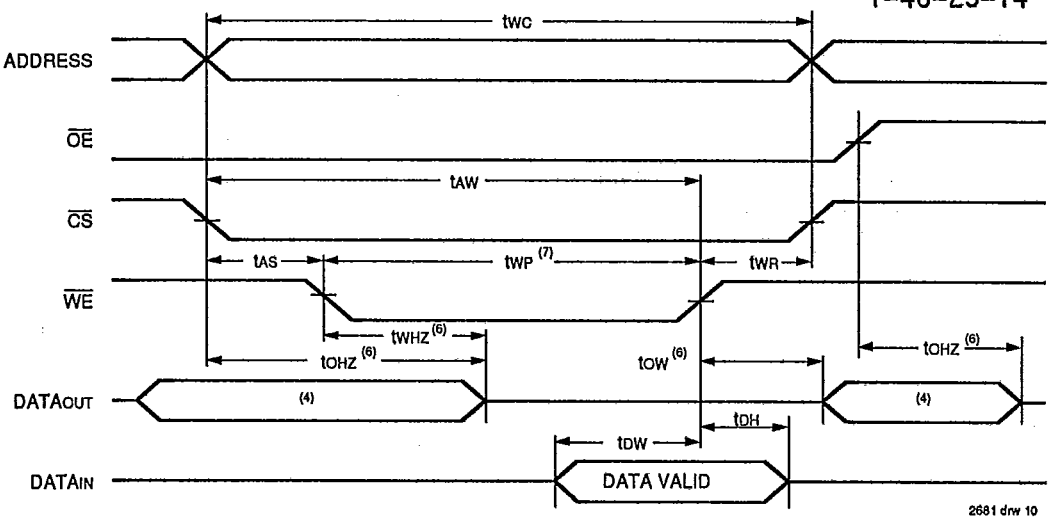
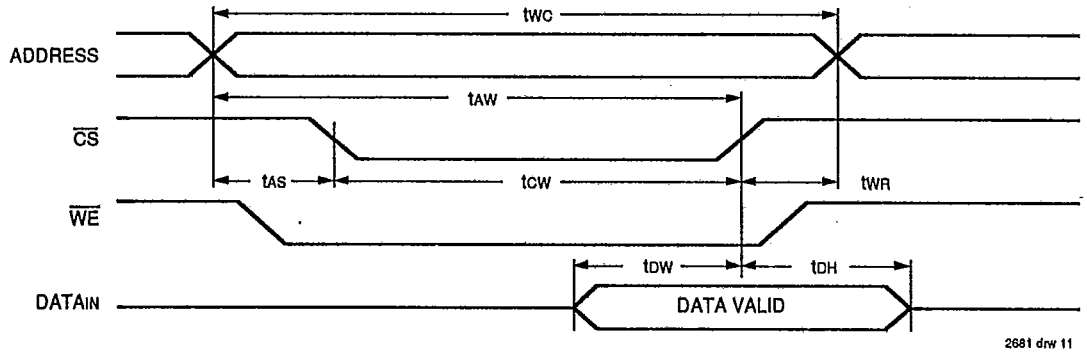


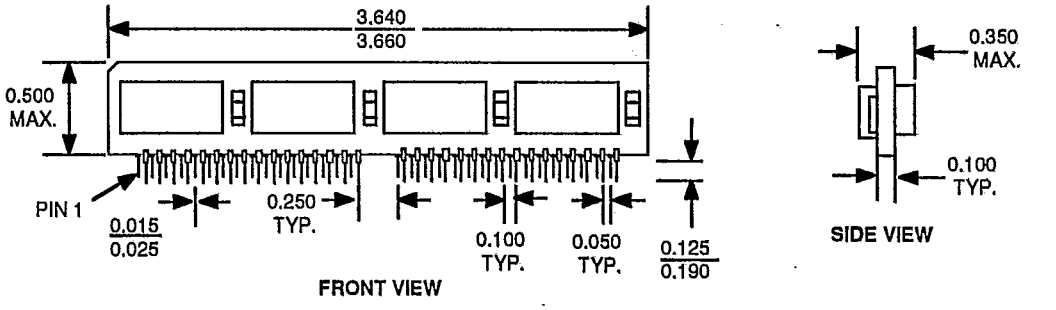
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (twp) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twr is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of twp or (twhz + tow) to allow the I/O drivers to turn off data and to be placed on the bus for the required tow. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp .

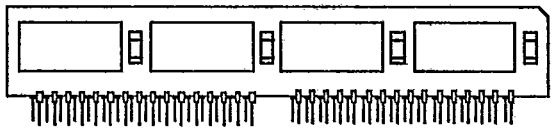
PACKAGE DIMENSIONS

T-46-23-14



FRONT VIEW

SIDE VIEW



BACK VIEW

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