HMC644

GaAs MMIC 5-BIT DIGITAL PHASE SHIFTER, 15 - 18.5 GHz

Typical Applications

The HMC644 is ideal for:

- EW Receivers
- Weather & Military Radar
- Satellite Communications
- Beamforming Modules
- Phase Cancellation

Features

Low RMS Phase Error: 4°

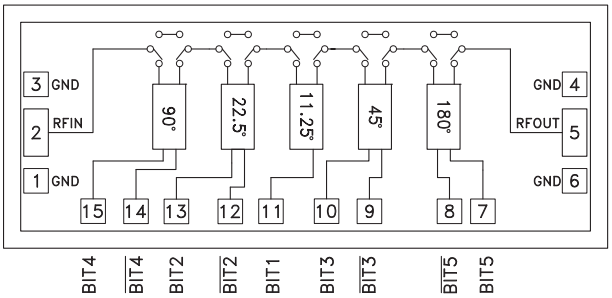
Low Insertion Loss: 7 dB

High Linearity: +40 dBm

360° Coverage, LSB = 11.25°

Die Size: 2.75 x 0.99 x 0.1 mm

Functional Diagram



General Description

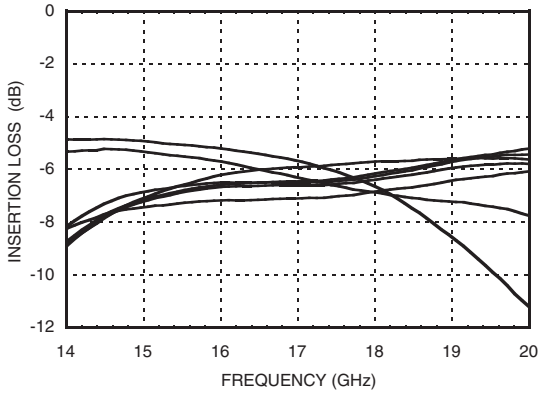
The HMC644 is a 5-bit digital phase shifter die which is rated from 15 to 18.5 GHz, providing 360 degrees of phase coverage, with a LSB of 11.25 degrees. The HMC644 features very low RMS phase error of 4 degrees and extremely low insertion loss variation of ±0.5 dB across all phase states. This high accuracy phase shifter is controlled with complementary logic of 0/-3V, and requires no fixed bias voltage and is internally matched to 50 Ohms with no external components. Simple external level shifting circuitry can be used to convert a positive CMOS control voltage into complementary negative control signals.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Control Voltage = 0/-3V

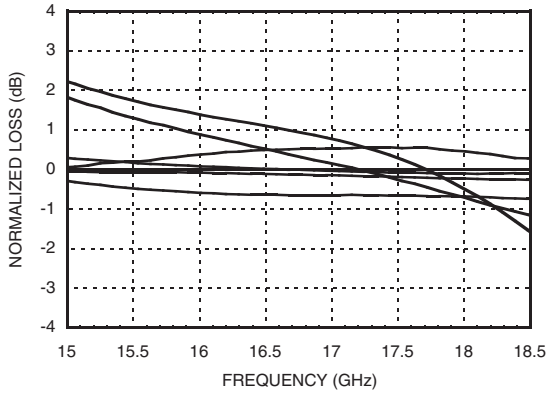
Parameter	Min.	Typ.	Max.	Units
Frequency Range	15		18.5	GHz
Insertion Loss*		7	9	dB
Input Return Loss*		10		dB
Output Return Loss*		8		dB
Phase Error*		±5	-15 / +10	deg
RMS Phase Error		4		deg
Insertion Loss Variation*		±0.5		dB
Input Power for 1 dB Compression		23		dBm
Input Third Order Intercept		40		dBm
Control Voltage Current		<1		µA

*Note: Major States Shown

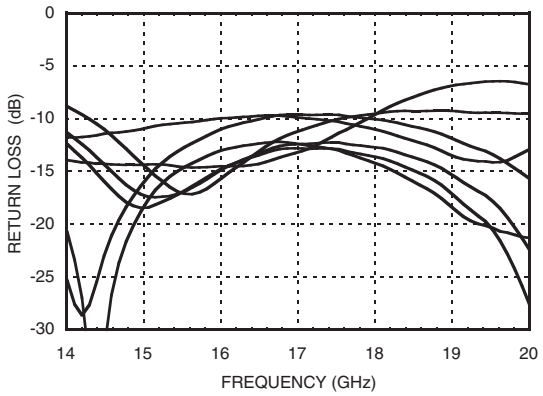
Insertion Loss, Major States Only



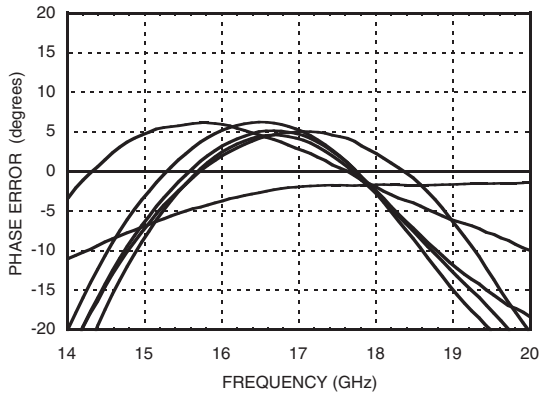
Normalized Loss, Major States Only



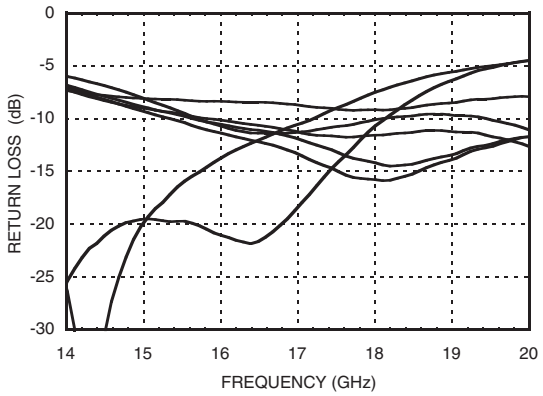
Input Return Loss, Major States Only



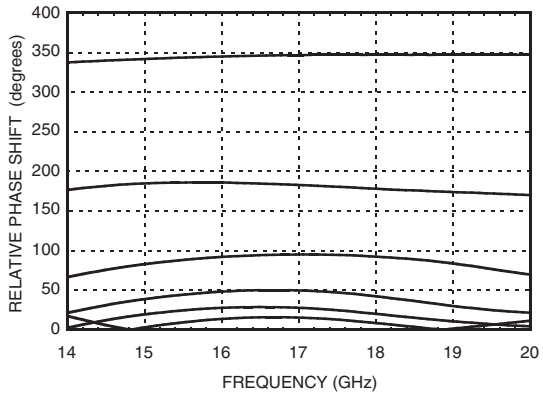
Phase Error, Major States Only



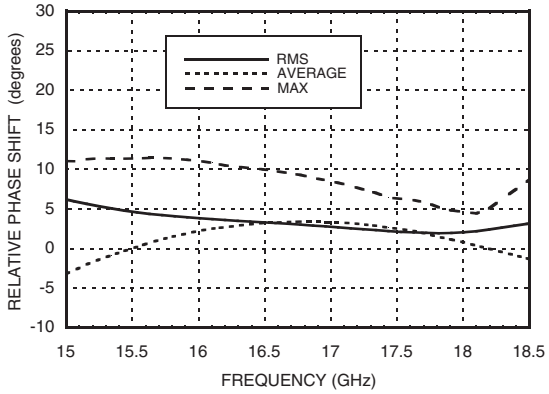
Output Return Loss, Major States Only



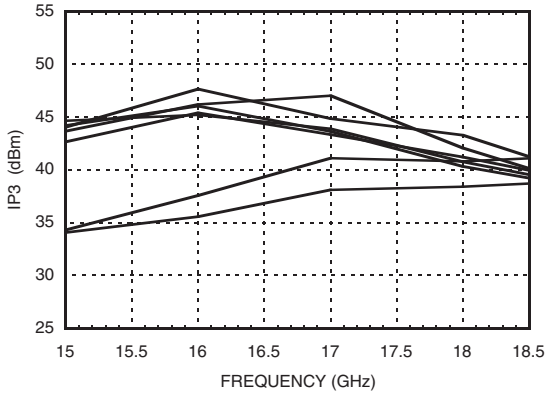
Relative Phase Shift Major States, Including All Bits



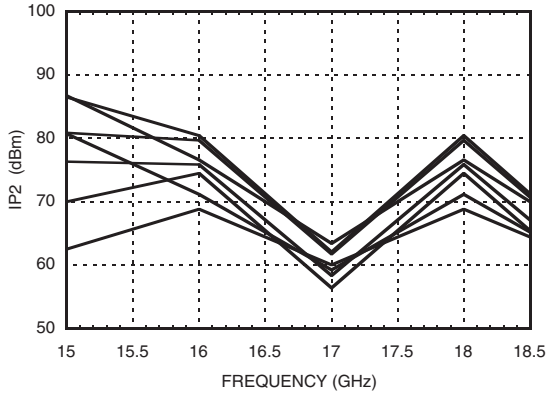
Relative Phase Shift, RMS, Average, Max, All States



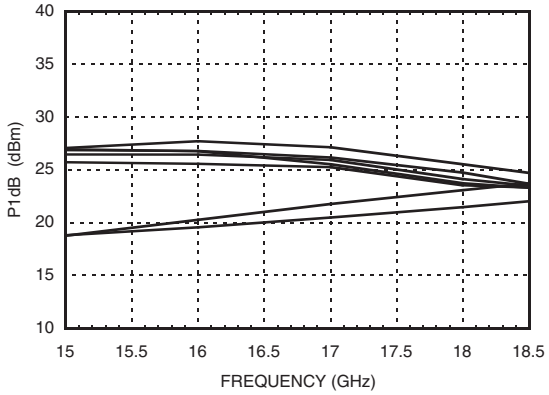
Input IP3, Major States Only



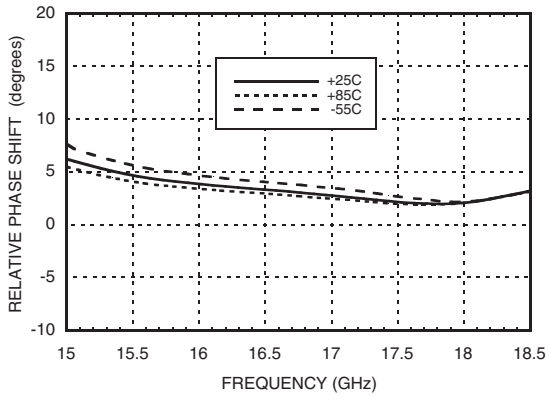
Input IP2, Major States Only



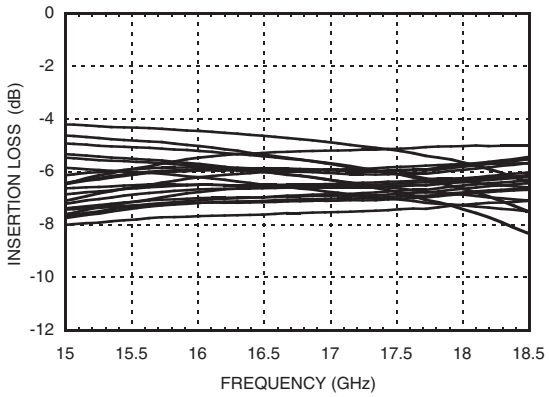
Input P1dB, Major States Only



RMS Phase Error vs. Temperature



Insertion Loss vs. Temperature, Major States Only



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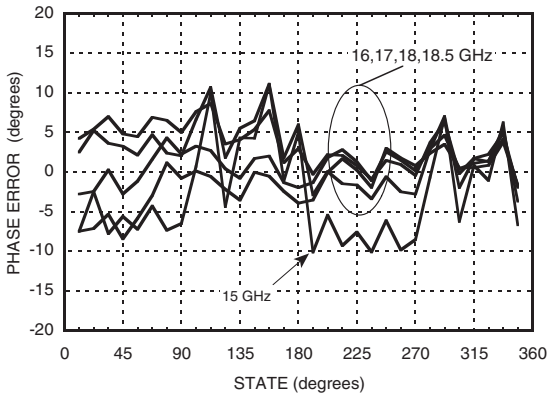
Phase Error vs. State



Absolute Maximum Ratings

Input Power (RFIN)	27 dBm (T= +85 °C)
Channel Temperature (Tc)	150 °C
Thermal Resistance (channel to die bottom)	130 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

Control Voltage

State	Bias Condition
Low (0)	-2.5 to -3.5V @ 0.4 µA Typ.
High (1)	0 to +0.3V @ 0.4 µA Typ.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Truth Table

Control Voltage Input									Phase Shift (Degrees) RFIN - RFOUT
Bit 1	Bit 2	$\overline{\text{Bit 2}}$	Bit 3	$\overline{\text{Bit 3}}$	Bit 4	$\overline{\text{Bit 4}}$	Bit 5	$\overline{\text{Bit 5}}$	
0	0	1	0	1	0	1	0	1	Reference*
1	0	1	0	1	0	1	0	1	11.25
0	1	0	0	1	0	1	0	1	22.5
0	0	1	1	0	0	1	0	1	45.0
0	0	1	0	1	1	0	0	1	90.0
0	0	1	0	1	0	1	1	0	180.0
1	1	0	1	0	1	0	1	0	348.75

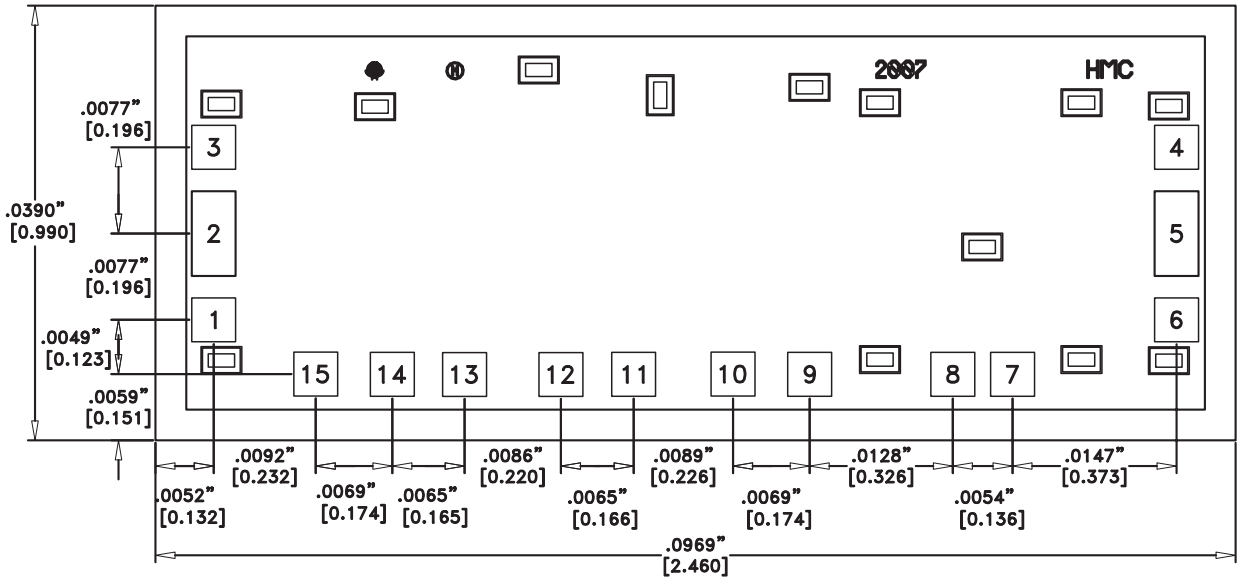
Any combination of the above states will provide a phase shift approximately equal to the sum of the bits selected.

*Reference corresponds to monotonic setting

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1, 3, 4, 6	GND	These pads and die bottom must be connected to RF/DC ground.	GND
2	RFIN	This port is DC coupled and matched to 50 Ohms.	RFIN
5	RFOUT	This port is DC coupled and matched to 50 Ohms.	RFOUT
8, 9, 12, 14	$\overline{\text{BIT5}}$, $\overline{\text{BIT3}}$ $\overline{\text{BIT2}}$, $\overline{\text{BIT4}}$	Inverted Control Input. See truth table and control voltage tables.	
7, 10, 11, 13, 15	BIT5, BIT3, BIT1, BIT2, BIT4	Non-Inverted Control Input. See truth table and control voltage tables.	

Outline Drawing



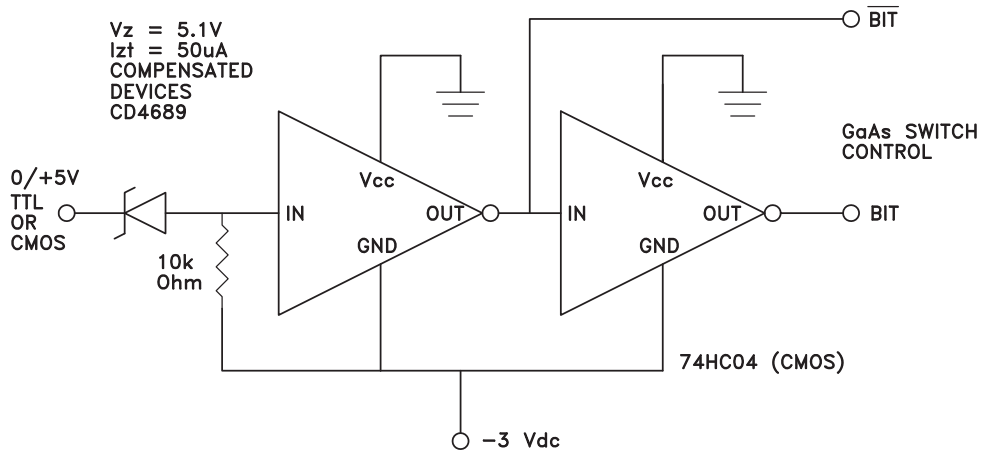
Die Packaging Information [1]

Standard	Alternate
GP-2 (Gel Pack)	[2]

[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. DIE THICKNESS IS 0.004
3. BACKSIDE METALLIZATION: GOLD
4. BACKSIDE METAL IS GROUND
5. BOND PADS METALLIZATION: GOLD
6. OVERALL DIE SIZE ±0.002

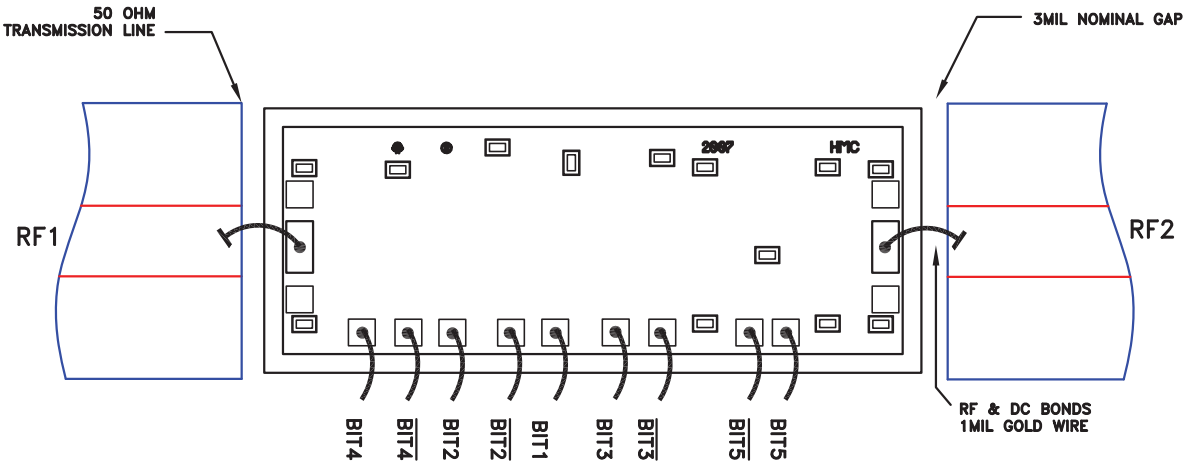
Application Circuit



Note:

This circuit converts a single line positive (0/+5V) control signal to complementary negative (0/-3V) control signals.

Assembly Diagram



Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against > ± 250V ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).