Features

- **Dual ADC**
- **8-bit Resolution**
- **1 Gsps Sampling Rate Per Channel**
- **2 Gsps Equivalent Sampling Rate With One Channel (Interlaced Mode)**
- **500 mVpp Analog Input (Differential Only)**
- **Differential or Single-ended 50 Ω PECL/LVDS Compatible Clock Inputs**
- **LVDS Output Format (100 Ω)**
- **3-wire Serial Interface (16-bit Data, 3-bit Address):**
  - **Full or Partial Standby Mode**
  - **1:2 or 1:1 Selectable Data Output Demultiplexer**
  - **Analog Gain (±1.5 dB) Digital Control**
  - **Input Clock Selection**
  - **Analog Input Switch Selection**
  - **Binary or Gray Logical Outputs**
  - **Asynchronous Data Ready Reset**
  - **Data Ready Delay Adjustable On Both Channels**
  - **Interlacing Functions:**
    - **Offset And Gain (Channel to Channel) Calibration**
    - **Digital Fine SDA (Fine Sampling Delay Adjust) On One Channel**
- **Internal Static Or Dynamic Built-in Test (BIT)**
- **Very Low Input Capacitance: 2 pF**
- **Power Supply: 3.3 V (Analog), 3.3 V (Digital), 2.25 V (Output)**
- **LQFP144**
- **Temperature Range:**
  - **"C" Grade: 0°C < T_A < 70°C**
  - **"I" Grade: -20°C < T_A < 85°C**

Performance

- Low Power Consumption: 1.4 W (Typ)
- Power Consumption in Standby Mode: 60 mW
- 1.5 GHz Full Power Input Bandwidth (-3 dB)
- SINAD = 46 dB Typ (7.3 ENOB), THD = -60 db, SFDR = - 62 dB at Fs = 1 Gsps, Fin = 500 MHz
- 2-tone IMD: -60 dBc Min (499 MHz, 501 MHz) at 1 Gsps
- DNL = 0.25 LSB Typ, INL = 0.5 LSB Typ
- Channel to Channel Input Offset Error: 0.5 LSB Max (After Calibration)
- Gain Matching (Channel to Channel): 0.5 LSB Max (After Calibration)
- Low Bit Error Rate (2.10^{-13}) at 1 Gsps

Application

- Instrumentation
- Satellite Receiver
- Direct RF Down Conversion
- WLAN

Description

- The AD84AD001B is a monolithic low-power (1.4 W typ) dual 8-bit analog-to-digital converter, designed for digitizing in-phase (I) and quadrature (Q) wide bandwidth analog signals at very high sampling rates of up to 1 Gsps. The ability to directly interface I and Q signals makes the AD84AD001B ideal for use in direct satellite demodulation applications or dual channel acquisition applications (instrumentation).
- The AD84AD001B uses an innovative architecture, including an on-chip Sample and Hold (S/H), and is manufactured with an advanced high-speed BiCMOS process.
- The on-chip 2 S/H have a well matched 1.5 GHz full power input bandwidth, providing excellent dynamic performance in undersampling applications (high IF digitizing).
- A 3-wire serial bus interface provides extra adjustment (standby mode, input range, Gray or binary coding).

Dual 8-bit 1 Gsps ADC

AT84AD001B Smart ADC™

Preliminary

Summary

For more information
please contact
hotline-bdc@gfo.atmel.com

2153BS–BDC–08/03

Functional Description

The AT84AD001B is a dual 8-bit 1Gsps ADC based on an advanced high-speed BiCMOS technology.

Each ADC includes a front-end analog multiplexer followed by a Sample and Hold (S/H), and an 8-bit flash-like architecture core analog to digital converter. The output data is followed by a switchable 1:1 or 1:2 demultiplexer and LVDS output buffers (100 W).

Two over-range bits are given for external gain control adjustment on each channel.

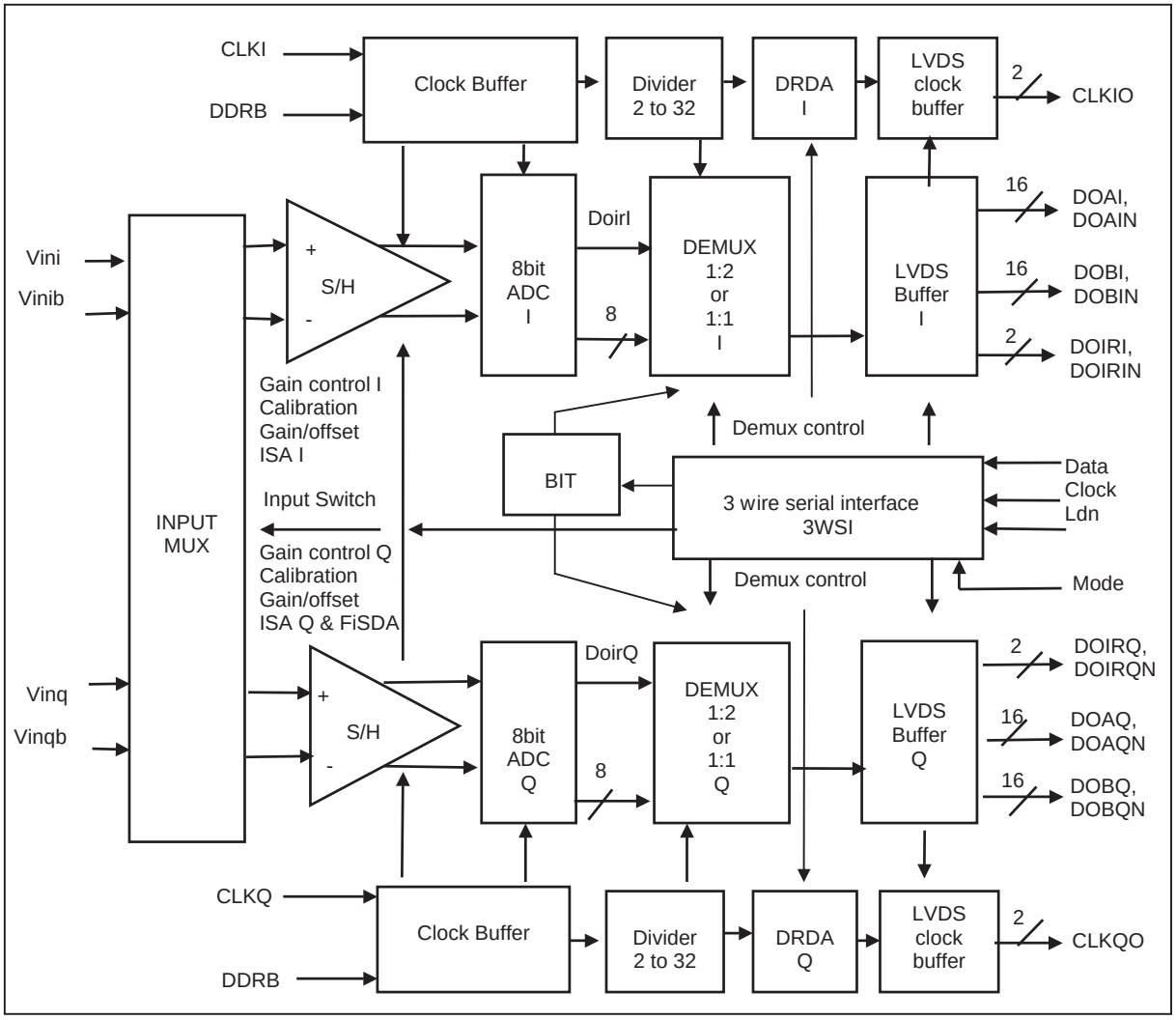
A 3-wire serial interface (3-bit address, 16-bit data) is included to provide several adjustments:

- Analog input range adjustment (±1.5 dB) with 8-bit data control using a 3-wire bus interface (step of 0.18 dB)
- Analog input switch: both ADCs can convert the same analog input signal I or Q
- Gray or binary encoder output. Output format: DEMUX 1:2 or 1:1 with control output frequency on data ready output signal
- Partial or full standby channel I or Q
- Clock selection:
  - Two independent clocks CLKI and CLKQ
  - One master clock (CLKI) with same phase for channel I and Q
  - One master clock but with two phases (CLKI for channel I, CLKIB for channel Q)
- ISA: Internal Settling Adjustment on channel I and Q
- FiSDA: Fine Sampling Delay Adjustment on channel Q
- Adjustable data ready output delay on both channels
- Test mode: decimation mode with a selectable factor (4, 8, 16, 32). Bit error rate (between the 3 most significant bits), ADC gain, offset and DRDA test setting.

A calibration phase is provided to set the two DC offsets of channel I and Q close to code 127.5 and calibrate the two gains to achieve a maximum difference of 0.5 LSB. The offset and gain error can also be set externally via the 3-wire serial interface.

The AD84AD001B works in fully differential mode from analog inputs up to digital outputs. The AD84AD001B features a full power input bandwidth of 1.5 GHz.

Figure 1. Simplified Block Diagram



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

Disclaimer: Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

© Atmel Corporation 2003. **All rights reserved.** Atmel® and combinations thereof are the registered trademarks and Smart ADC™ is the trademark of Atmel Corporation or its subsidiaries. Other terms and product names may be the trademarks of others.

Printed on recycled paper.

2153BS–BDC–08/03 0M