



Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16244T/AT/CT/ET
IDT54/74FCT162244T/AT/CT/ET
IDT54/74FCT166244T/AT//CT
IDT54/74FCT16XH244T/AT/CT/ET
ADVANCE INFORMATION

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015;
 - > 200V using machine model (C = 200pF, R = 0)
 - 25 mil pitch SSOP and Cerpack packages and 19.6 mil pitch TSSOP package
 - Extended commercial range of -40°C to +85°C
- **Features for FCT16244T/AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162244T/AT/CT/ET:**
 - **Balanced Output Drivers:** $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C
- **Features for FCT166244T/AT/CT:**
 - **Light Drive Balanced Output:** $\pm 8\text{mA}$ (commercial), $\pm 6\text{mA}$ (military)
 - Minimal system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.4V at Vcc = 5V, TA = 25°C
- **Features for FCT16XH244T/AT/CT/ET:**
 - Bus Hold retains last active bus state during 3-state
 - Eliminates the need for external pull up resistors.

DESCRIPTION:

The 16-Bit Buffer/Line Driver is for bus interface or signal buffering applications requiring high speed and low power dissipation. These devices have a flow through pin organization, and shrink packaging to simplify board layout. All inputs are designed with hysteresis for improved noise margin. The three-state controls allow independent 4-bit, 8-bit or combined 16-bit operation. These parts are plug in replacements for 54/74ABT16244 where higher speed, lower noise or lower power dissipation levels are desired.

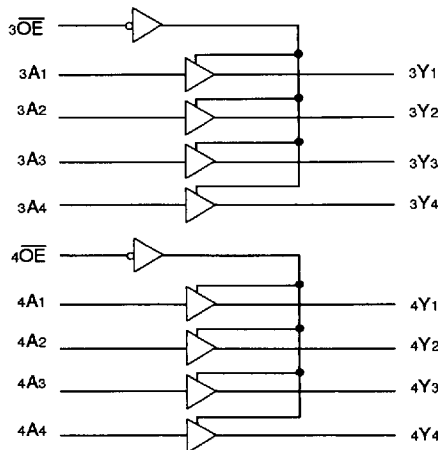
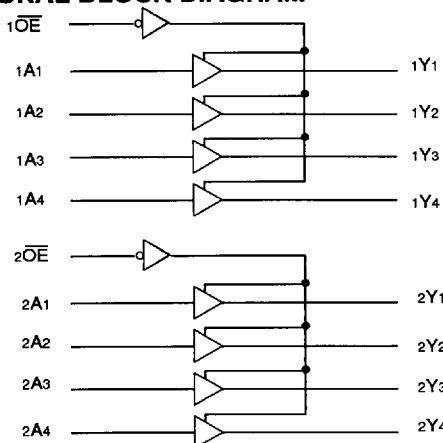
The IDT54/74FCT16244T/AT/CT/ET are ideally suited for driving high capacitance loads (>200pF) and low impedance backplanes. These "high drive" buffers are designed with power off disable capability to allow "live insertion" of boards when used in a backplane interface.

The IDT54/74FCT162244T/AT/CT/ET have balanced output current levels and current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times, reducing the need for external series terminating resistors while still providing very high speed operation for loads of less than 200pF.

The IDT54/74FCT166244T/AT/CT are suited for very low noise, point-to-point driving where there is a single receiver, or a very light lumped load (<50pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors.

The IDT54/74FCT16XH244T/AT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull up resistors.

FUNCTIONAL BLOCK DIAGRAM



The IDT Logo is a registered trademark of Integrated Device Technology, Inc. 2544 drw 01

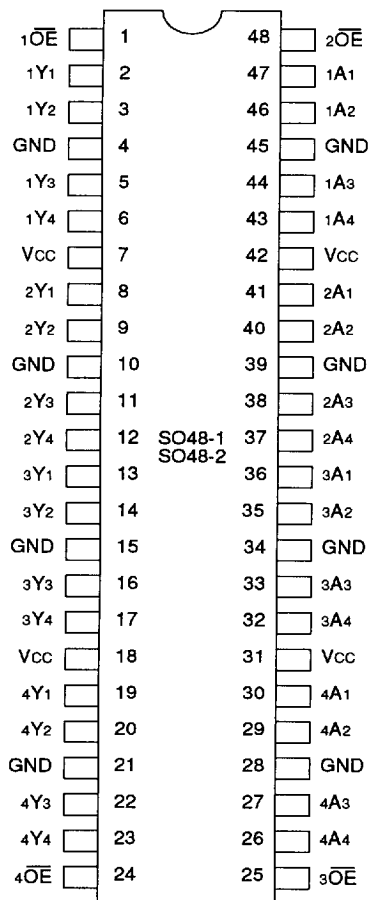
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1993

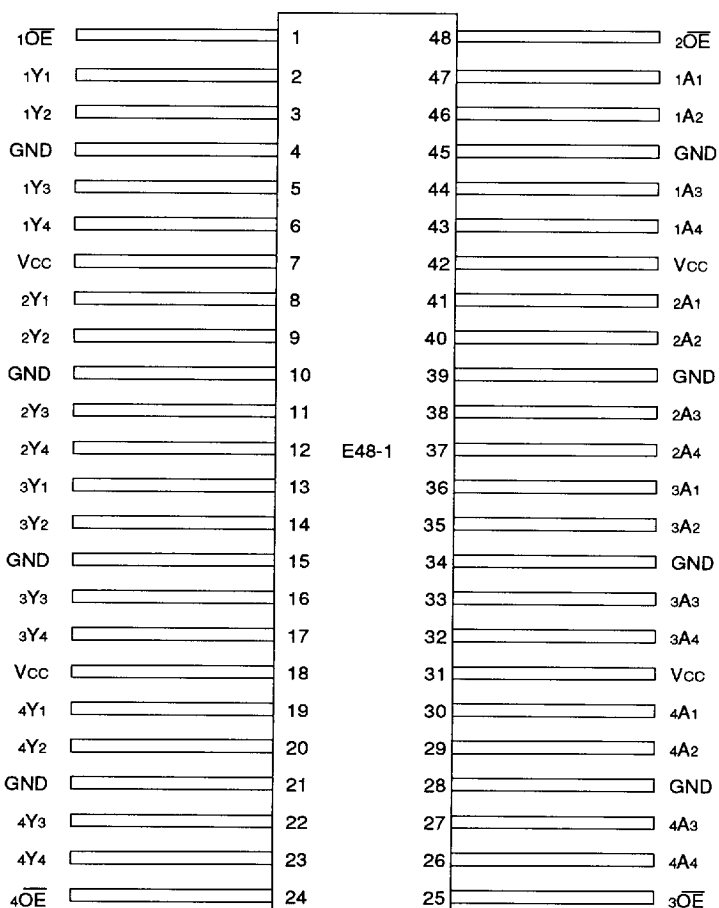
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PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2544 drw 03



CERPACK
TOP VIEW

2544 drw 04

INTEGRATED DEVICE

66E D

4825771 0012623 745

IDT

INTEGRATED DEVICE
66E D
4825771 0012624 681
IDT

PIN DESCRIPTION

Pin Names	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs ⁽¹⁾
XYx	3-State Outputs

NOTE:

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- On FCT16XH244T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
xOE	xAx	XYx
L	L	L
L	H	H
H	X	Z

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NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTerm ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTerm ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC	-0.5 to VCC	V
TA	Operating Temperature	-40 to +85	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT and FCT166XXXT output and I/O terminals.
- Output and I/O terminals for FCT162XXXT and FCT166XXXT.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6.0	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8.0	pF

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NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{IL}	Input LOW Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = GND	—	—	±1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _H	Input Hysteresis	—		—	100	—	mV
I _{CC1} I _{CC2} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁶⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
				—	—	±1	
				±100	—	—	
				±100	—	—	
I _{IL}	Input LOW Current ⁽⁶⁾	V _{CC} = Max.	V _I = GND	—	—	±1	μA
				—	—	±1	
				±100	—	—	
				±100	—	—	
I _{I(HOLD)}	Input Current ⁽⁶⁾	V _{CC} = Min.	V _I = 2.4V	-50	—	—	μA
			V _I = 0.4V	+50	—	—	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _H	Input Hysteresis	—		—	100	—	mV
I _{CC1} I _{CC2} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ±5μA at T_A = -55°C.
- Pins with Bus Hold are identified in the pin description.

OUTPUT DRIVE CHARACTERISTICS FOR FCT16244T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IOH = -3mA	2.5	3.5	—	V
			IOH = -12mA MIL.	2.4	3.5	—	V
			IOH = -15mA COM'L.				
			IOH = -24mA MIL. IOH = -32mA COM'L. ⁽⁴⁾	2.0	3.0	—	V
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 48mA MIL.	—	0.2	0.55	V
			IOL = 64mA COM'L.				
IOFF	Input/Output Power Off Leakage ⁽⁵⁾	VCC = 0V, VIN or VO ≤ 4.5V		—	—	±1	μA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT162244T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
IODL	Output LOW Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V ⁽³⁾		60	115	150	mA
IODH	Output HIGH Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V ⁽³⁾		-60	-115	-150	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IOH = -16mA MIL.	2.4	3.3	—	V
			IOH = -24mA COM'L.				
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 16mA MIL.	—	0.3	0.55	V
			IOL = 24mA COM'L.				

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OUTPUT DRIVE CHARACTERISTICS FOR FCT166244T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
IODL	Output LOW Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V ⁽³⁾		24	48	72	mA
IODH	Output HIGH Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V ⁽³⁾		-24	-48	-72	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IOH = -6mA MIL.	2.4	3.3	—	V
			IOH = -8mA COM'L.				
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 6mA MIL.	—	0.3	0.55	V
			IOL = 8mA COM'L.				

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ± 5μA at TA = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 ⁽⁵⁾	

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$$

$I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$N_{CP} = \text{Number of Clock Inputs at } f_{CP}$

$f_i = \text{Input Frequency}$

$N_i = \text{Number of Inputs at } f_i$

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INTEGRATED DEVICE

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT16244T/FCT162244T

Symbol	Parameter	Condition ⁽¹⁾	FCT16244T/162244T/166244T ⁽⁴⁾				FCT16244AT/162244AT/166244AT ⁽⁴⁾				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
tPHL	xAx to xYx										
tPZH	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
tPZL											
tPHZ	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns
tPLZ											
tSK(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

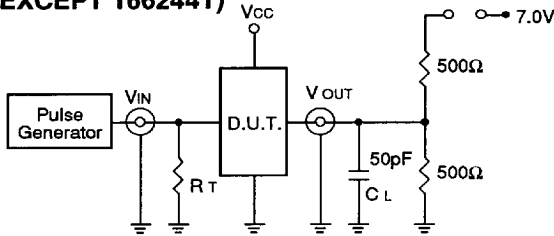
Symbol	Parameter	Condition ⁽¹⁾	FCT16244CT/162244CT/166244CT ⁽⁴⁾				FCT16244ET/162244ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	4.1	1.5	4.6	1.5	3.2	—	—	ns
tPHL	xAx to xYx										
tPZH	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.4	—	—	ns
tPZL											
tPHZ	Output Disable Time		1.5	5.2	1.5	5.7	1.5	3.6	—	—	ns
tPLZ											
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. CL = 20pF for FCT166244T/AT/CT.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS (EXCEPT 166244T)



2544 drw 05

SWITCH POSITION

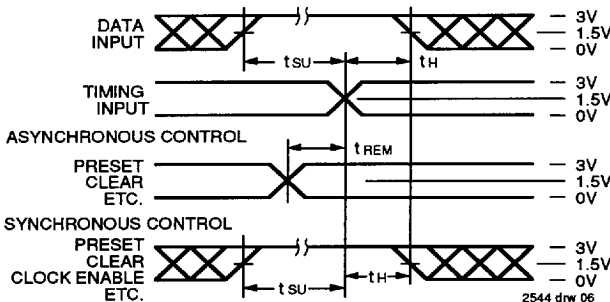
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance; includes jig and probe capacitance.
RT = Termination resistance; should be equal to ZOUT of the Pulse Generator.

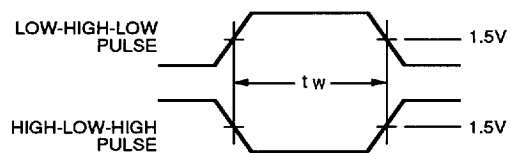
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SET-UP, HOLD AND RELEASE TIMES

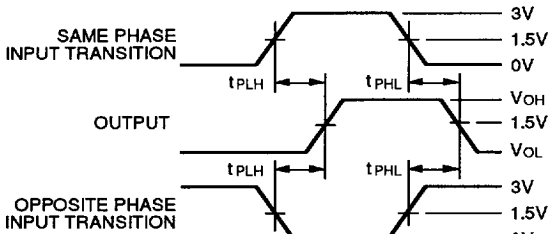


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PULSE WIDTH

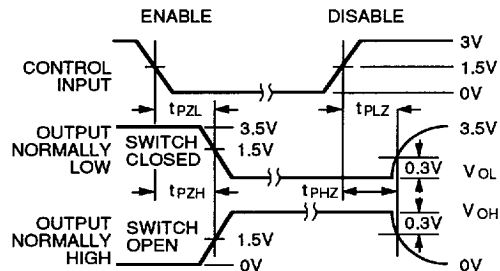


PROPAGATION DELAY



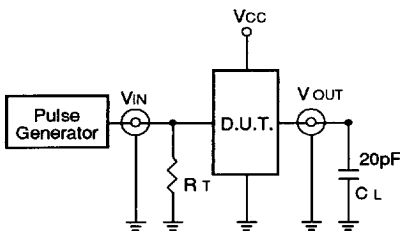
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ENABLE AND DISABLE TIMES



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TEST CIRCUITS FOR 166244T OUTPUTS



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NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $t_r \leq 2.5$ ns; $t_{tr} \leq 2.5$ ns

2544 drw 09

IDT 985 0012630 4825771 66E D INTEGRATED DEVICE

ORDERING INFORMATION

IDT	XX	FCT	X	X	XXXX	X	X		
	Temp. Range		Drive	Bus Hold	Device Type	Package	Process		
								Blank B	Commercial MIL-STD-883, Class B
								PV PA E	Shrink Small Outline Package (SO48-1) Thin Shrink Small Outline Package (SO48-2) CERPACK (E48-1)
								244T 244AT 244CT 244ET	Non-Inverting 16-Bit Buffer/Line Driver
								Blank H	Standard Bus Hold
								16 162 166	16-Bit High Drive 16-Bit Balanced Drive 16-Bit Light Drive
								54 74	-55°C to +125°C -40°C to +85°C

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