Integrated Device Technology, Inc.

CMOS CacheRAM™ 32K x 9-BIT (288K-BIT) BURST COUNTER & SELF-TIMED WRITE

IDT71589SA

FEATURES:

- High density 32K x 9 architecture
- Internal write registers (address, data, and control)
- Self-timed write cycle
- Internal burst read and write address counter
- Clock to data times: 19, 24, and 34ns
- Chip select for depth expansion
- Complies with all timing and signals of 80486 processors up to 40MHz
- I/O pins directly TTL-compatible
- Packaged in plastic 300 mil 32-pin SOJ
- BiCMOS version available for 50MHz and 67MHz systems (IDT71B589)
- SIMM module versions also available from IDT in 128KB (IDT7MP6085 and IDT7MP6086) and 256KB (IDT7MP6087) densities, plus parity

DESCRIPTION:

The IDT71589 is a very high-speed 32K x 9-bit static RAM with full on-chip hardware support of the 80486 CPU interface. This part is designed to facilitate the implementation of the highest-performance secondary caches for the 486 architecture while using low-speed cache-tag RAMs and PALs and consuming the minimum possible board space.

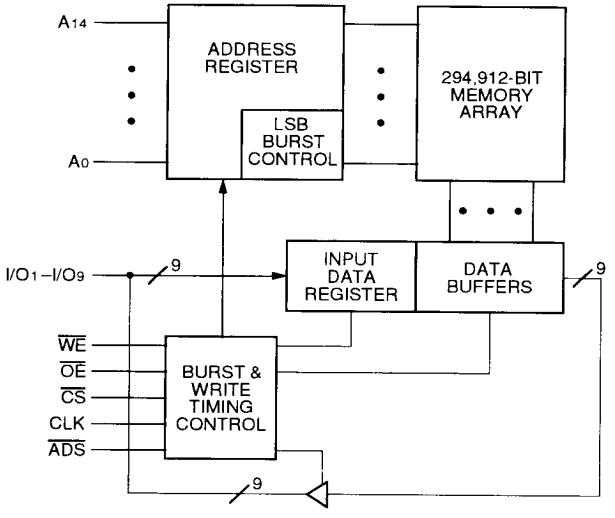
The IDT71589 CacheRAM contains a full set of write data and address registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent four locations using the 486's burst refill sequence on appropriate rising edges of the system clock.

Fabricated using IDT's CMOS high-performance sub-micron technology, this device operates at a very low power consumption and offers a maximum clock to data access time as fast as 19ns.

The IDT71589SA CacheRAMs are packaged in a 32-pin small-outline J-bend (SOJ) package, which allows for a 128KB (plus parity) secondary cache to be built in approximately 1.20 square inches.

FUNCTIONAL BLOCK DIAGRAM



2947 drw 01

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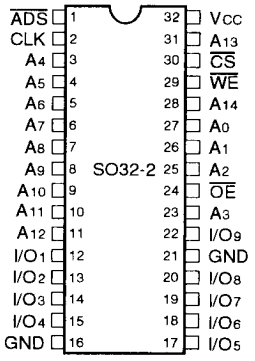
COMMERCIAL TEMPERATURE RANGE **SEPTEMBER 1992**

PIN CONFIGURATION



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SOJ
TOP VIEW

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_1–I/O_9	Data Input/Output
$\overline{CS}$	Chip Select/Count Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{ADS}$	Address Status
CLK	System Clock
GND	Ground
Vcc	Power

2947 tbl 01

SPEED SELECTION

80486 Speed	Suggested IDT71589
25MHz	IDT71589SA35
33MHz	IDT71589SA25
40MHz	IDT71589SA20
50MHz	IDT71B589S14(1, 2)
50MHz	IDT71B589S12(1, 2)
67MHz	IDT71B589S10(1, 3)

2947 tbl 02

NOTES:
1. Separate data sheet available for BiCMOS version.
2. Either part may be used, depending on system loads.
3. Intended for the P5 or future faster versions of the 80486.

COUNT SEQUENCE(1) (A_0, A_1 ONLY)

Start	+1	+2	+3
0	1	2	3
1	0	3	2
2	3	0	1
3	2	1	0

NOTE:
1. The counter wraps around to its starting value and repeats the same sequence after the last count.

2947 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

2947 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2947 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:
1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

2947 tbl 06

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.25V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage (I/O_1–I/O_9)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2947 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 5%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Test Condition	71589SA20[3]		71589SA25		71589SA35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[2]	130	—	130	—	130	—	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	240	—	220	—	200	—	mA

2947 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines are changing.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2947 tbl 09

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz, SOJ package only)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	7	pF

2947 tbl 10

NOTE:
1. This parameter is determined by device characterization but is not production tested.

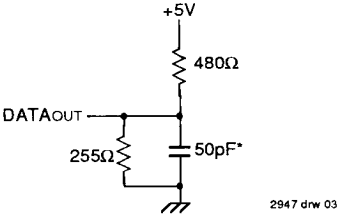

Figure 1. Output Load

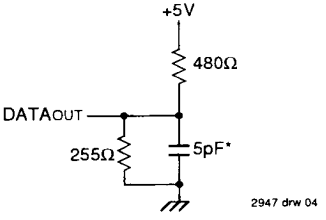

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

FUNCTIONAL DESCRIPTION

The IDT71589 is a very fast 32K x 9 CMOS static CacheRAM with internal edge-triggered registers dedicated to the support of the 486 CPU. These registers support the fastest systems and allow a 128KB or larger cache to be designed to consume the smallest number of chips, the lowest power and board space, and allow the designer to avoid the use of expensive high-speed cache-tag RAMs and PALs.

The internal registers are designed to support two high-speed functions: Burst read cycles, and a late-abort self-timed write cycle.

Burst read cycles are accomplished through the assertion of the $\overline{ADS}$ signal with a valid address input during the rising edge of the clock input. This address will be used to access the data in the CacheRAM during the next clock cycle, and data will be output during the following three cycles in accordance with the 486's burst refill sequence (i.e., during the next cycle the address' LSB is inverted, then the second LSB is inverted as the LSB is restored to its original value, etc.). Since the CacheRAM contains this counter internally, the critical clock-to-data time of even the fastest CPU speeds can be met by using a slower RAM speed grade without resorting to chip-intensive interleaving schemes. Should the $\overline{ADS}$ signal be sampled as valid after having been sampled as invalid, any bursting in process will be reinitialized to the new address, and a new burst cycle will be started. The burst counter wraps around at the end of the sequence and continues to count until stopped by the $\overline{ADS}$ or $\overline{CS}$ inputs. A fast copy-back scheme can harness this capability by reading, then writing the four burst addresses within a single burst cycle.

The self-timed write cycle significantly eases the timing of the address and data inputs during a write cycle, and allows the write/don't write decision to be postponed until the very end of the second cycle of a write cycle. During a write cycle, the address will be strobed into the address register during the first rising edge of the clock after the $\overline{ADS}$ input becomes valid. Data is sampled into the data input register during the next cycle's rising edge, as is the write enable input. If a write has been enabled the data will be written from the address and input data registers into the CacheRAM during the high phase of the clock of that cycle.

A chip select pin is provided to give control over interruption of write cycles and burst read cycles. When the $\overline{CS}$ input is used to interrupt a burst cycle, it operates as a synchronous input to the burst counter. A low level must be present on the chip select input and must satisfy data set-up and hold times in order for the counter to progress to its next state. To stop the counter at its current state, the chip select input must be taken high, and must stay high long enough to satisfy the CacheRAM's data set-up and hold times. The $\overline{CS}$ pin also is used as an auxiliary to the $\overline{WE}$ input. Writes can only be accomplished if both $\overline{CS}$ and $\overline{WE}$ are simultaneously sampled active.

The SOJ package allows for very effective space utilization as illustrated by the IDT Cache-SIMMs. The IDT7MP6086 offers 128KB in a 72-pin SIMM and the IDT7MP6085/7 offer 128KB/256KB in an 80-pin SIMM.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, All Temperature Ranges)

Symbol	Parameter	71589SA20		71589SA25		71589SA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Clock Cycle Time	25	—	30	—	40	—	ns
tCH	Clock Pulse High(1)	10	—	11	—	14	—	ns
tCL	Clock Pulse Low(1)	10	—	11	—	14	—	ns
tSD	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	3	—	4	—	5	—	ns
tHD	Hold Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	2	—	2	—	2	—	ns
tSA	Address Set-up Time	3	—	4	—	5	—	ns
tHA	Address Hold Time	2	—	2	—	2	—	ns
tCD	Clock to Data Valid	—	19	—	24	—	34	ns
tDC	Data Valid After Clock	4	—	4	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	10	ns
tOLZ	Output Enable to Output in Low-Z(2,3)	2	—	2	—	2	—	ns
tOHZ	Output Disable to Output in High-Z(2,3)	—	8	—	9	—	10	ns

NOTES:
1. This parameter is measured as a HIGH time above 2.2V and LOW time below 0.8V.
2. Transition is measured ±200mV from steady state.
3. This parameter is guaranteed with the AC load (Figure 2), but is not production tested.

2947 tbl 11

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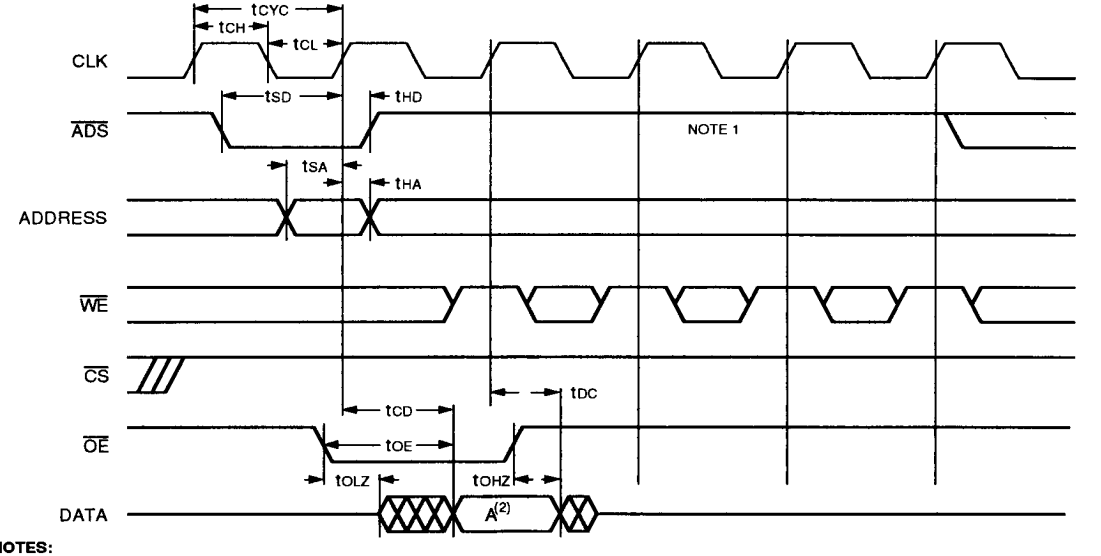
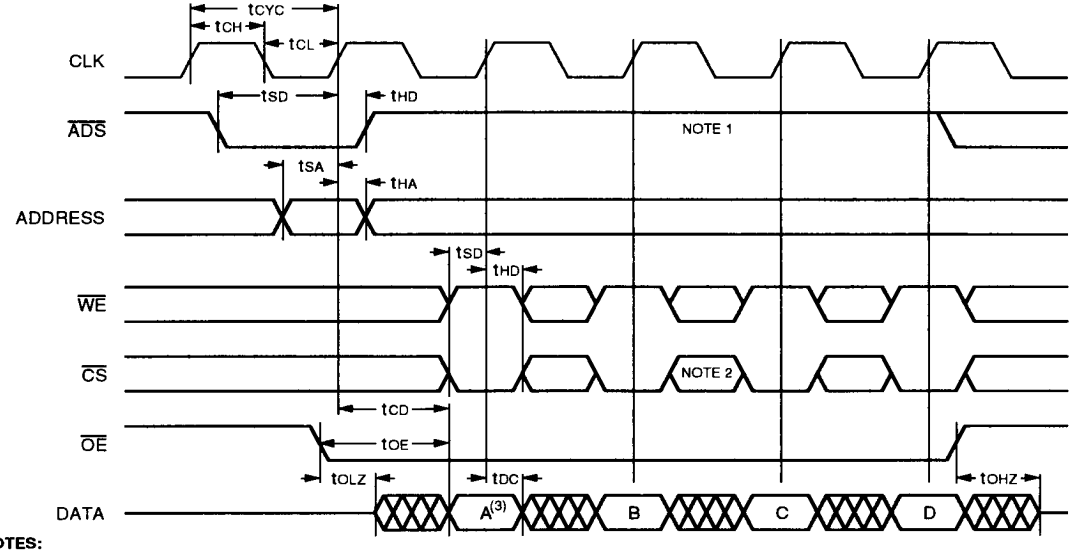
TIMING WAVEFORM OF READ CYCLE



NOTES:
1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. A-Data from address, counter is not imcremented to the next addresses. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}. The output remains unchanged as long as the $\overline{CS}$ is inactive to advance the counter and as long as the $\overline{OE}$ reamins active.

2947 drw 05

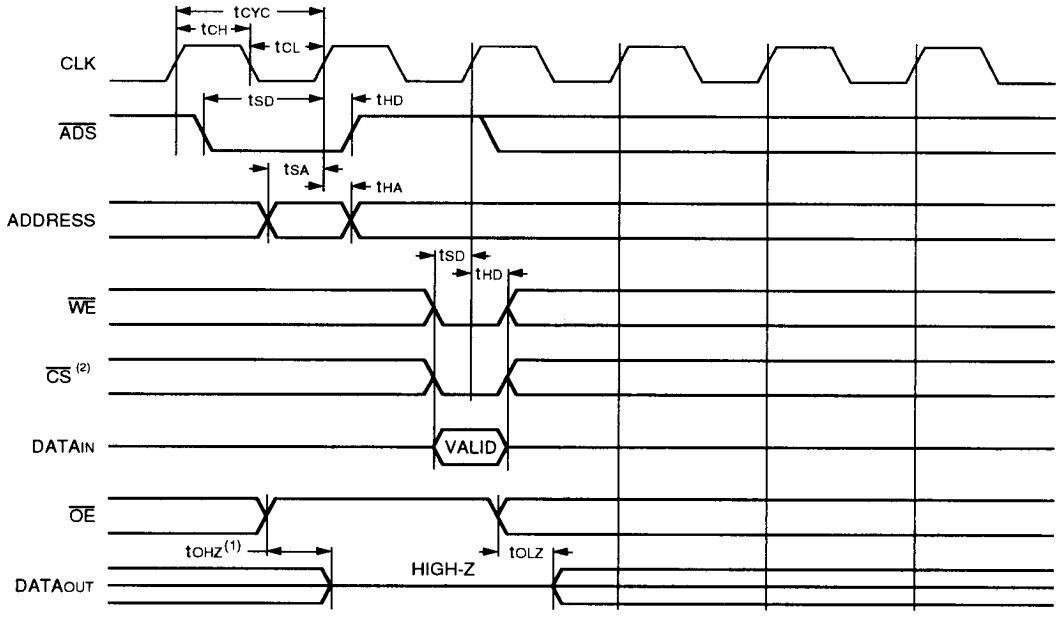
TIMING WAVEFORM OF BURST READ CYCLE



NOTES:
1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}.
3. A-Data from input address. B-Data from input address except A_0 is now $\overline{A}_0$. C-Data from input address except A_1 is now $\overline{A}_1$. D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.

2947 drw 06

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. $\overline{OE}$ must be taken inactive at least as long as $t_{OHZ} + t_{SA}$ before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

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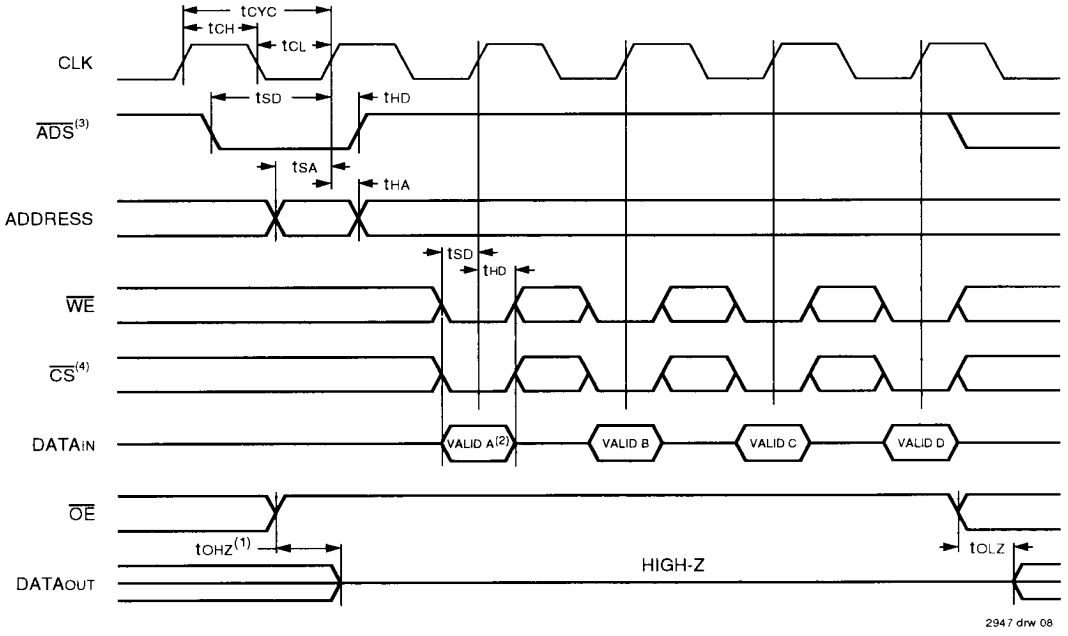
TIMING WAVEFORM OF BURST WRITE CYCLE



NOTES:
1. $\overline{OE}$ must be taken inactive at least as long as $t_{OHZ} + t_{SA}$ before the second rising clock edge of write cycle.
2. A-Data to be written to original input address. B-Data to be written to original input address except A_0 is now $\overline{A}_0$. C-Data to be written to original input address except A_1 is now $\overline{A}_1$. D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

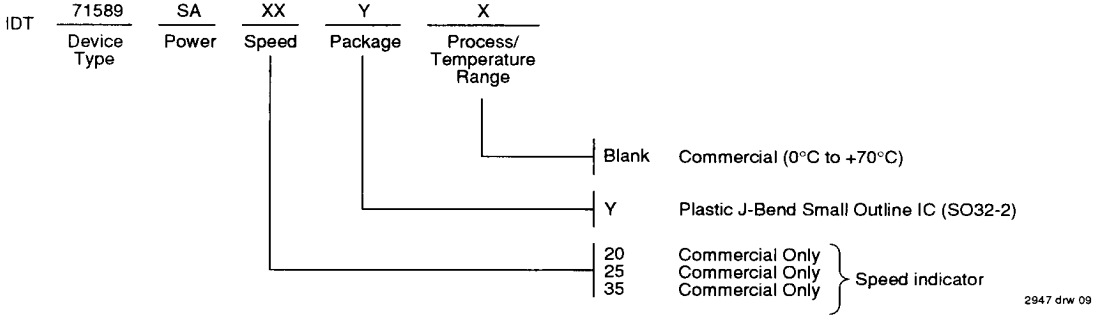
TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	High-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

2947 tbl 12

NOTE:
H = HIGH
L = LOW
X = Don't Care
– = Unrelated
High-Z = High Impedance

ORDERING INFORMATION



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