



Integrated Device Technology, Inc.

**CMOS STATIC RAM
16K (4K x 4-BIT)**

**IDT6168SA
IDT6168LA**

FEATURES:

- High-speed (equal access and cycle time)
 - Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
 - Commercial: 10/12/15/20/25/35ns (max.)
- Low power consumption
 - IDT6168SA
 - Active: 225mW (typ.)
 - Standby: 100μW (typ.)
 - IDT6168LA
 - Active: 225mW (typ.)
 - Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin SOJ, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS™ process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86705 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for high-speed memory applications.

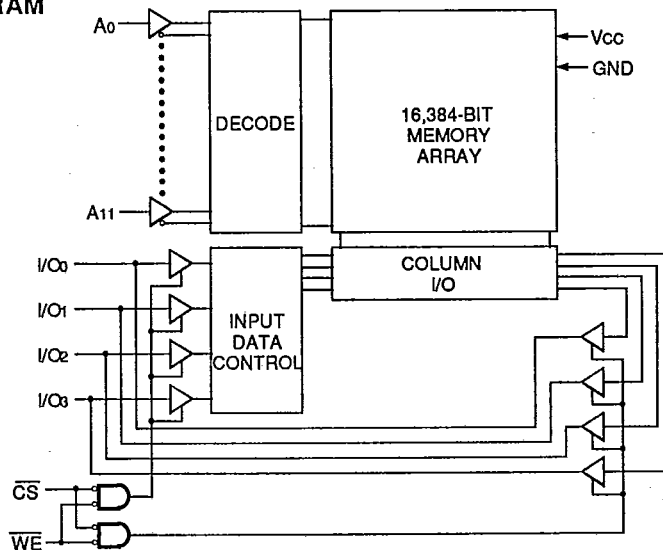
Access times as fast 10ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When \overline{CS} goes high, the circuit will automatically go to, and remain in, a standby mode as long as \overline{CS} remains high. In the standby mode, the device consumes less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300 mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, 20-pin SOJ, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.



FUNCTIONAL BLOCK DIAGRAM



2955 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

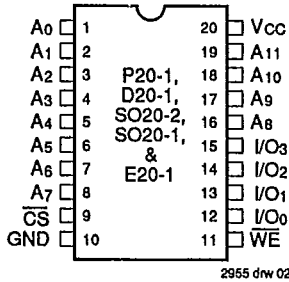
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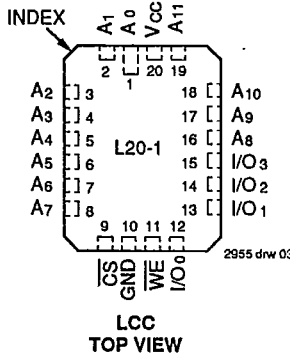
IDT6168SA/LA
CMOS STATIC RAM 16K (4K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



LCC
TOP VIEW

TRUTH TABLE⁽¹⁾

Mode	CS	WE	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care

2955 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2955 tbl 03

PIN DESCRIPTIONS

Name	Description
A ₀ -A ₁₁	Address Inputs
CS	Chip Select
WE	Write Enable
I/O ₀₋₃	Data Input/Output
V _{CC}	Power
GND	Ground

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

2955 tbl 05

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

2955 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(VCC = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = VCC - 0.2V)

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Symbol	Parameter	Power	6168SA10		6168SA12 ⁽⁴⁾		6168SA15 ⁽⁴⁾		6168SA20 6168LA20		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc1	Operating Power Supply Current CS = V _{IL} , Outputs Open, VCC = Max., f = 0 ⁽³⁾	SA	120	—	110	120	110	120	90	100	mA
		LA	—	—	—	—	—	—	70	80	
Icc2	Dynamic Operating Current CS = V _{IL} , Outputs Open, VCC = Max., f = f _{MAX} ⁽³⁾	SA	175	—	165	175	145	165	120	120	mA
		LA	—	—	—	—	—	—	100	110	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , VCC = Max., Outputs Open, f = f _{MAX} ⁽³⁾	SA	65	—	65	65	55	60	45	45	mA
		LA	—	—	—	—	—	—	30	35	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , VCC = Max., VIN ≥ V _{HC} or VIN ≤ V _{LC} , f = 0 ⁽³⁾	SA	20	—	20	20	20	20	20	20	mA
		LA	—	—	—	—	—	—	0.5	5	

DC ELECTRICAL CHARACTERISTICS (Continued)⁽¹⁾

(VCC = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = VCC - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25		6168SA35 6168LA35		6168SA45/55 6168LA45/55		6168SA70 ⁽²⁾ 6168LA70 ⁽²⁾		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc1	Operating Power Supply Current CS = V _{IL} , Outputs Open, VCC = Max., f = 0 ⁽³⁾	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
Icc2	Dynamic Operating Current CS = V _{IL} , Outputs Open, VCC = Max., f = f _{MAX} ⁽³⁾	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , VCC = Max., Outputs Open, f = f _{MAX} ⁽³⁾	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , VCC = Max., VIN ≥ V _{HC} or VIN ≤ V _{LC} , f = 0 ⁽³⁾	SA	2	10	2	10	—	10	—	10	mA
		LA	0.05	0.3	0.05	0.3	—	0.3	—	0.3	

NOTES:

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f = f_{MAX} (all inputs except Chip Select cycling at f = 1/trc). f = 0 means no address or control lines change.
4. Military values are preliminary only.

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS

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VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT6168SA		IDT6168LA		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	MIL COM'L	— 10 2	— 5 2	— 5 2	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC}	MIL COM'L	— 10 2	— 5 2	— 5 2	μA
V _{OL}	Output Low Voltage	I _{OL} = 10mA, V _{CC} = Min.		0.5	—	0.5	V
		I _{OL} = 8mA, V _{CC} = Min.		—	0.4	0.4	V
V _{OH}	Output High Voltage	I _{OL} = -4mA, V _{CC} = Min.		2.4	—	2.4	V

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DATA RETENTION CHARACTERISTICS

(LA Version Only)

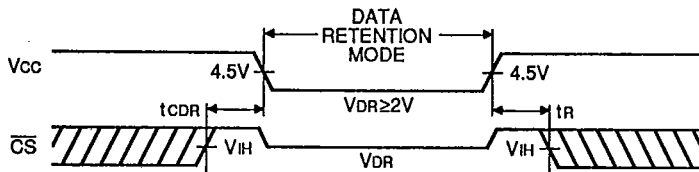
Symbol	Parameter	Test Condition	IDT6168LA			Unit	
			Min.	Typ. ⁽¹⁾	Max.		
V _{DR}	V _{CC} for Data Retention		2.0	—	—	V	
I _{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or ≤ 0.2V	MIL	—	0.5 ⁽²⁾ 1.0 ⁽³⁾	100 ⁽²⁾ 150 ⁽³⁾	μA
			COM'L	—	0.5 ⁽²⁾ 1.0 ⁽³⁾	20 ⁽²⁾ 30 ⁽³⁾	μA
t _{CDR} ⁽⁵⁾	Chip Deselect to Data Retention Time		0	—	—	ns	
t _R ⁽⁵⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	ns	

2955 tbl 09

NOTES:

- TA = +25°C.
- at V_{CC} = 2V
- at V_{CC} = 3V
- t_{RC} = Read Cycle Time.
- This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2955 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

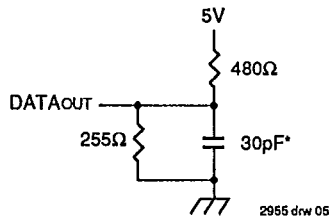


Figure 1. Output Load

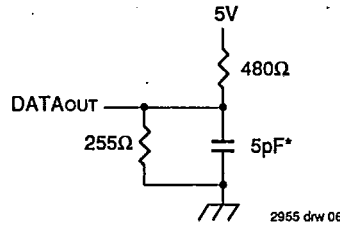


Figure 2. Output Load
(for tHZ, tLZ, tWZ and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10 ⁽³⁾		6168SA12		6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	12	12	15	15	20/25	20/25	20/25	ns
tAA	Address Access Time	10	12	12	15	15	20/25	20/25	20/25	ns
tACS	Chip Select Access Time	10	12	12	15	15	20/25	20/25	20/25	ns
tOH	Output Hold from Address Change	3	3	3	3	3	3	3	3	ns
tLZ	Chip Select to Output in Low Z ⁽²⁾	3	3	3	3	3	5	5	5	ns
tHZ	Chip Deselect to Output in High Z ⁽²⁾	6	7	7	8	8	10	10	10	ns
tPU	Chip Select to Power Up Time ⁽²⁾	0	0	0	0	0	0	0	0	ns
tPD	Chip Deselect to Power Down Time ⁽²⁾	10	12	12	15	15	20/25	20/25	20/25	ns



AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35		6168SA45/55 ⁽¹⁾ 6168LA45/55 ⁽¹⁾		6168SA70 ⁽¹⁾ 6168LA70 ⁽¹⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	35	45/55	45/55	70	70	70	ns
tAA	Address Access Time	35	45/55	45/55	70	70	70	ns
tACS	Chip Select Access Time	35	45/55	45/55	70	70	70	ns
tOH	Output Hold from Address Change	3	3	3	3	3	3	ns
tLZ	Chip Select to Output in Low Z ⁽²⁾	5	5	5	5	5	5	ns
tHZ	Chip Deselect to Output in High Z ⁽²⁾	15	25	25	30	30	30	ns
tPU	Chip Select to Power Up Time ⁽²⁾	0	0	0	0	0	0	ns
tPD	Chip Deselect to Power Down Time ⁽²⁾	35	40/50	40/50	60	60	60	ns

- NOTES:
- 55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
 - This parameter is guaranteed, but not tested.
 - 0° to +70°C temperature range only.

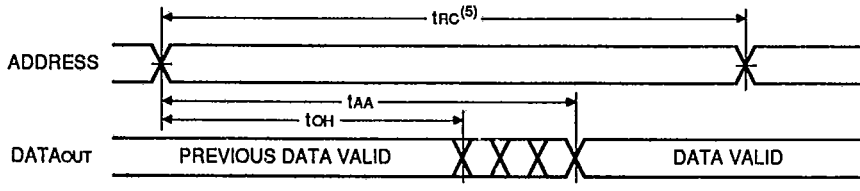
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

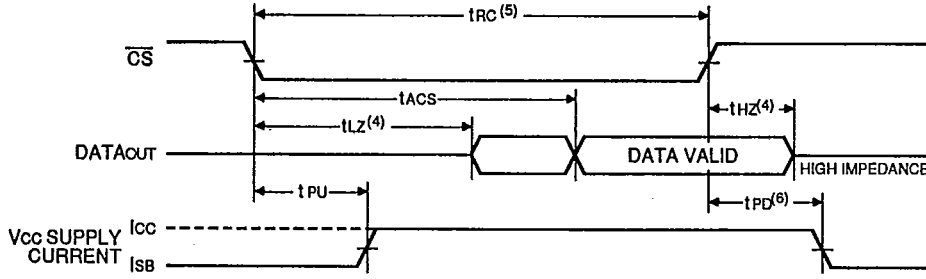
TIMING WAVEFORM OF READ CYCLE NO. 1^(1, 2)

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TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 3)



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NOTES:

1. \overline{WE} is high for READ cycle.
2. \overline{CS} is low for READ cycle.
3. Address valid prior to or coincident with \overline{CS} transition low.
4. Transition is measured $\pm 200mV$ from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is guaranteed and not 100% tested.

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10 ⁽⁴⁾		6168SA12		6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t _{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t _{CW}	Chip Select to End of Write	10	—	12	—	15	—	20	—	ns
t _{AW}	Address Valid to End of Write	10	—	12	—	15	—	20	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	10	—	12	—	15	—	20	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End of Write	7	—	8	—	9	—	10	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t _{WZ}	Write Enable to Output in High Z ⁽²⁾	—	4	—	5	—	6	—	7	ns
t _{OW}	Output Active from End of Write ⁽²⁾	0	—	0	—	0	—	0	—	ns

AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35		6168SA45/55 ⁽¹⁾ 6168LA45/55 ⁽¹⁾		6168SA70 ⁽¹⁾ 6168LA70 ⁽¹⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle								
t _{WC}	Write Cycle Time	30	—	40/50	—	60	—	ns
t _{CW}	Chip Select to End of Write	30	—	40/50	—	60	—	ns
t _{AW}	Address Valid to End of Write	30	—	40/50	—	60	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	30	—	40/50	—	60	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End of Write	15	—	20	—	25	—	ns
t _{DH}	Data Hold Time	0	—	3	—	3	—	ns
t _{WZ}	Write Enable to Output in High Z ⁽²⁾	—	13	—	20/25	—	30	ns
t _{OW}	Output Active from End of Write ⁽²⁾	0	—	0	—	0	—	ns



NOTES:

- 55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
- This parameter is guaranteed, but not tested.
- The specification for t_{OH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{OH} and t_{OW} values will vary over voltage and temperature, the actual t_{OH} will always be smaller than the actual t_{OW}.
- 0° to +70°C temperature range only.

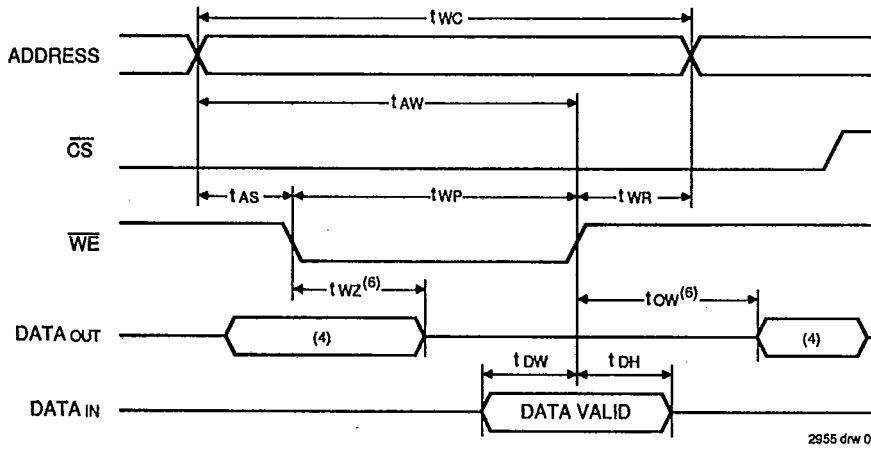
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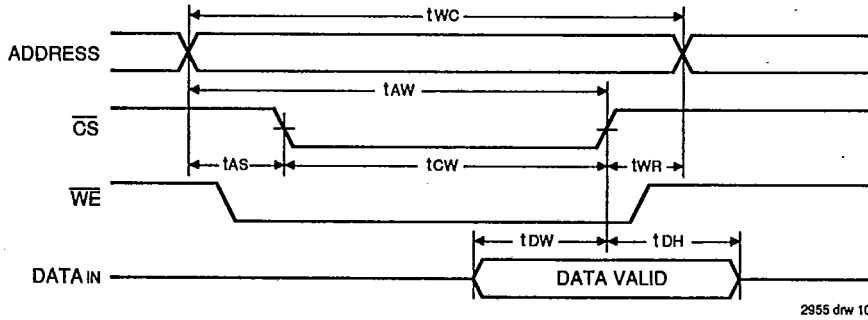
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CMOS STATIC RAM 16K (4K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1, 2, 3, 5)



NOTES:

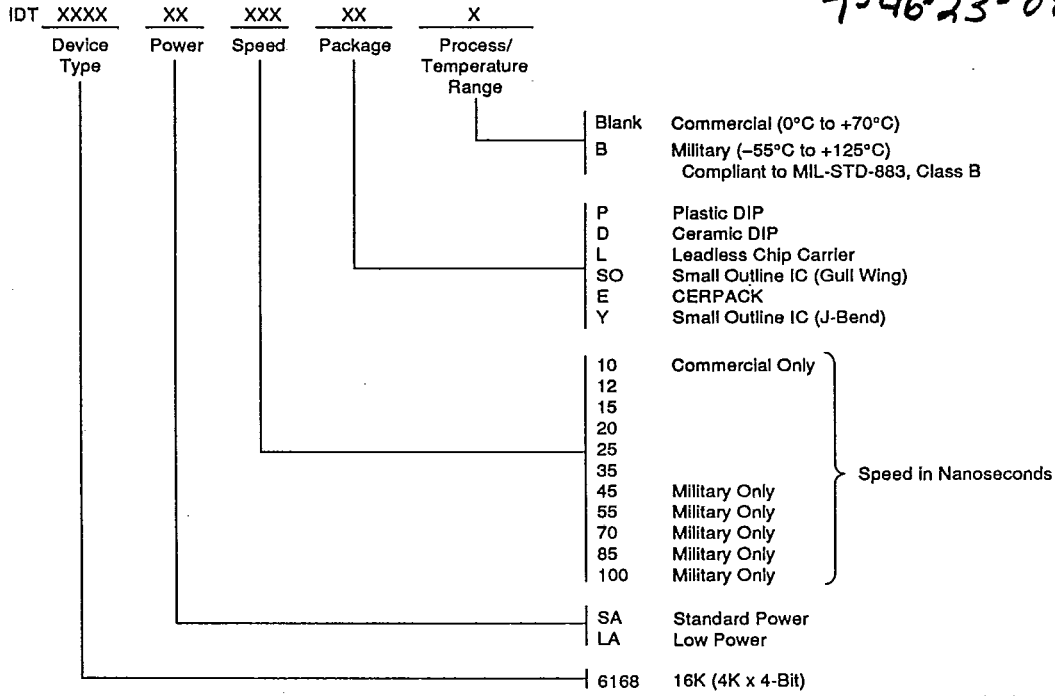
1. \overline{WE} or \overline{CS} must be high during all address transitions.
2. A write occurs during the overlap (t_{WP} or t_{CW}) of a low \overline{CS} and a low \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, the outputs remain in the high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state with a 5pF load (including scope and jig).

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ORDERING INFORMATION

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