2x64Kx16 SRAM, DSP Memory Solution

FEATURES

- Access Times of 10, 12 and 15ns
- DSP Memory Solution
  - Texas Instruments TMS320C5x
- Packaging:
  - 74 pin BGA, JEDEC MO-151
- 3.3V Operating Supply Voltage
- Single Write Control and Output Enable Lines
- One Chip Enable Line per Memory Bank
- 50% Space Savings vs. Monolithic TSOPs
- Upgrade Path Available in Same Footprint
- Multiple Vcc and Vss Pins
- Reduced Inductance and Capacitance

DESCRIPTION

The EDI8L21665VxxBC is a 3.3V, 2x64Kx16 SRAM constructed with two 64Kx16 die mounted on a multi-layer laminate substrate. The device is packaged in a 74 lead, 15mm by 15mm, BGA.

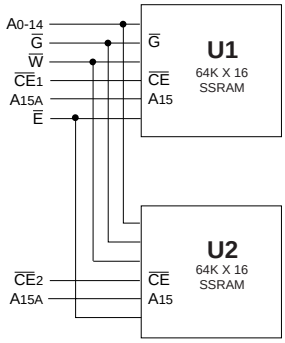
Operating with a 3.3V power supply and with access times as fast as 10ns, the device allows the user to develop a fast external memory for Texas Instuments' TMS320C5x DSP.

The device consists of two separate banks of 64Kx16 of memory. Each bank has a separate Chip Enable pin and higher order address select pin. Bank 'A' is controlled using CE1\ and A15A. Bank 'B' is controlled using CE2\ and A15B. The two banks have common I/Os (DQ0-15) and control lines (WE\, E\ and G\). E\ connects to the mstrb\ pin of the C54x DSPs and is required for write and read timing control.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	
A	Vss	Vcc	Vcc	DQ_{15}	DQ_{14}	Vcc	DQ_{13}	DQ_{11}	DQ_9	DQ_8	NC	A
B	Vss	Vcc	Vcc	Vss	Vss	Vcc	DQ_{12}	DQ_{10}	DQ_4	Vcc	Vcc	B
C	Vss	Vss				Vcc				Vss	Vcc	C
D	Vss	Vss								Vss	Vcc	D
E	Vss	Vss								Vss	Vcc	E
F	A_{15A}	$\overline{CE}_1$								DQ_3	DQ_7	F
G	$\overline{E}$	$\overline{W}$								DQ_5	DQ_0	G
H	Vss	$\overline{CE}_2$								DQ_6	DQ_1	H
I	Vss	A_{14}				Vcc				DQ_2	NC	I
J	Vss	A_{12}	Vcc	A_{10}	A_8	Vss	A_6	A_4	A_2	A_0	$\overline{G}$	J
K	A_{15B}	A_{13}	Vcc	A_{11}	A_9	Vss	A_7	Vss	A_5	A_3	A_1	K
	1	2	3	4	5	6	7	8	9	10	11	

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Symbol	Type	Description
	A_{0-14}	Input	Addresses
	A_{15A}	Input	Addresses: A_{15} on Bank 'A' of memory
	A_{15B}	Input	Addresses: A_{15} on Bank 'B' of memory
	$\overline{W}$	Input	Write Enable: This active LOW input allows a full 16-bit WRITE to occur.
	$\overline{CE}_1$	Input	Chip Enable: This active LOW input is used to enable the 'A' Bank of the device.
	$\overline{CE}_2$	Input	Chip Enable: This active LOW input is used to enable the 'B' Bank of the device.
	$\overline{G}$	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
Various	DQ_{0-15}	Input/Output	Data Inputs/Outputs
Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground
	$\overline{E}$	Input	Enable, This active LOW input controls Write and Read Timing

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-0.5V to 4.6V
V_{IN}	-0.5V to Vcc+0.5V
Storage Temperature	-55°C to +125°C
Junction Temperature	+125°C
Power Dissipation	3 Watts
Short Circuit Output Current (per I/O)	50 mA

* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.2	Vcc+0.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Supply Voltage	Vcc	3.0	3.6	V

CAPACITANCE

(f = 1MHz, V_{IN} = Vcc or Vss)

Parameter	Symbol	Max	Unit
Address Lines	CA	8	pF
Data Lines	CD/Q	17	pF
Control Lines	CC	15	pF

DC ELECTRICAL CHARACTERISTICS

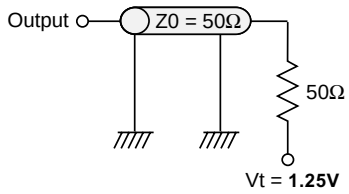
(f = 1MHz, V_{IN} = Vcc or Vss)

Parameter	Symbol	Conditions	Min	Max	Units
Power Supply Current: Operating	ICC1	Device Selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ t_{KC} MIN; Vcc = MAX; outputs open -10ns -12ns -15ns		380 360 260	mA
CMOS Standby	ISB2	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0		60	mA
TTL Standby	ISB3	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; Vcc = MAX; CLK frequency = 0		120	mA
Input Leakage Current	ILI	0V ≤ V_{IN} ≤ Vcc	-5	5	µA
Output Leakage Current	ILO	Output(s) disabled, 0V ≤ V_{OUT} ≤ Vcc	-5	5	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4		V
Output Low Voltage	VOL	IOL = 8.0mA		0.4	V

AC ELECTRICAL CHARACTERISTICS

Read Cycle	Symbol	10ns Min	10ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Read Cycle Time	t_{AVAV}	10		12		15		ns
Address Access Time	t_{AVQV}		10		12		15	ns
Chip Enable Access	t_{ELQV}		10		12		15	ns
Output Hold from Address Change	t_{AVQX}	3		4		4		ns
Chip Enable to Output in Low-Z	t_{ELQX}	3		4		4		ns
Chip Disable to Output in High-Z	t_{EHQZ}		5		6		7	ns
Output Enable access time	t_{GLQV}		5		6		7	ns
Output Enable to Output in Low-Z	t_{GLQX}	0		0		0		ns
Output Disable to Output in High-Z	t_{GHQZ}		5		6		7	ns
Write Cycle								
Write Cycle Time	t_{AVAV}	10		12		15		ns
Chip Enable to End of Write	t_{ELWH}	8		8		9		ns
Address valid to End of Write, with $\overline{G}$ HIGH	t_{AVGHWH}	8		8		9		ns
Address Setup Time	t_{AVWL}	0		0		0		ns
Address Hold from End of Write	t_{AVWH}	8		8		10		ns
Write Pulse Width	t_{WLWH}	10		10		11		ns
Write Pulse Width, with $\overline{G}$ HIGH	t_{WLGHWH}	8		8		9		ns
Data Setup Time	t_{DVWH}	6		6		7		ns
Data Hold Time	t_{WHDX}	0		0		0		ns
Write Disable to Output in Low-Z	t_{WHQX}	3		4		5		ns
Write Enable to Output in High-Z	t_{WLQZ}		5		6		7	ns

AC TEST CIRCUIT

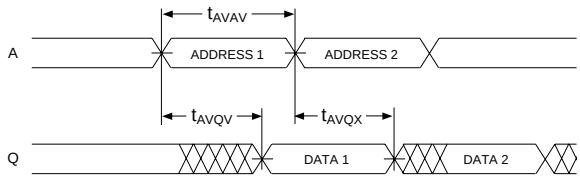


AC Output Load Equivalent

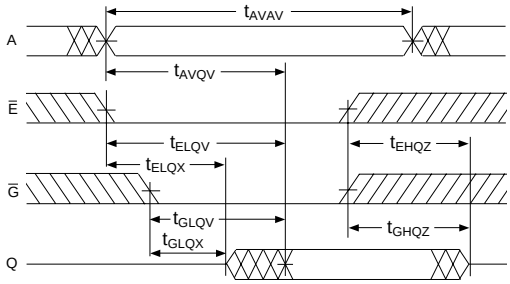
AC TEST CONDITIONS

Parameter	I/O	Unit
Input Pulse Levels	V_{SS} to 3.0	V
Input Rise and Fall Times (max)	1.5	ns
Input and Output Timing Levels	1.5	V
Output Load	See figure, at left	

READ CYCLE TIMING DIAGRAMS

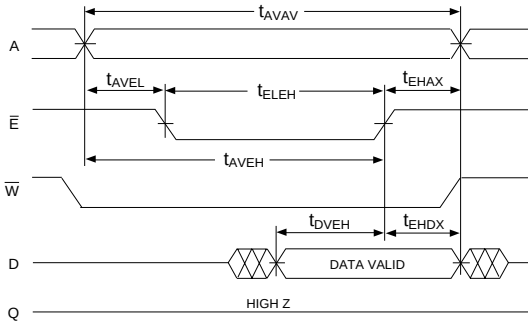


READ CYCLE 1 ($\overline{W}$ HIGH; $\overline{G}$, $\overline{E}$ LOW)



READ CYCLE 2 ($\overline{W}$ HIGH)

WRITE CYCLE TIMING DIAGRAM



WRITE CYCLE 2, $\overline{E}$ CONTROLLED

NOTES: All Writes are $\overline{E}$ controlled when connected to the TMS320C54X. $\overline{E}$ is connected to $\overline{MSTRB}$ and $\overline{W}$ is connected to R/$\overline{W}$ of the TMS320C54X.

ORDERING INFORMATION

Commercial Temperature Range (0°C to +70°C)

Part Number	Speed (ns)	Package No.
EDI8L21665V10BC	10	428
EDI8L21665V12BC	12	428
EDI8L21665V15BC	15	428

Industrial Temperature Range (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L21665V15BI	15	428

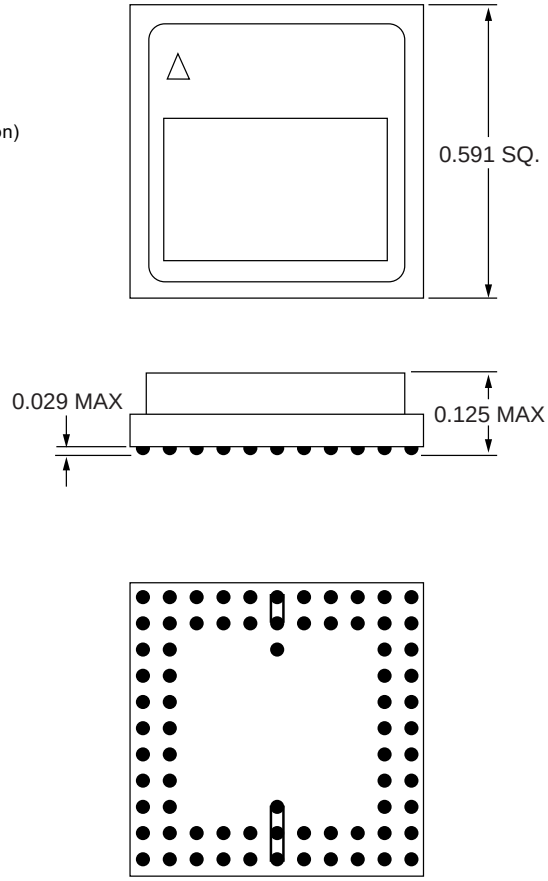
PACKAGE DESCRIPTION: 74 PIN BGA

PACKAGE NO. 428

THERMAL PACKAGE PERFORMANCE:

θ_{JA} = 28°C/Watt (Natural Connection)

θ_{JB} = 4°C/Watt



ALL DIMENSIONS ARE IN INCHES