REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Z. Table I, change t_{S8} and t_{h8}. Changes to figures 1 and 7. Editorial changes throughout.	1988 JUL 26	M.A. Frye

REV																								
SHEET																								
REV	A	A	A	A	A																			
SHEET	22	23	24	25	26																			

REV STATUS OF SHEETS	REV	A	A	A		A	A	A		A	A	A		A	A	A						A	A	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE: 4 Aug 1987

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, BIPOLAR, 16-BIT ERROR DETECTION AND CORRECTION UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87602

SHEET 1 OF 26

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

E5962-E950

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87602	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2960	16-bit error detection and correction unit

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-14 (48-lead, 2.435" x .620" x .225"), dual-in-line package.
Y	(48-lead, 1.235" x .660" x .098"), top braze flat package (see figure 1).
U	C-6 (52-terminal, .761" x .761" x .120"), square chip carrier package.
Z	(52-terminal, .760" x .760" x .075"), thin square chip carrier package (see figure 2).

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	2.2 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and U	See MIL-M-38510, appendix C
Case Y	30°C/W 1/
Case Z	30°C/W 1/
Junction temperature (T_J)	+185°C
DC voltage applied to outputs for high output state	-0.5 V to V_{CC} (maximum)
DC output current, into outputs	30 mA
DC input current	-30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figures 1 and 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Block diagram. The block diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -0.8 mA	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 8 mA	1, 2, 3		0.5	V
Input high voltage	V_{IH}	Guaranteed input logical high voltage for all inputs 1/ 2/		1, 2, 3	2.0		V
Input low voltage	V_{IL}	Guaranteed input logical low voltage for all inputs 1/ 2/		1, 2, 3		0.8	V
Input clamp voltage	V_I	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V	$DATA_{0-15}$ 3/	1, 2, 3		-410	µA
			All other inputs			-360	µA
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.7 V	$DATA_{0-15}$ 3/	1, 2, 3		70	µA
			All other inputs			50	µA
High level input current	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 5.5 V		1, 2, 3		1.0	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Off state (high impedance) output current	I_{OZH} I_{OZL}	V_{CC} = 5.5 V	$DATA_{0-15}$ 3/	V_O = 2.4 V	1, ,2 ,3		70	µA
				V_O = 0.5 V			-410	µA
			SC_{0-6} 3/	V_O = 2.4 V			50	µA
				V_O = 0.5 V			-50	µA
Output short circuit current 4/	I_{OS}	$V_{CC} = V_{CC}(max)+0.5$ V, V_O = 0.5 V			1, 2, 3	-25	-85	mA
Power supply current 5/	I_{CC}	V_{CC} = 5.5 V	T_C = +25°C		1, 2, 3		390	mA
			T_C = -55 to +125°C				400	mA
			T_C = +125°C				345	mA
Functional testing		See 4.3.1c 6/			7, 8			
Combinational delay, 1-4 Input: $DATA_{0-15}$ Output:		C_L = 50 pF						
SC_{0-6}	t_{pd1}	See figure 5 7/			9,10,11		35	ns
$DATA_{0-15}$	t_{pd2}	See figure 5 8/ 9/					73	ns
$\overline{ERROR}$	t_{pd3}	See figure 6 7/					36	ns
$\overline{MULT\ ERROR}$	t_{pd4}	See figure 6 7/					56	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Combinational delay, 5-8 Input: CB_{0-6} (CODE ID_{2-0} = 000,011) Output:		C_L = 50 pF	9,10,11			
SC_{0-6}	t_{pd5}	See figure 5 7/ 10/			30	ns
$DATA_{0-15}$	t_{pd6}	See figure 5 7/ 10/			61	ns
$\overline{ERROR}$	t_{pd7}	See figure 6 7/ 10/			31	ns
$\overline{MULT\ ERROR}$	t_{pd8}	See figure 6 7/ 10/			50	ns
Combinational delay, 9-12 Input: CB_{0-6} (CODE ID_{2-0} = 010, 100, 101, 110, 111) Output:		C_L = 50 pF	9,10,11			
SC_{0-6}	t_{pd9}	See figure 5 7/ 10/			30	ns
$DATA_{0-15}$	t_{pd10}	See figure 5 7/ 10/			50	ns
$\overline{ERROR}$	t_{pd11}	See figure 6 7/ 10/			31	ns
$\overline{MULT\ ERROR}$	t_{pd12}	See figure 6 7/ 10/			37	ns
Combinational delay, 13-16 Input: $\overline{GENERATE}$ Output:		C_L = 50 pF	9,10,11			
SC_{0-6}	t_{pd13}	See figure 5 7/			38	ns
$DATA_{0-15}$	t_{pd14}	See figure 5 9/			69	ns
$\overline{ERROR}$	t_{pd15}	See figure 6 7/			41	ns
$\overline{MULT\ ERROR}$	t_{pd16}	See figure 6 7/			62	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Combinational delay, 17 Input: CORRECT (not internal control mode) Output: $DATA_{0-15}$	t_{pd17}	C_L = 50 pF See figure 5 7/	9,10,11		49	ns
Combinational delay, 18-21 Input: DIAG MODE (not internal control mode) Output: SC_{0-6}	t_{pd18}	C_L = 50 pF See figure 5 7/	9,10,11		58	ns
$DATA_{0-15}$	t_{pd19}	See figure 5 9/			89	ns
$\overline{ERROR}$	t_{pd20}	See figure 6 7/			65	ns
$\overline{MULT\ ERROR}$	t_{pd21}	See figure 6 7/			90	ns
Combinational delay, 22-25 Input: PASS THRU (not internal control mode) Output: SC_{0-6}	t_{pd22}	C_L = 50 pF See figure 5 7/	9,10,11		39	ns
$DATA_{0-15}$	t_{pd23}	See figure 5 7/			51	ns
$\overline{ERROR}$	t_{pd24}	See figure 6 7/			34	ns
$\overline{MULT\ ERROR}$	t_{pd25}	See figure 6 7/			54	ns
Combinational delay, 26-29 Input: CODE ID_{2-0} Output: SC_{0-6}	t_{pd26}	C_L = 50 pF See figure 5 7/	9,10,11		69	ns
$DATA_{0-15}$	t_{pd27}	See figure 5 7/			100	ns
$\overline{ERROR}$	t_{pd28}	See figure 6 7/			68	ns
$\overline{MULT\ ERROR}$	t_{pd29}	See figure 6 7/			90	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Combinational delay, 30-33 Input: LE IN (from latched to transparent)		C_L = 50 pF		9,10,11			
Output: SC_{0-6}	t_{pd30}	See figure 5	7/			44	ns
$DATA_{0-15}$	t_{pd31}	See figure 5	8/ 9/			82	ns
$\overline{ERROR}$	t_{pd32}	See figure 6	7/			43	ns
$\overline{MULT\ ERROR}$	t_{pd33}	See figure 6	7/			66	ns
Combinational delay, 34 Input: LE OUT (from latched to transparent)		C_L = 50 pF		9,10,11			
Output: $DATA_{0-15}$	t_{pd34}	See figure 5	7/			33	ns
Combinational delay, 35-38 Input: LE DIAG (from latched to transparent, not internal control mode)		C_L = 50 pF		9,10,11			
Output: SC_{0-6}	t_{pd35}	See figure 5	9/			50	ns
$DATA_{0-15}$	t_{pd36}	See figure 5	9/			88	ns
$\overline{ERROR}$	t_{pd37}	See figure 6	9/			49	ns
$\overline{MULT\ ERROR}$	t_{pd38}	See figure 6	9/			72	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Combinational delay, 39-42 Input: Internal control mode LE DIAG (from latched to transparent)		C_L = 50 pF	9,10,11			
Output: SC_{0-6}	t_{pd39}	See figure 5 9/			75	ns
$DATA_{0-15}$	t_{pd40}	See figure 5 9/			106	ns
$\overline{ERROR}$	t_{pd41}	See figure 6 9/			74	ns
$\overline{MULT\ ERROR}$	t_{pd42}	See figure 6 9/			96	ns
Combinational delay, 43-46 Input: Internal control mode, $DATA_{0-15}$ (via diagnostic latch)		C_L = 50 pF	9,10,11			
Output: SC_{0-6}	t_{pd43}	See figure 5 9/			75	ns
$DATA_{0-15}$	t_{pd44}	See figure 5 9/			106	ns
$\overline{ERROR}$	t_{pd45}	See figure 6 9/			74	ns
$\overline{MULT\ ERROR}$	t_{pd46}	See figure 6 9/			96	ns
Setup time 1 Hold time 1 Input: $DATA_{0-15}$ To: LE IN	t_{s1} t_{h1}	See figure 7 7/ 7/ 11/ All setup and hold times relative to latch enables	9,10,11	7 7		ns ns
Setup time 2 Hold time 2 Input: CB_{0-6} To: LE IN	t_{s2} t_{h2}	7/ 7/ 11/	9,10,11	5 7		ns ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time 3 Hold time 3 Input: $DATA_{0-15}$ To: LE OUT	t_{s3} t_{h3}	See figure 7 7/ 7/ 11/ All setup and hold times relative to latch enables	9,10,11	50 5		ns ns
Setup time 4 Hold time 4 Input: CB_{0-6} (CODE ID=000, 011) To: LE OUT	t_{s4} t_{h4}	7/ 7/ 11/	9,10,11	38 0		ns ns
Setup time 5 Hold time 5 Input: CB_{0-6} (CODE ID=010, 100, 101, 110, 111) To: LE OUT	t_{s5} t_{h5}	7/ 7/ 11/	9,10,11	30 0		ns ns
Setup time 6 Hold time 6 Input: $\overline{\text{GENERATE}}$ To: LE OUT	t_{s6} t_{h6}	9/ 7/ 11/	9,10,11	46 0		ns ns
Setup time 7 Hold time 7 Input: CORRECT To: LE OUT	t_{s7} t_{h7}	7/ 7/ 11/	9,10,11	28 1		ns ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time 8 Hold time 8 Input: DIAG MODE To: LE OUT	t_{s8} t_{h8}	See figure 7 7/ 7/ 11/ All setup and hold times relative to latch enables	9,10,11	84 0		ns ns
Setup time 9 Hold time 9 Input: PASS THRU To: LE OUT	t_{s9} t_{h9}	7/ 7/ 11/	9,10,11	30 0		ns ns
Setup time 10 Hold time 10 Input: CODE ID_{2-0} To: LE OUT	t_{s10} t_{h10}	7/ 7/ 11/	9,10,11	89 0		ns ns
Setup time 11 Hold time 11 Input: LE IN To: LE OUT	t_{s11} t_{h11}	9/ 7/ 11/	9,10,11	59 5		ns ns
Setup time 12 Hold time 12 Input: $DATA_{0-15}$ To: LE DIAG	t_{s12} t_{h12}	7/ 7/ 11/	9,10,11	7 9		ns ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Enable time 1 Disable time 1 From: $\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1 To: $DATA_{0-15}$	t_{en1} t_{dis1}	C_L = 5.0 pF See figures 5 and 7 7/ 12/ 7/	9,10,11		35 35	ns ns
Enable time 2 Disable time 2 From: $\overline{OE}$ SC To: SC_{0-6}	t_{en2} t_{dis2}	C_L = 5.0 pF See figures 6 and 7 7/ 12/ 7/	9,10,11		35 35	ns ns
Minimum pulse widths LE IN, LE OUT, LE DIAG	t_{pw}	7/	9,10,11	15		ns

1/ These input levels provide zero noise immunity and should only be tested in a static, noise free environment.

2/ Threshold testing: The noise associated with automatic testing, the long inductive cables, and the high gain of bipolar devices frequently give rise to oscillations when testing high speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and ac testing are performed at "hard" input levels rather than at V_{IL} maximum and V_{IH} minimum.

3/ These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with output enables high.

4/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed 1 second.

5/ Worst case I_{CC} is at minimum temperature.

6/ Function testing: Function testing is done with input low less than V_{IL}, and input high greater than V_{IH}. Single trip point at the approximate threshold voltage is used to determine output logic level. In the case of three-state outputs, double point voltages are used.

7/ AC testing: Automatic tester hardware and handler hardware add additional round trip ac delay to test measurements. Actual propagation delay testing may incorporate a correlation factor to negate the additional delay.

8/ DATA in (or LE IN) to correct data out measurement requires timing as shown on figure 7.

9/ AC delay is tested indirectly as it is a combination of other ac parameters as shown in the list of calculated delays below:

LE IN to DATA = (LE IN to SC) - (DATA to SC) + (DATA to DATA)

$\overline{\text{GENERATE}}$ to DATA = ($\overline{\text{GENERATE}}$ to SC) - (CB to SC) + (CB to DATA)

DIAG MODE to DATA = (DIAG MODE to SC) - (CB to SC) + (CB to DATA)

DATA to DATA = (CB to DATA) - (CB to LE OUT setup) + (DATA to LE OUT setup)

INTERNAL CONTROL to DATA = (INTERNAL CONTROL to SC) - (DATA to SC) + (DATA to DATA)

INTERNAL CONTROL to $\overline{\text{ERROR}}$ = (INTERNAL CONTROL to SC) - (DATA to SC) + (DATA to $\overline{\text{ERROR}}$)

INTERNAL CONTROL to $\overline{\text{MULT ERROR}}$ = (INTERNAL CONTROL to SC) - (DATA to SC) + (DATA to $\overline{\text{MULT ERROR}}$)

$\overline{\text{GENERATE}}$ to DATA setup = ($\overline{\text{GENERATE}}$ to DATA) - (DATA to DATA) + DATA setup

$\overline{\text{GENERATE}}$ to DATA hold = PASS THRU hold

LE DIAG to X = LE IN to X + 6 ns, X = any output

LE DIAG to X (INTERNAL CONTROL) = CODE ID to X + 6 ns, X = any output

INTERNAL CONTROL to X = CODE ID to X + 6 ns, X = any output

LE IN to LE OUT setup = (LE IN to SC) - (DATA to SC) + DATA setup

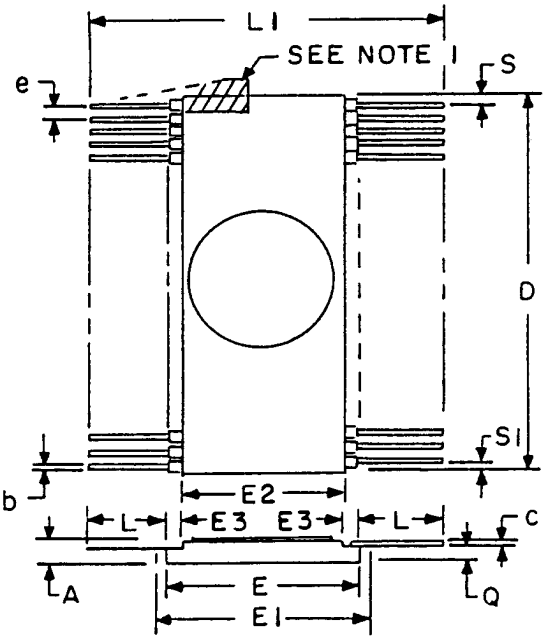
LE IN to LE OUT hold = DATA hold

10/ CB_{0-6} propagation delay and setup time tests use CODE ID = 011 and 010 as the test conditions. Other setup conditions are not performed as they are redundant.

11/ AC hold time parameters are not tested. They are guaranteed by correlation/characterization.

12/ Output enable/disable time tests are performed at system load of 50 pF typically with limits correlated to 5 pF and measured to 0.5 V change of output voltage level.

Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.070	.098	1.78	2.49
b	.017	.023	0.43	0.58
c	.008	.012	0.20	0.30
D	1.185	1.235	30.10	31.37
E	.620	.660	15.75	16.76
E1	---	.720	---	18.29
E2	.520	---	13.21	---
E3	.030	---	0.76	---
e	.045	.055	1.14	1.40
L	.250	.370	6.35	9.40
L1	1.140	1.380	28.96	35.05
Q	.030	.060	0.76	1.52
S	---	.045	---	1.14
S1	.005	---	0.13	---



NOTES
1. Index area: A notch, tab, or pin one identification mark shall be located at within the shade area shown.
2. E1 allows for Ag-Cu alloy brazed overrun.
3. Dimensions b and c increase by 3 mils maximum limit if tin plate or solder dip lead finish, or both is applied.
4. All dimensions are given in inches.

FIGURE 1. Case outline Y.

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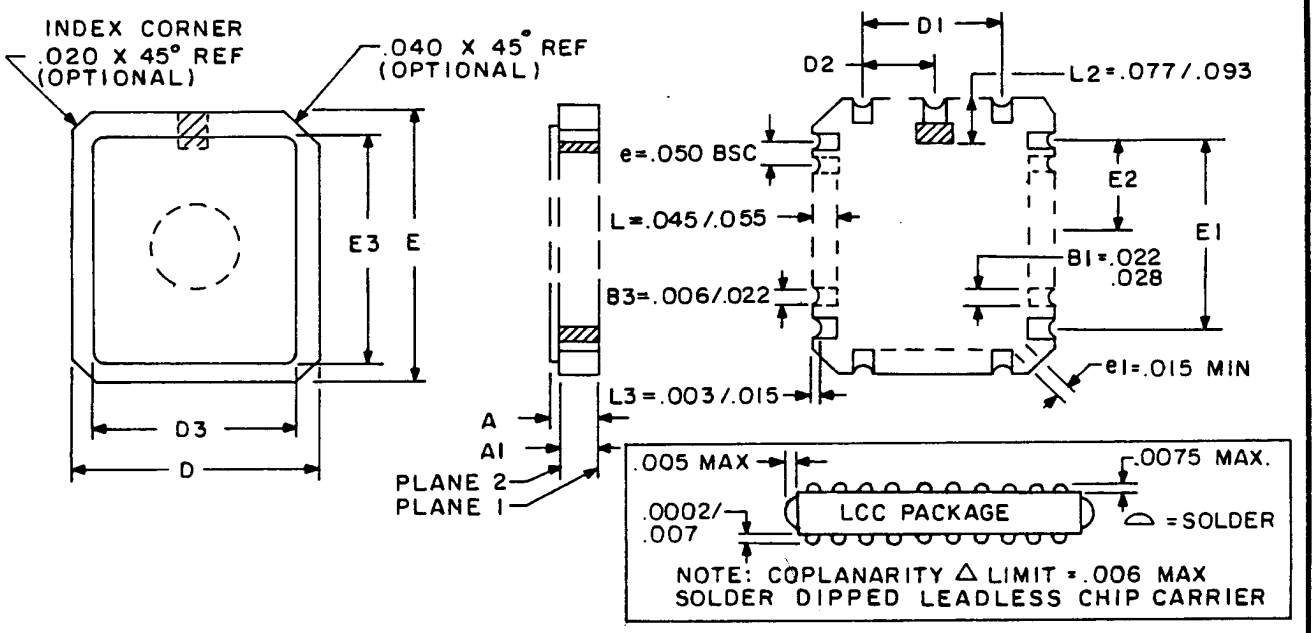


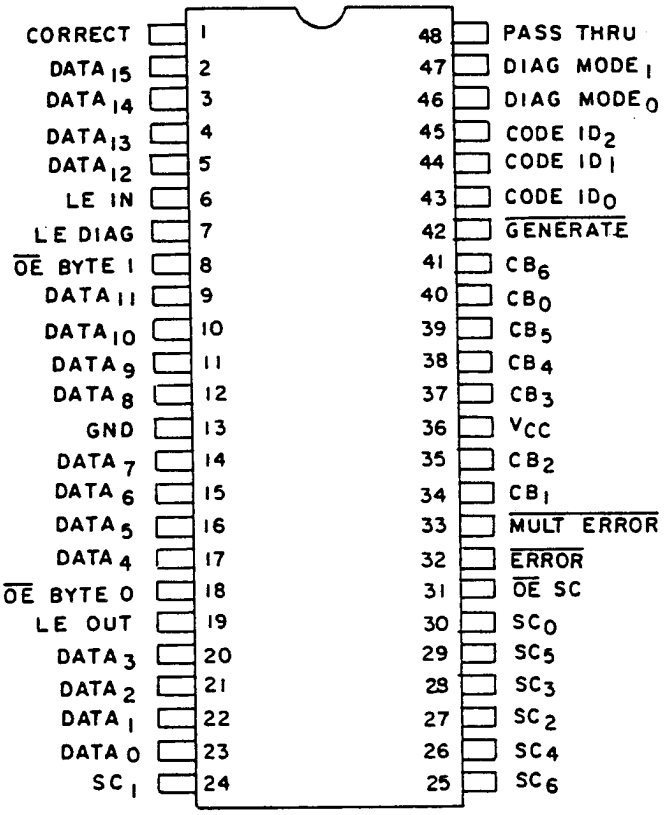
Variations								
A		A1		D/E		D1/E1	D3/E3	ND/NE
Min	Max	Min	Max	Min	Max	BSC	Max	
.064	.075	.054	.065	.740	.760	.600	.660	13

Inches	mm
.003	0.08
.005	0.13
.006	0.15
.007	0.18
.0075	0.19
.015	0.38
.020	0.51
.022	0.56
.028	0.71
.040	1.02
.045	1.14
.054	1.37
.055	1.40
.064	1.63
.065	1.65
.075	1.91
.077	1.96
.093	2.36
.600	15.24
.660	16.76
.740	18.80
.760	19.30

NOTES:
1. A minimum clearance of .015 inch (0.38 mm) shall be maintained between all metallized features. Corner terminal pads may have a .020" x 45° maximum chamfer to accomplish e1 dimension.
2. The lid shall not extend beyond the edges of the body.
3. N is the maximum quantity of terminal positions. ND and NE are the number of terminals along the sides of length D and E respectively.
4. Electrical connection terminals are required on plane 1 and optional on plane 2. However, if plane 2 has such terminals, they shall be electrically connected to opposing terminals on plane 1.
5. The index feature for pin 1 D1, optical orientation or handling purposes shall be within the shaded area shown, and is defined by dimensions B1 and L2.
6. Plane 1 is the heat radiating surface which may optionally be metallized with checkerboard pattern of thermal conduction pads; the number of pads is determined in accordance with MIL-M-38510, appendix C for LCC outlines.
7. The chip carrier corner shape (square, notch, radius, etc.) may vary at the manufacturers option from that shown in the detailed drawing.
8. Dimensions B3 and L3 define the castellation width and depth respectively at any point of the surface. Castellations are required on bottom two layers and optional in the top layer. See MIL-M-38510, appendix C for details.
9. Package shall consist of a minimum of two layers.
10. Solder dipped LCC packages shall conform to MIL-M-38510, appendix C on coplanarity measurements.

FIGURE 2. Case outline Z.

Case outlines X and Y



TOP VIEW

FIGURE 3. Terminal connections.

Case outlines U and Z

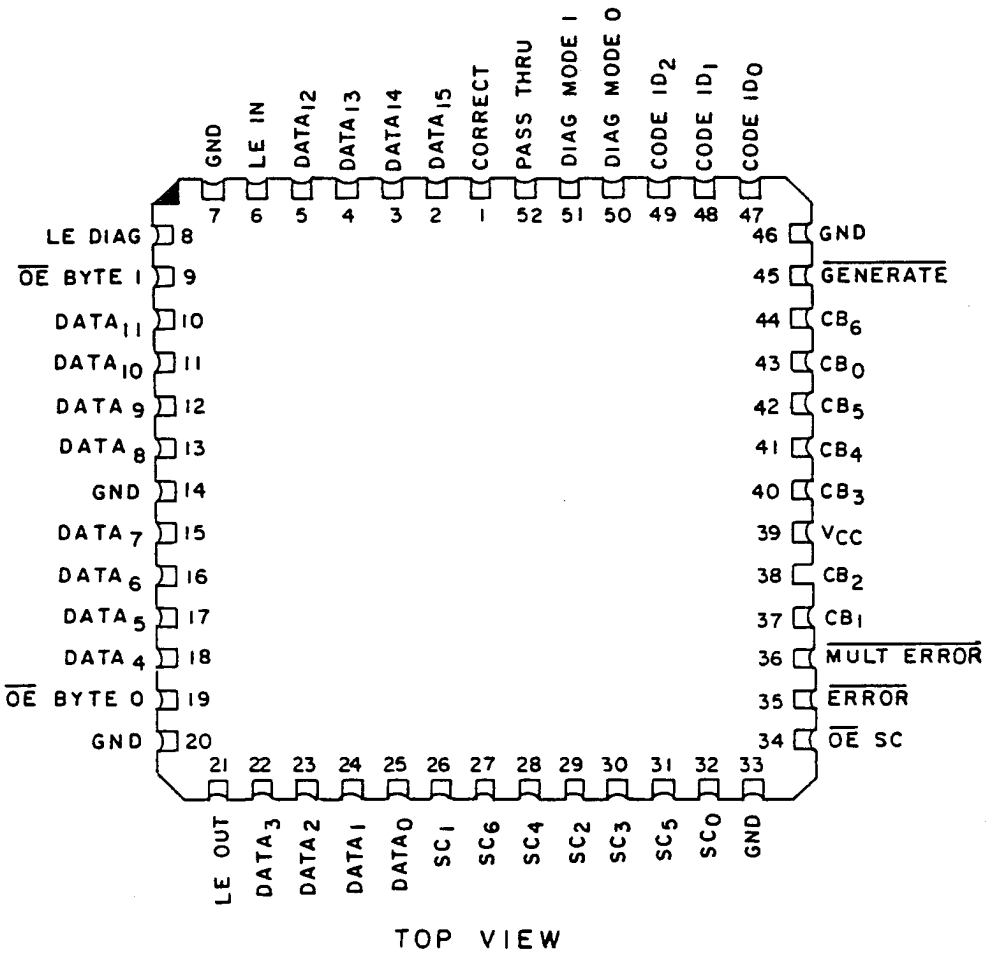


FIGURE 3. Terminal connections - Continued.

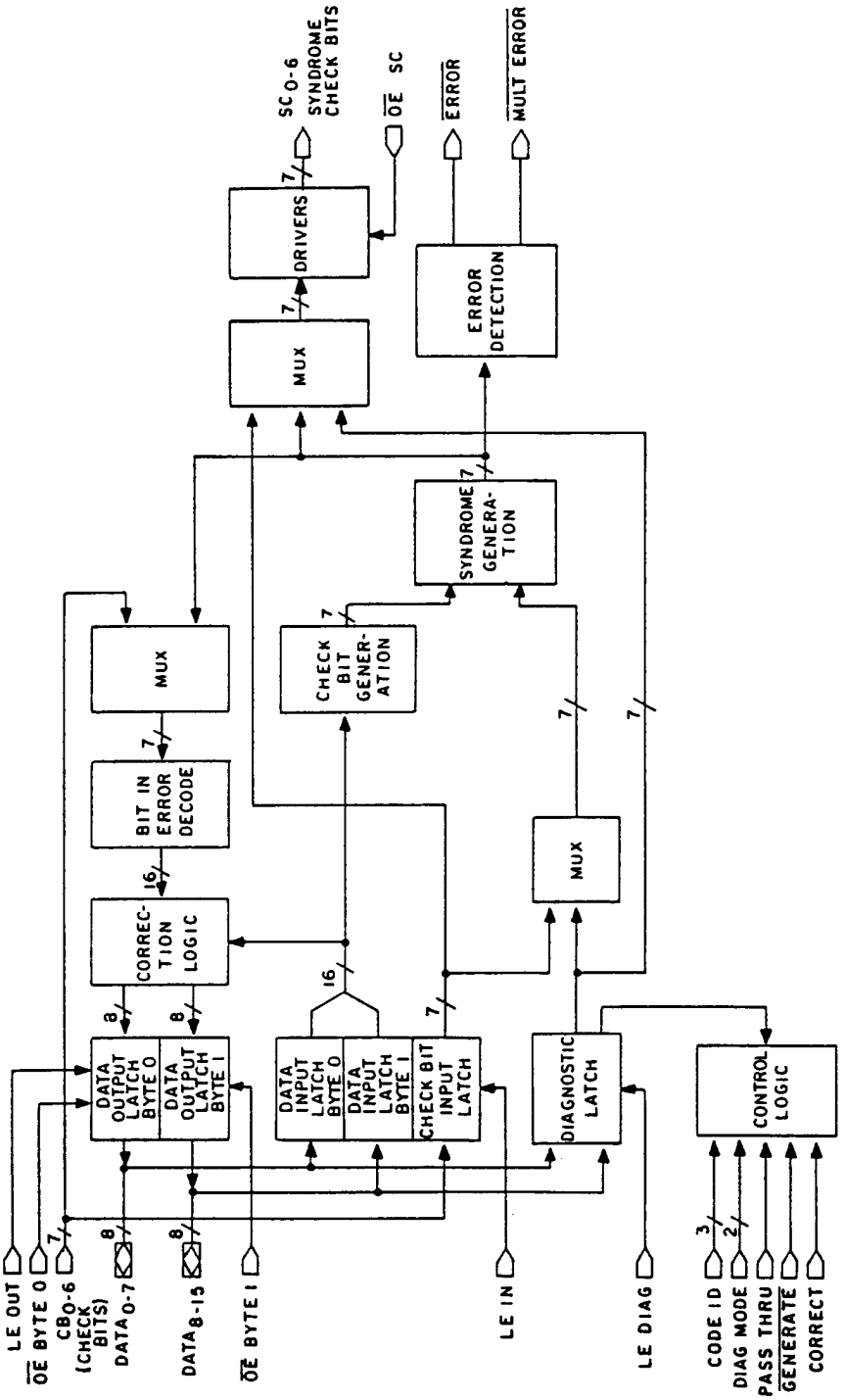


FIGURE 4. Block diagram.

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Test output loads

Pin label	Test circuit	R1	R2
$DATA_{0-15}$	Figure 5	430Ω	1 kΩ
SC_0-SC_6	Figure 5	430Ω	1 kΩ
$\overline{ERROR}$	Figure 6	470Ω	3 kΩ
$\overline{MULT\ ERROR}$	Figure 6	470Ω	3 kΩ

Switching test circuits

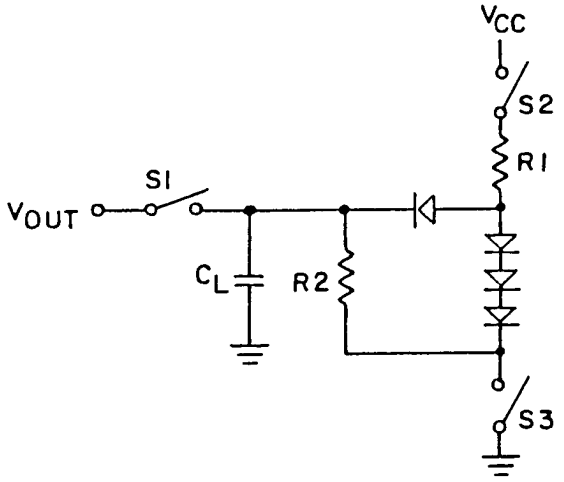

FIGURE 5. Three-state outputs.

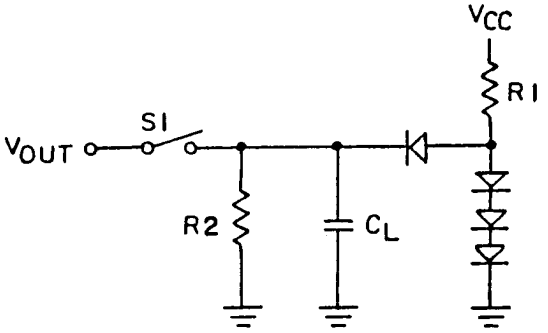

FIGURE 6. Normal outputs.

NOTES:
1. C_L = 50 pF includes scope probe, wiring, and stray capacitances without device in test fixture.
2. S1, S2, and S3 are closed during function test and all ac tests, except output enable tests.
3. S1 and S3 are closed while S2 is open for t_{en} high test.
   S1 and S2 are closed while S3 is open for t_{en} low test.
4. R2 = 1 k for three-state output.
   R2 is determined by the I_{OH} at V_{OH} = 2.4 V for non-three-state outputs.
5. R1 is determined by I_{OL} (MIL) with V_{CC} = 5.0 V minus the current to ground through R2.
6. C_L = 5.0 pF for output disable tests.

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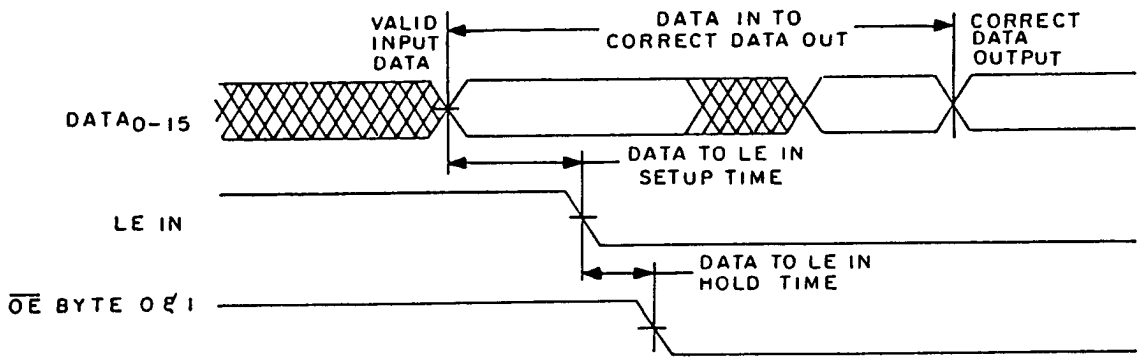

NOTE: Inputs switch between 0 V and 3.0 V at 1 V/ns with measurements made at 1.5 V. All outputs have maximum dc load.

FIGURE 7. Switching waveform.

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3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 testing shall be sufficient to verify the functional operation of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Symbols and definitions.

Pin description

Pin no. Cases X and Y	Pin no. Cases U and Z	Name	I/O	Description
23-20 17-14 12-9 5-2	25-22 18-15 13-10 5-2	$DATA_{0-15}$	I/O	16 bidirectional data lines. They provide input to the data input latch, and diagnostic latch, and receive output from the data output latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.
34,35 37-41	37,38 40-44	CB_{0-6}	I	Seven check bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.
6	6	LE·IN	I	Latch enable - data input latch. Controls latching of the input data. When high, the data input latch and check bit input latch follow the input data and input check bits. When low, the data input latch and check bit input latch are latched to their previous state.
42	45	$\overline{\text{GENERATE}}$	I	Generate Check Bits Input. When this input is low the EDC is in the check bit generate mode. When high, the EDC is in the detect mode or correct mode. In the generate mode the circuit generates the check bits or partial check bits specific to the data in the data input latch. The generated check bits are placed on the SC outputs. In the detect or correct modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the data input latch and check bit input latch. In correct mode, single bit errors are also automatically corrected - corrected data is placed at the inputs of the data output latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.
30,24 27,28 26,29 25	32,26 29,30 28,31 27	SC_{0-6}	O	Syndrome/check bit outputs. These seven lines hold the check/partial-check bits when the EDC is in generate mode, and will hold the syndrome/partial syndrome bits when the device is in detect or correct modes. These are three-state outputs.
31	34	$\overline{\text{OE}}$ SC	I	Output enable - syndrome/check bits. When low the three-state output lines SC_{0-6} are enabled. When high, the SC outputs are in high impedance state.

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Pin description

Pin no. Cases X and Y	Pin no. Cases U and Z	Name	I/O	Description
32	35	$\overline{\text{ERROR}}$	O	Error detected output. When the EDC is in detect or correct mode, this output will go low if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be high. In generate mode, $\overline{\text{ERROR}}$ is forced high. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)
33	36	$\overline{\text{MULT}}$ $\overline{\text{ERROR}}$	O	Multiple errors detected output. When the EDC is in detect or correct mode, this output if low indicates that there are two or more bit errors that have been detected. If high, this indicates that either one or more errors have been detected. In generate mode, $\overline{\text{MULT ERROR}}$ is forced high. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.)
1	1	CORRECT	I	Correct input. When high, this signal allows the correction network to correct any single-bit error in the data input latch (by complementing the bit-in-error) before putting it into the data output latch. When low, the EDC will drive data directly from the data input latch to the data output latch without correction.
19	21	LE OUT	I	Latch enable - data output latch. Controls the latching of the data output latch. When low, the data output latch is latched to its previous state. When high, the data output latch follows the output of the data input latch as modified by the correction logic network. In correct mode, single-bit errors are corrected by the network before loading into the data output latch. In detect mode, the contents of the data input latch are passed through the correction network unchanged into the data output latch. The inputs to the data output latch are unspecified if the EDC is in generate mode.
8, 18	9,19	$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1	I	Output enable - bytes 0 and 1, data output latch. These lines control the three-state outputs for each of the two bytes of the data output latch. When low, these lines enable the data output latch, and when high these lines force the data output latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the data output latch at a time.

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Pin description

Pin no. Cases X and Y	Pin no. Cases U and Z	Name	I/O	Description
48	52	PASS THRU	I	Pass thru input. This line when high forces the contents of the check bit input latch onto the syndrome/check bit outputs (SC_{0-6}) and the unmodified contents of the data input latch onto the inputs of the data output latch.
46,47	50,51	DIAG $MODE_{0-1}$	I	Diagnostic mode select. These two lines control the initialization and diagnostic operation of the EDC.
43-45	47-49	CODE ID_{0-2}	I	Code identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32, and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the diagnostic latch, rather than from the input control lines.
7	8	LE DIAG	I	Latch enable - diagnostic latch. When high the diagnostic latch follows the 16-bit data on the input lines. When low, the outputs of the diagnostic latch are latched to their previous states. The diagnostic latch holds diagnostic check bits, and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

6.5 Approved sources of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8760201XX	34335	AM2960/BXC	
5962-8760201YX	34335	AM2960/BYC	
5962-8760201UX	34335	AM2960/BUA	
5962-8760201ZX	34335	AM2960/BZC	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088

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