TDF8546

I²C-bus controlled 4 × 45 W best efficiency amplifier

Rev. 4 — 19 September 2011 Product data sheet

1. General description

The TDF8546 is one of a new generation of complementary quad Bridge-Tied Load (BTL) audio power amplifiers intended for automotive applications. It has a best efficiency mode with full I²C-bus controlled diagnostics, including start-up diagnostics. The TDF8546 can operate at a battery voltage as low as 6 V making this amplifier suitable for stop/start-car operation.

The new best efficiency principle uses a patented switch technique which reduces switching distortion. To reduce power dissipation, the new best efficiency principle uses the audio information on all four channels instead of only the front or rear signals. Dissipation is more than 65 % less than standard BTL when used for front and rear correlated audio signals. Dissipation is 35 % less than standard BTL when used for uncorrelated (delayed) audio signals between front and rear, and 17 % less for uncorrelated audio signals when the front or rear information is used.

The amplifier uses a complementary DMOS output stage in a Silicon-On-Insulator (SOI)-based BCD process. The DMOS output stage ensures a high power output signal with perfect sound quality. The SOI-based BCD process ensures a robust amplifier, where latch-up cannot occur, with good separation between the four independent channels, with every component isolated and without substrate currents.

2. Features and benefits

- Stop/start-car prepared: keeps operating without audible disturbance during engine start at a battery voltage as low as 6 V
- New best efficiency mode with patented low switching distortion
- Extreme best efficiency mode (uses information from 4 channels) with 17 % less dissipation for uncorrelated signals compared to 2-channel best efficiency mode.
- Operates in either legacy (non I²C-bus) or I²C-bus modes (3.3 V and 5 V compliant)
- Four hardware-programmable I²C-bus addresses
- Can drive 2 Ω and 4 Ω loads
- Speaker fault detection
- Start-up diagnostics with load detection: open, short, present; filtered for door-slam and chatter relays
- AC load (tweeter) detection with low and high current mode
- Gain select after start-up without audible disturbance
- Independent selectable soft mute of front and rear channels
- Programmable gain (26 dB and 16 dB), independently programmable for the front and rear channels

- Line driver mode supports engine start at a battery voltage as low as 6 V (16 dB and mid-tap voltage 0.25V_P)
- Programmable clip detect: 2 %, 5 % or 10 %
- Programmable thermal pre-warning
- Pin STB can be programmed/multiplexed with second-clip detect
- Clip information of each channel can be directed separately to pin DIAG or pin STB
- Independent enabling of thermal-, clip- or load fault information (short across the load or to V_P or to ground) on pin DIAG
- Loss-of-ground and open V_P safe (minimum series resistance required)
- All amplifier outputs short-circuit proof to ground, supply voltage and across the load (channel independent)
- All pins short-circuit proof to ground
- Temperature controlled gain reduction to prevent audio holes at high junction temperatures
- Programmable low battery voltage detection to enable 7.5 V or 6 V minimum battery voltage operation
- Overvoltage protection (load-dump safe up to V_P = 50 V) with overvoltage pre-warning at 16 V
- Offset detection

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω	6	14.4	18	V
I_q	quiescent current	no load	-	260	350	mA
		no load; V_P = 7 V	-	190	-	mA
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; maximum power; V_i = 2 V RMS square wave	37	40	-	W
		R_L = 4 Ω; V_P = 15.2 V; maximum power; V_i = 2 V RMS square wave	41	45	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %	18	20	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %	23	25	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %	40	44	-	W
		R_L = 2 Ω; V_P = 14.4 V; maximum power; V_i = 2 V RMS square wave	58	64	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω; BTL mode	-	0.01	0.1	%
		P_o = 1 W; f_i = 1 kHz; R_L = 4 Ω; high efficiency mode	-	0.015	-	%
		P_o = 4 W; f_i = 1 kHz; R_L = 4 Ω; high efficiency mode	-	0.03	-	%
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz; R_S = 1 kΩ				
		amplifier mode	-	43	65	μV
		line driver mode	-	25	33	μV

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDF8546J/N1	DBS27P	plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)	SOT827-1
TDF8546SD/N1	RDBS27P	plastic rectangular-DIL-bent-SIL (reverse bent) power package; 27 leads (row spacing 2.54 mm)	SOT878-1

5. Block diagram

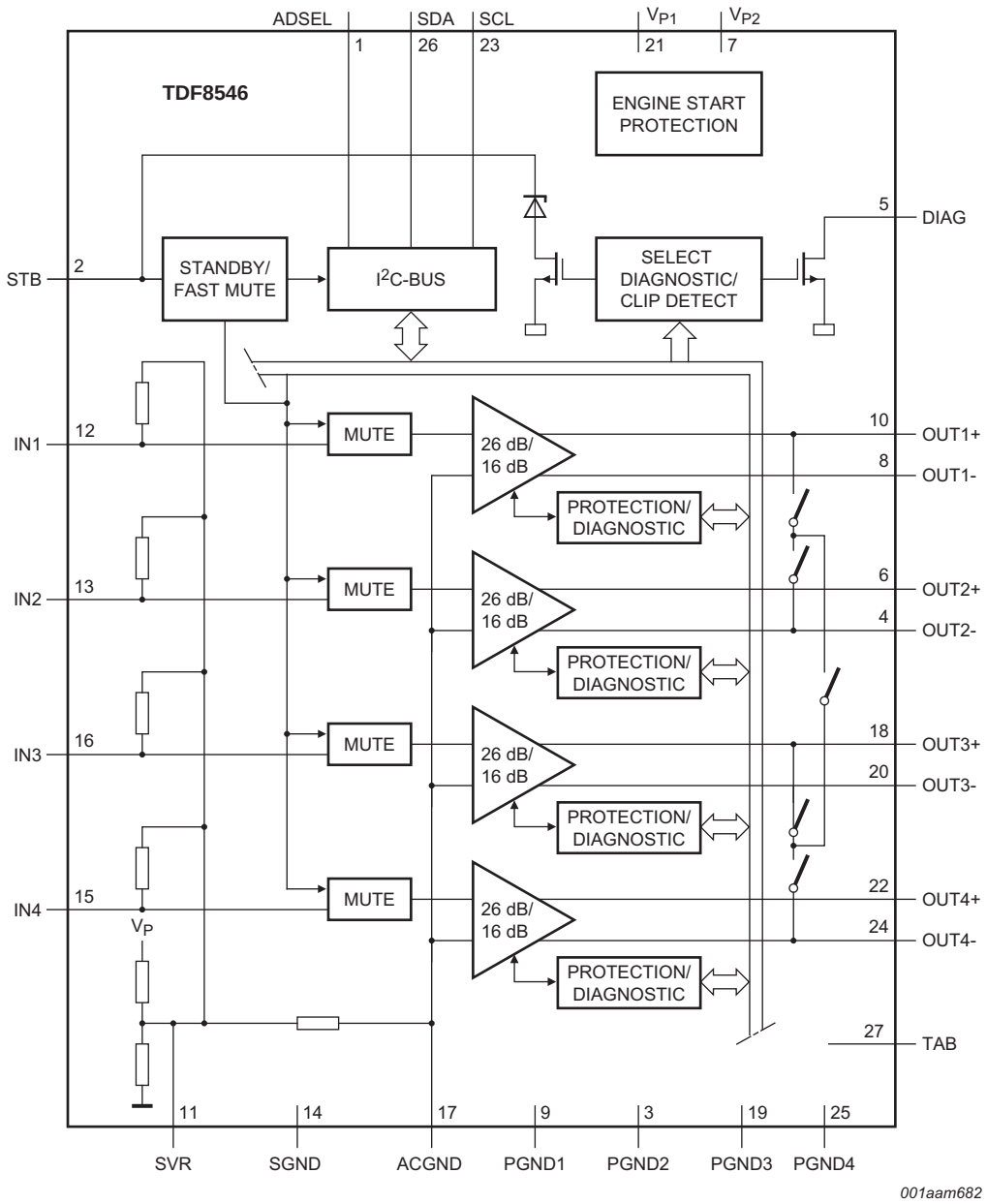


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

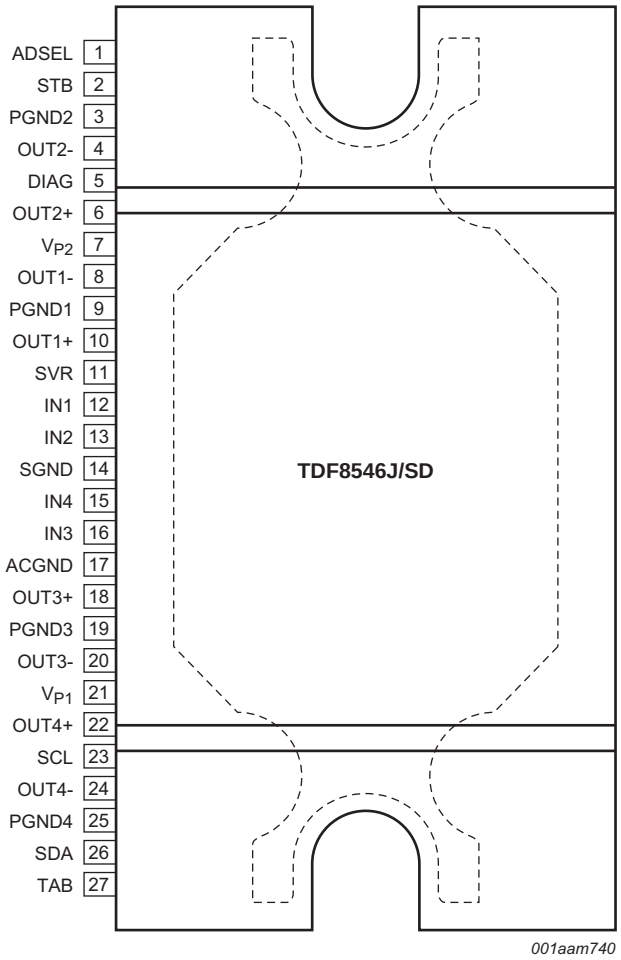


Fig 2. Pin configuration of TDF8546J/SD (packages DBS27P and RDBS27P)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
	TDF8546J/SD	
ADSEL	1	I²C-bus address select
STB	2	stand-by (I²C-bus mode) or mode pin (legacy mode) programmable second clip indicator
PGND2	3	channel 2 power ground
OUT2−	4	channel 2 negative output (right rear)
DIAG	5	diagnostic and clip detection output
OUT2+	6	channel 2 positive output (right rear)
V_{P2}	7	power supply voltage 2
OUT1−	8	channel 1 negative output (right front)
PGND1	9	channel 1 power ground
OUT1+	10	channel 1 positive output (right front)
SVR	11	half supply voltage filter capacitor
IN1	12	channel 1 input
IN2	13	channel 2 input
SGND	14	signal ground
IN4	15	channel 4 input
IN3	16	channel 3 input
ACGND	17	AC ground
OUT3+	18	channel 3 positive output (left front)
PGND3	19	channel 3 power ground
OUT3−	20	channel 3 negative output (left front)
V_{P1}	21	power supply voltage 1
OUT4+	22	channel 4 positive output (left rear)
SCL	23	I²C-bus clock input
OUT4−	24	channel 4 negative output (left rear)
PGND4	25	channel 4 power ground
SDA	26	I²C-bus data input and output
TAB	27	heatsink connection; must be connected to ground

7. Functional description

The TDF8546 is a complementary quad BTL audio power amplifier made with SOI-based BCDMOS technology. It contains four independent amplifiers in a BTL configuration; see Figure 1. The amplifier remains fully operational at a battery voltage as low as 6 V. Below 6 V, a crank detector is activated to shut down the amplifier without audible plops.

A new best efficiency principle uses a patented switch technique that reduces the switching distortion and reduces dissipation by using the audio information on all four channels instead of only the front or rear signals.

The TDF8546 is protected against overvoltage, short-circuit, overtemperature, open ground and open V_P connections.

The diagnostics for temperature and clip levels are programmable via the I²C-bus, and the information indicated at diagnostic pins DIAG and STB is selectable. The status of each amplifier can be read separately for output offset, load or no load, short-circuit or speaker falsely connected.

During amplifier start-up the built-in start-up diagnostics can be used to detect shorted load, open load, short to ground or short to V_P. The TDF8546 is software and hardware compatible with its predecessors: stand-alone amplifiers TDA8594 and TDA8595.

A resistor can be connected to pin ADSEL and ground to emulate an I²C-bus address that is determined by the resistor value. Up to four different I²C-bus addresses are possible; see Table 8. If pin ADSEL is shorted to ground, the TDF8546 operates in legacy mode. In this mode, the I²C-bus is not needed and the function of pin STB changes from 2-level (stand-by mode and on mode) to a 3-level pin (stand-by mode, on mode and mute).

The output stage of an amplifier channel consists of two PDMOS power transistors and two NDMOS transistors in BTL configuration and ensures a high power output signal with perfect sound quality. The BCDMOS process is used with an isolated SOI substrate which ensures a robust amplifier, where latch-up cannot occur, and low crosstalk between the channels with every component isolated, without substrate currents.

The input stage is biased (at 0.23 × battery voltage + 1.4 V) and can accept an input voltage of up to 8 V (peak). The DC input bias voltage can be measured on pin SVR. At a bias voltage of 0.23 × battery voltage + 1.4 V (= 4.7 V at a supply of 14.4 V), the input capacitors can remain biased even with an engine start crank as low as 6 V. If the input capacitors are allowed to discharge quickly, a small input signal is caused by a different input time-constant due to a different AC ground and input capacitor. This small input signal would be amplified to the output resulting in an audible plop noise.

7.1 Start-up and shut-down sequence

The capacitor on pin SVR is used for smooth start-up and shut-down which prevents the amplifier from producing switch-on or -off plop noise. Increasing the SVR capacitor value increases start-up and shut-down time.

If the amplifier is switched on in I²C-bus mode (IB1[D0] = 1) or in legacy mode (V_{STB} > 2.5 V), the amplifier output voltage rises to 1.4 V less than half the supply voltage with the output muted. When the output voltage is half the supply voltage, the start-up mute is either released, if the I²C-bus is set to unmute (V_{STB} > 5.9 V in legacy mode), or stays in mute if the bits are set to mute (2.5 V < V_{STB} < 4.5 V in legacy mode).

To enable short start-up times, the 70 kΩ input resistor is reduced to 3 kΩ during start-up until just before the start-up mute release.

The speaker fault detection (double-fault condition, one side of the speaker connected to ground and one side connected to one output) is detected during start-up, just before mute release.

If the amplifier is switched off by I²C-bus (IB1[D0] = 0) the soft mute is activated and the capacitor on pin SVR is discharged. If the amplifier is switched off in legacy mode, pin STB must be set to mute for 50 ms to ensure a low switch-off plop and then pin STB can be set to ground which discharges the SVR capacitor.

If the amplifier is switched off by pulling pin STB LOW, the amplifier is muted (fast mute) and then the capacitor on pin SVR is discharged. This fast mute can be used in I²C-bus and legacy mode, when for instance an external engine start detection is used.

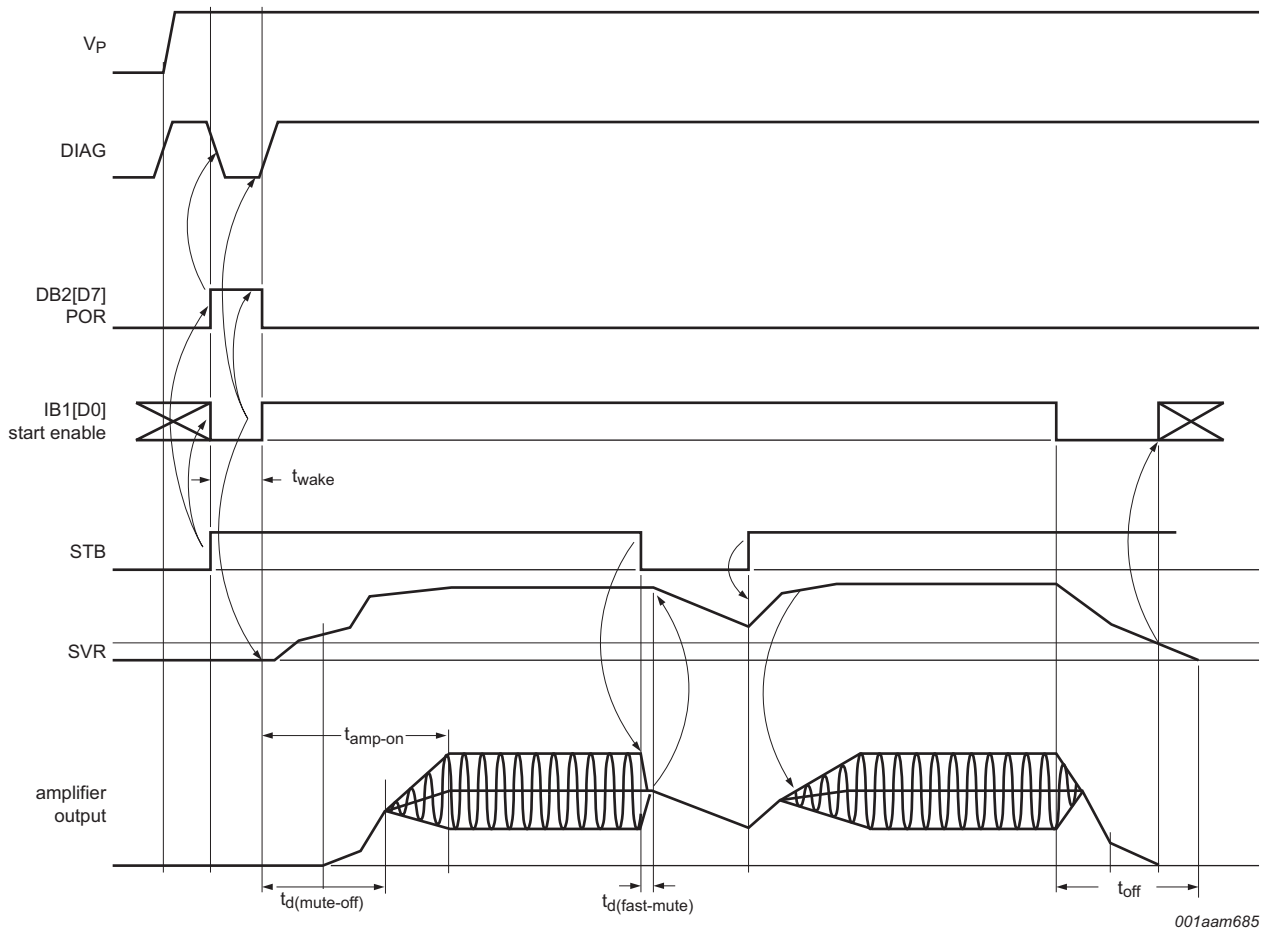


Fig 3. Start-up and shut-down in I²C-bus mode

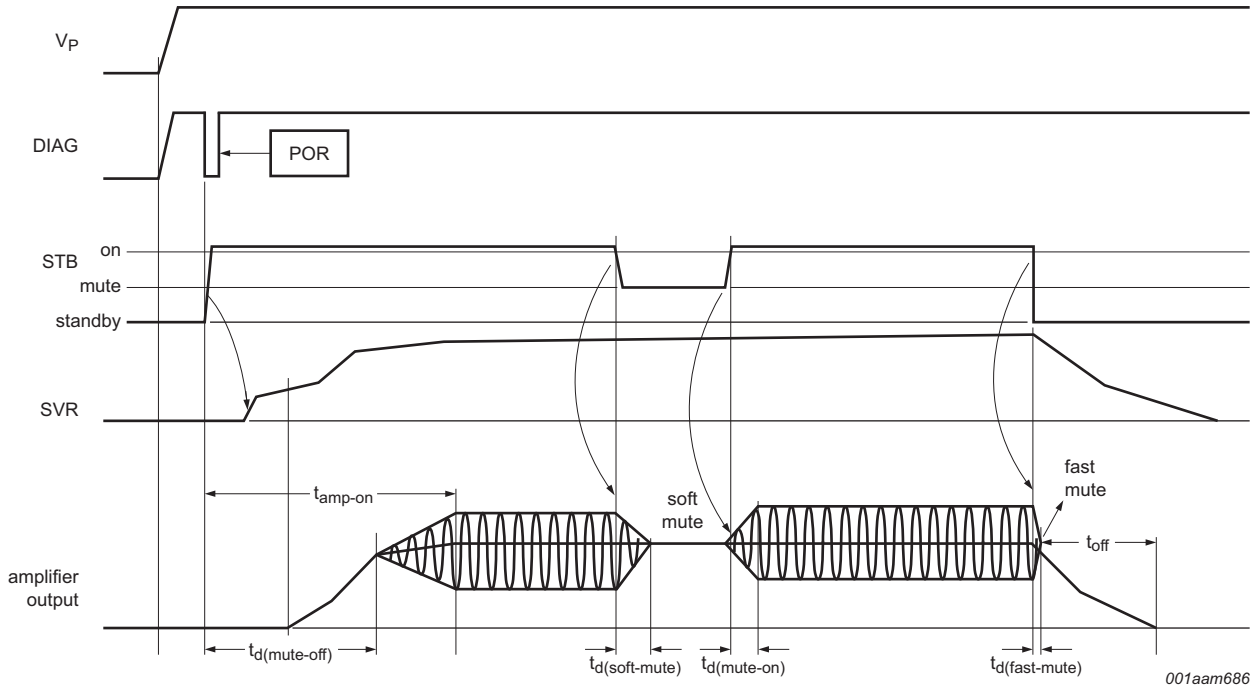


Fig 4. Start-up and shut-down in legacy mode

7.2 Engine start and low voltage operation

The voltage on pin SVR acts as a reference voltage for the input bias (set to 0.23 × battery voltage + 2 × diode voltage V_{be}) and as a reference for generating the filtered half supply voltage at the amplifier output. The capacitor connected to pin SVR improves supply voltage ripple rejection and channel separation between the four channels.

The DC output voltage relates to the SVR voltage to prevent common mode ripple on the speaker lines. If the supply voltage drops during an engine start, the output follows slowly due to the SVR capacitor. To enable sufficient headroom for the output signal below a battery voltage of 10 V, the DC-output voltage directly follows the half supply voltage. This ensures that at low supply voltage the undistorted output power is maximized. If the battery voltage is above 10 V, the DC-output voltage relates to the SVR voltage and is filtered again for supply ripple; see Figure 5.

Best efficiency mode is switched off when the battery voltage is below 10 V to ensure a distortion-free signal. The DC input voltage follows the supply voltage slowly, due to the SVR capacitor, to prevent audible plops, even during engine start.

If the battery voltage drops below 6 V, the low V_P mute is activated. During low V_P mute, the amplifier is fast muted (about 400 µs). When mute is completed, the capacitors on pin ACGND and pin SVR are discharged to prevent audible plops.

If the battery rises again above the low V_P mute threshold (6 V), and a Power-On Reset (POR) (DB2[D7] = 1) is not detected, the amplifier starts automatically. The amplifier restart only occurs if the SVR capacitor has been discharged to 0.7 V to prevent a start-up plop. If the battery voltage has dropped too much that the internal registers lose their

information, a POR occurs and the amplifier will not restart automatically. In I²C-bus mode, pin DIAG is pulled LOW to indicate a POR has occurred. In legacy mode, the amplifier restarts if pin STB remains HIGH.

The device prevents amplifier plops during engine start. To prevent plops on the amplifier output caused by, for instance, a tuner regulator out of regulation, the voltage on pin STB can be made zero when an engine start is detected. Pin STB activates the fast mute, suppressing disturbances at the amplifier inputs.

The built-in low battery voltage mute is the default, and in legacy mode is set to 5.5 V, but can also be set to 7.2 V via the I²C-bus. If the low battery voltage mute is set to 7.2 V, the amplifier activates fast mute (400 μs) and enters the same cycle when the low V_P mute was set to 5.5 V: discharge of the ACGND and SVR capacitors when the mute is completed and start-up when the supply voltage is above 8 V, when no POR has occurred.

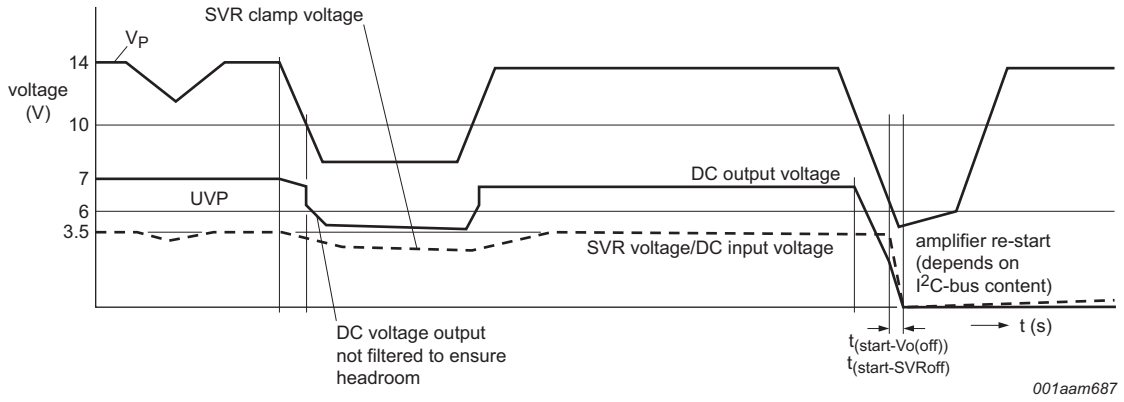
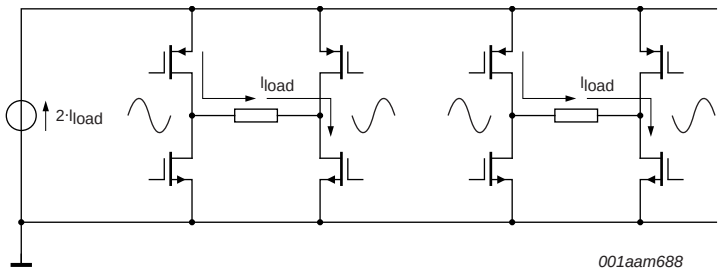


Fig 5. Engine start protection

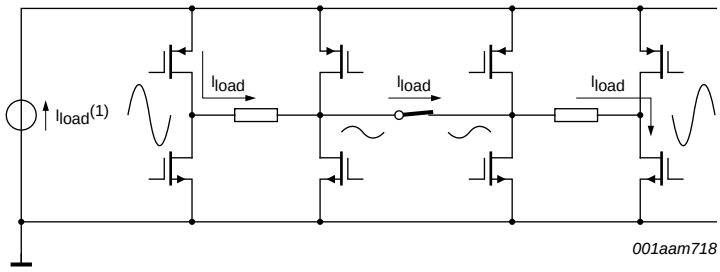
7.3 Best efficiency mode

7.3.1 2- and 4-channel best efficiency principle

Best efficiency mode is intended for signals of amplitude less than half the supply voltage. It re-uses the current between two channels by adding a switch (see best efficiency mode in Figure 6). If the two channels in Figure 6 have the same signal, the current from the supply is, in normal BTL mode, twice the I_L current, and in best efficiency mode, only I_L. At the same output power, best efficiency mode needs less power from the supply, resulting in less power dissipation in best efficiency mode.



a. Normal BTL mode

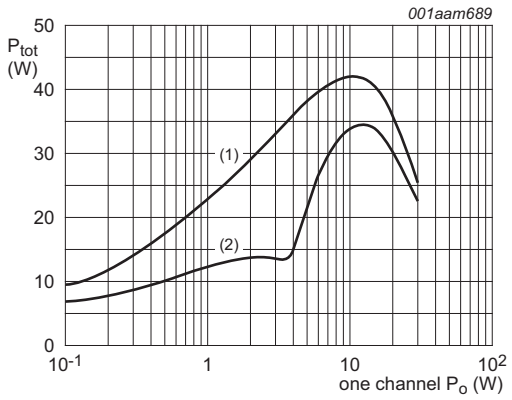


b. Best efficiency mode

(1) Same output power with less supply current.

Fig 6. Best efficiency principle

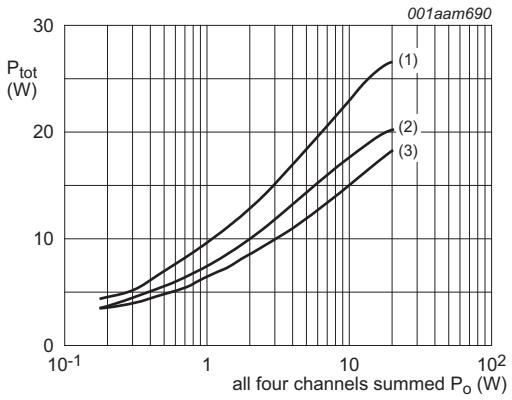
If the two channels have exactly the same signal, the current sharing between the channels is maximum and the dissipation minimum. This can be obtained in the car by using the front and rear channels for current sharing. In more advanced audio systems, the correlation between the front and rear channels is not 100 % because additional signal processing is used. Dissipation in best efficiency mode is more than when an identical signal is used; see Figure 7. By using the patented 4-channel best efficiency mode, where the information of all four channels is used instead of only the front or rear information, the dissipation is reduced for uncorrelated signals.



a. Same signal front and rear

(1) BTL mode.

(2) Best efficiency mode: 2-channel and 4-channel.



b. Uncorrelated signal front and rear

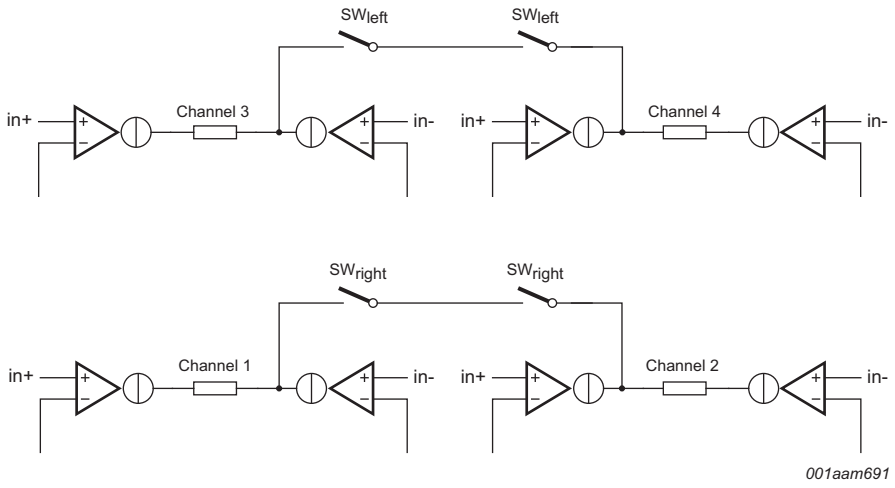
(1) BTL mode.

(2) Best efficiency mode: 2-channel.

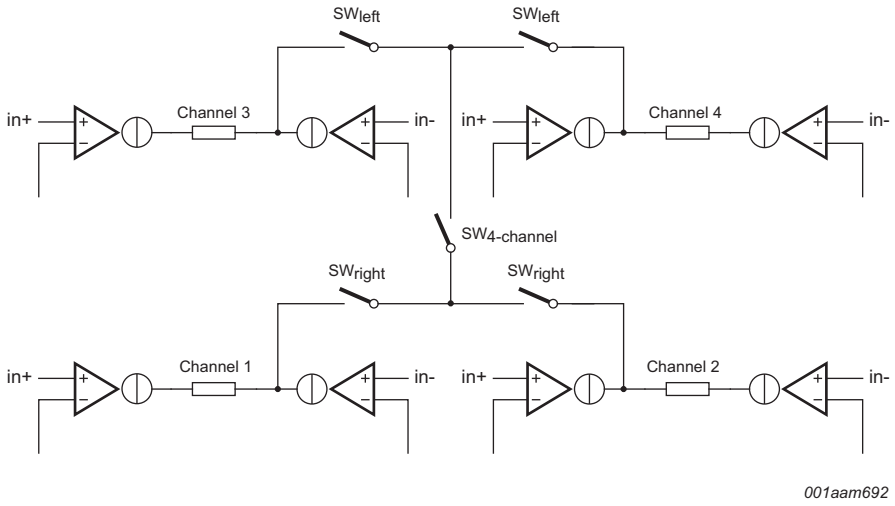
(3) Best efficiency mode: 4-channel.

Fig 7. Power dissipation of hypothetical quad amplifier with correlated and uncorrelated signals

Dissipation can be reduced by up to 65 % compared to standard BTL under normal listening conditions; see Figure 7a. With uncorrelated front and rear signals, the reduction in dissipation in 4 channel best efficiency mode is 8 W (35 %) compared to BTL, and 3 W (17 %) compared to 2 × 2 channel best efficiency; see Figure 7b.



a. 2 × 2 channel best efficiency mode

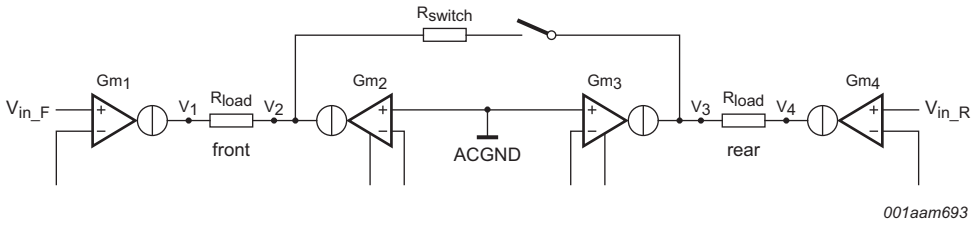


b. 4-channel best efficiency mode

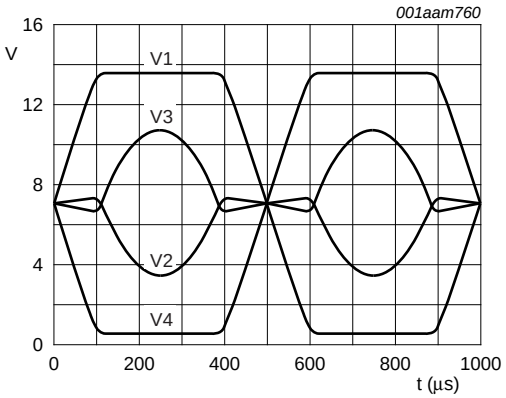
Fig 8. 2 × 2 channel and 4 channel best efficiency mode

7.3.2 Switching distortion

At output voltages lower than V_P / 2, the switch in Figure 9a is closed and V2 is almost constant at ACGND level, and current in both channels is shared (best efficiency mode active). If the output voltage increases above half the supply voltage, the switch needs to open and voltage V2 needs to decrease to eliminate distortion from the front loud speaker R_L. This opening and closing of the switch can cause additional distortion. By using a patented switch construction, no amplifier part is switched on and off and hot switching (switching within the signal current) is not required. This results in low THD values at high output powers in best efficiency mode; see Figure 10.

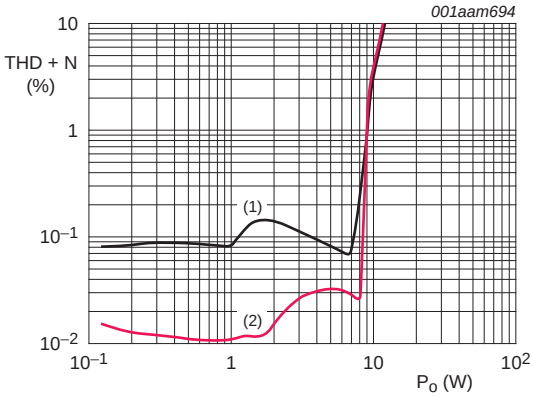


a. Voltage waveform locations



b. Voltage waveforms

Fig 9. Low switching distortion in best efficiency mode



(1) 10 kHz.

(2) 1 kHz.

Fig 10. Total harmonic distortion plus noise as a function of output power

7.3.3 Start-up and shut-down engine start and best efficiency control

- start-up and shut-down of the amplifier is in BTL mode, even when best efficiency mode is selected
- best efficiency mode can be enabled or disabled via I²C-bus commands

- best efficiency mode can be selected in either 2 × 2 channel- or 4 channel-mode via I²C-bus commands
- If 4 Ω or 2 Ω loads are used, they can be selected via the I²C-bus. When 2 Ω loads are selected, the output voltage when the best efficiency switch is opened is lower than when 4 Ω is selected, to avoid switching distortion. This gives a slightly higher efficiency with 4 Ω loads
- If the supply voltage drops below 10 V, for example during an engine start, the best efficiency mode is switched off
- In legacy mode the amplifier is set to 4-channel best efficiency mode with the best efficiency switch levels set to 2 Ω

7.4 Power-on reset and supply voltage spikes

If in I²C-bus mode the supply voltage drops below 4.5 V, the content of the I²C-bus latches cannot be guaranteed and POR is activated at a typical V_P level of 3.1 V. All latches are reset, the amplifier is switched off and pin DIAG is pulled LOW to indicate that a POR has occurred; see DB2[D7]. If IB1[D0] is set, the power-on flag is reset, pin DIAG is released and the amplifier starts. In legacy mode a supply voltage drop below 6 V switches off the amplifier. When the supply voltage is above 6 V the amplifier restarts if pin STB is still enabled.

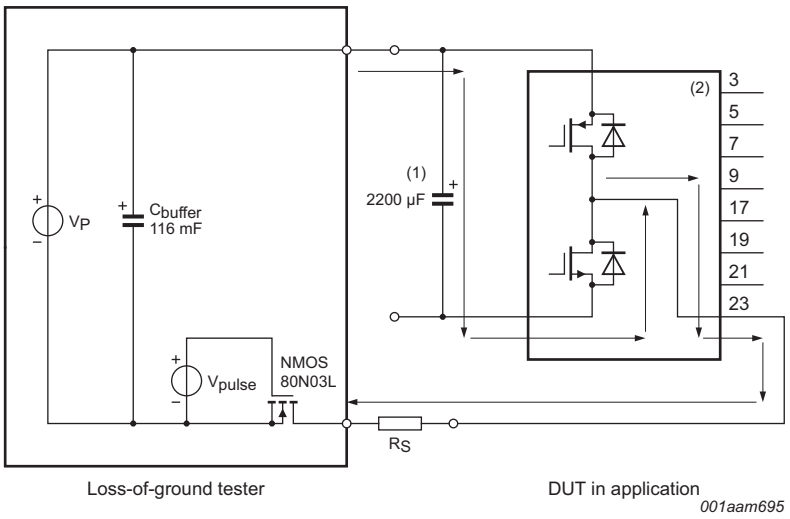
7.5 Protection

7.5.1 Output protection and short-circuit protection

If a short-circuit to ground, to V_P or across the load occurs on one or more amplifier outputs, only the channel with the short will be switched off. The channel that has a short-circuit and the type of short-circuit can be read via the I²C-bus. If pin DIAG is enabled for load fault information (IB2[D4] = 0) pin DIAG is pulled LOW. The window protection prevents a restart of the channel with a short to ground or V_P. With a short across the load the channel is switched on again after 15 ms to check if the short across the load is still present. If the short-circuit conditions are still present, the channel is switched off. If several channels have a short across the load at the same time, the channels are switched on one by one to prevent high supply current switching with four shorts across the load at the same time. The 15 ms cycle reduces power dissipation. To prevent audible distortion, the channel with the short can be disabled via the I²C-bus.

7.5.2 Loss-of-ground/loss of V_P

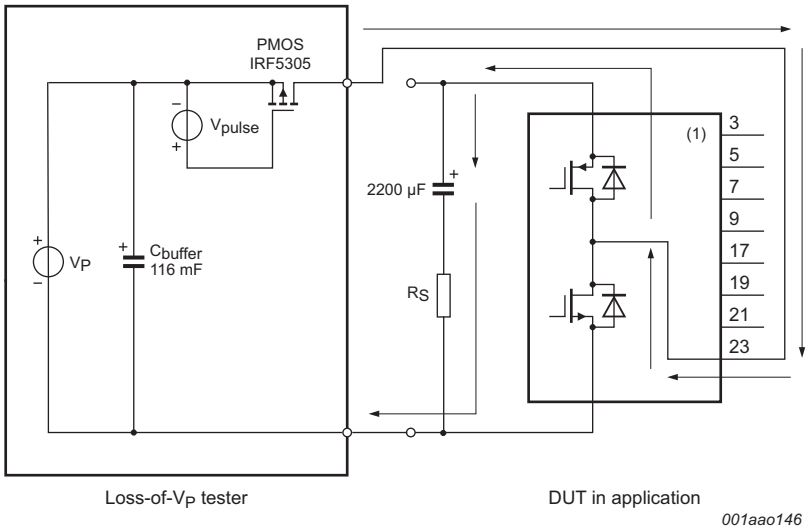
Loss-of-ground/loss of V_P is a double fault condition: the ground (or V_P) wire of the set is not connected and the ground (or V_P) wire is connected to one of the loudspeaker outputs. In this situation the supply capacitor in the set is charged through the body diodes of the output power transistors. This body diode (between the drain and source of the power transistor) is always present in amplifiers with MOS output stages. The capacitor charge current depends on the series impedance of the supply lines, the output impedance of the loss-of-ground tester and the value of the capacitor; see Figure 11. To simulate a worst-case condition, the loss-of-ground tester is equipped with a buffer capacitor of 116 mF to simulate a very low output impedance. With an R_S of 63 mΩ, peak currents of more than 70 A have been measured.



(1) Capacitor can be 2200 µF to 10000 µF.

(2) Amplifier output stage.

Fig 11. Test circuit for loss-of-ground test



(1) Amplifier output stage.

Fig 12. Test circuit for loss-of-V_P test

7.5.3 Speaker fault detection

A speaker fault protection has been built in to prevent damage to the speaker when one side of the speaker is connected to ground: during amplifier start-up, just before the start-up mute release (V_{SVR} = 4.6 V), there is a missing-current check. If the missing current is 1 A, a speaker fault is assumed. Therefore, when a load resistor of 4 Ω is connected to ground, the amplifier channel will not switch off but indicates a speaker fault.

7.5.4 Overvoltage warning and load dump protection

If the battery voltage V_P exceeds the maximum value of $V_{th(ovp)}$, the device switches off the output stages of the amplifier to protect the output transistors. The overvoltage pre-warning bit is set when the supply voltage level exceeds the value of $V_{P(ovp)pwarn}$.

The functionality of the diagnostic output can be chosen in I²C-bus mode. In this mode the pre-warning information can become visible at the diagnostic output. In legacy mode, pin DIAG will not be activated under pre-warning conditions.

Although the amplifier switches off the output stages, the device remains operational during load dump conditions (maximum value of V_P at load dump protection; duration 50 ms, rise time > 2.5 ms). The occurrence of the load dump situation can last for a longer period of time without damaging the device. Provided that the I²C-bus supply is within the levels specified, communication with the I²C-bus bus during load dump situations remains possible and the status of the channel outputs can be read.

7.5.5 Thermal pre-warning and thermal protection

If the average junction temperature reaches one of the adjustable levels set via the I²C-bus, selected with IB3[D4], pre-warning is activated resulting in pin DIAG LOW (if selected) and can be read via the I²C-bus. The default setting for the thermal pre-warning is IB3[D4] = 0 setting the warning level at $T_{j(AV)(pwarn)}$ = 160 °C. In legacy mode the thermal pre-warning is also set at $T_{j(AV)(pwarn)}$ = 160 °C.

If the temperature increases further, the temperature-controlled gain reduction is activated for all four channels to reduce the output power; see Figure 13. If this does not reduce the average junction temperature, all four channels are switched off at the absolute maximum temperature T_{off}.

If the temperature controlled gain is activated, mute is activated and best efficiency mode is deactivated.

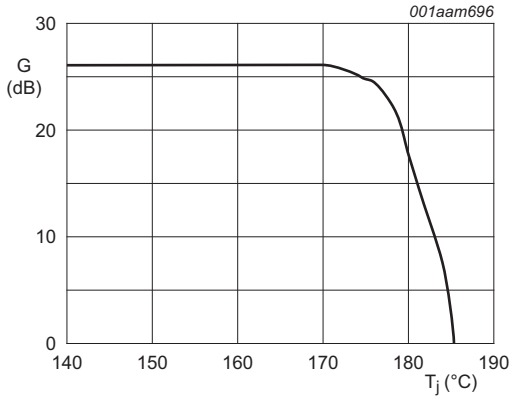


Fig 13. Temperature controlled amplifier gain

7.6 Diagnostics

Diagnostic information can be read via the I²C-bus, but can also be made available at pin DIAG or pin STB. Pin DIAG indicates information such as POR occurred, low battery, and high battery; the output load fault information is selectable via the I²C-bus. This

information is seen at pin DIAG as a logical OR. In case of a failure, pin DIAG remains LOW and the microcontroller can read the failure information via the I²C-bus; pin DIAG can be used as a microcontroller interrupt to minimize I²C-bus traffic. When the failure is removed, pin DIAG is released.

To enable full control over the clipping information, pin STB can be programmed as a second-clip detection pin. The clip detection level can be selected for all channels at once. The clip information can be selected to be available separately at pin DIAG or at pin STB for each channel. It is possible, for example, to distinguish between clipping of the front and the rear channels.

The diagnostic information available at either of the two diagnostic pins DIAG and STB is shown in Table 4.

Table 4. Diagnostic information on pins DIAG and STB

Diagnostic information	I²C-bus mode		Legacy mode
	DIAG pin	STB pin	DIAG pin
Power-On Reset (POR)	after POR, pin DIAG remains LOW until amplifier starts (inverse of start-up bit)	no	no
Low battery	yes	no	yes
Clip detection	can be enabled per channel; can be enabled by IB1[D7] if below V_P = 10 V; default is 'blocked'	can be enabled per channel; can be enabled by IB1[D7] if below V_P = 10 V; default is 'blocked'	yes; fixed level for all channels at 2 %; blocked for V_P < 10 V
Temperature pre-warning	can be enabled; default: $T_{j(AV)(pwarn)}$ = 160 °C	no	yes, pre-warning level is $T_{j(AV)(pwarn)}$ = 160 °C
Short	can be enabled; default is enabled	no	yes
Speaker fault detection	no	no	no
Offset detection	no	no	no
Load detection	no	no	no
Overvoltage protection (20 V)	yes	no	yes
Overvoltage pre-warning (16 V)	can be enabled; default is disabled	no	no
Maximum temperature protection (active)	yes	no	yes
Start-up diagnostics indication	no	no	no

7.6.1 Start-up diagnostics with DC load detection

If the start-up diagnostics are enabled, the load condition of all four channels is determined. At the end of the start-up diagnostics cycle, not only the load condition is known (shorted load, normal load or open load), but also if a separate amplifier is connected or if the outputs are shorted to battery or ground. If a separate amplifier (booster) is detected, the amplifier can start-up in line driver mode (low gain setting).

The load diagnostic is insensitive to door-slam (slowly moving speaker due to slamming of the car door) and to external interference such as crosstalk of relays switching in the wiring harness; see Figure 14.

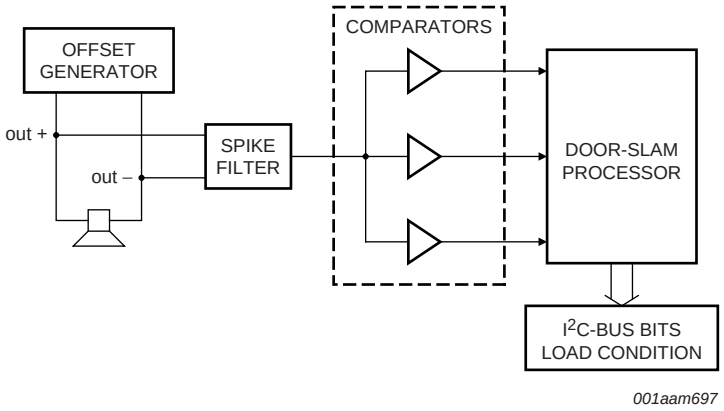


Fig 14. Principle of start-up diagnostics

The load detection values are shown in Figure 15.

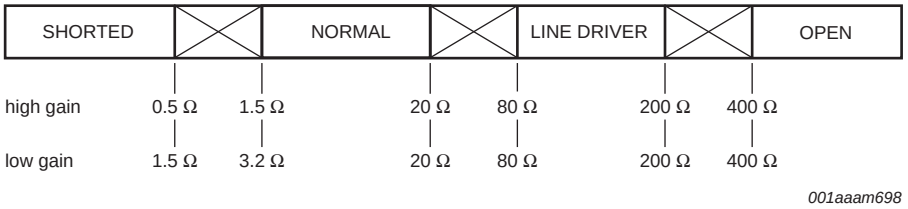
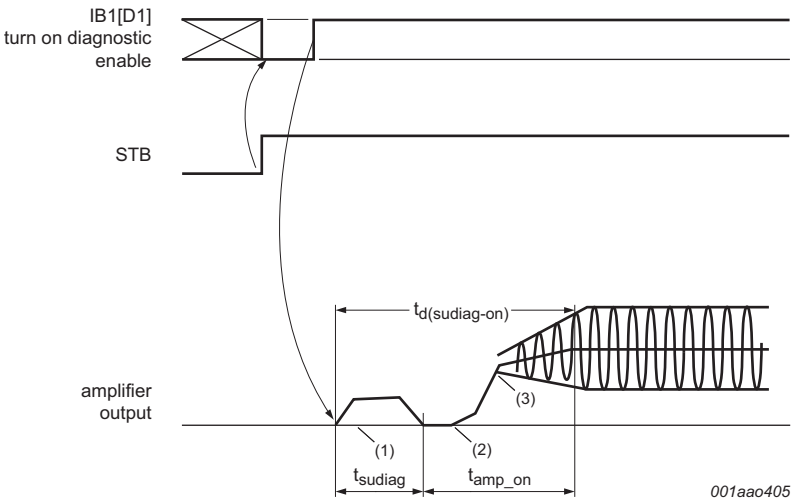


Fig 15. Start-up diagnostics load detection levels

If only 4 Ω speakers are connected, the low gain mode can be selected during the start-up diagnostics. A shorted load is indicated until an impedance of 1.5 Ω is reached. Even ‘soft’ shorts in the wiring harness will be detected.



(1) First stage: open load/load/line driver load; short across the load.

(2) Second stage: amplifier start plus short to ground/V_P; speaker fault.

(3) Latch of speaker fault.

Fig 16. Start-up with start-up diagnostics

In the first stage an offset is generated across the load. To avoid switch-on plop-noise the offset is increased after 15 ms. The measurement cycle lasts t_{sudiag}. After 15 ms the offset across the load is reduced. The offset is generated with resistors instead of the amplifier to avoid plop-noise during engine start. If the offset is removed quickly, audible plop can occur during periods without audio.

If the output voltage of the outputs is more than 3.5 V during the first stage, the start-up diagnostic is switched off to avoid damage to the amplifier. This can happen with a door slam or with a short to V_P. If a short is applied to V_P, that channel with the short will report invalid after the first stage. If only one or two channels report invalid after the first stage, a short to V_P in those channels can be assumed. If all four channels report invalid, under-over- voltage, a startup diagnostic cycle can be assumed.

The start-up diagnostics has a built-in spike filter to remove disturbances caused by switching relays in the wiring harness or EMC. The door-slam processor filters out disturbances caused when the car door closes: car door-slam can cause the speakers to move slowly which disturbs the measurement. With these filter techniques, reliable load detection is performed in a single start-up diagnostics cycle.

The start-up diagnostics can be repeated. Only the first stage, where the speaker load is determined, is sensitive to disturbance and needs to be repeated. When the start-up diagnostics start, the invalid bit is set, and “start-up diag busy bit” (TDF8546 bit DB5[D5]) indicates that the start-up diagnostics are not completed. When the start-up is completed, or interrupted by a POR, the “start-up diag busy bit” is reset.

Two situations are possible:

- the start-up diagnostics are enabled (IB1[D1] = 1) and the amplifier start is not enabled (IB1[D0] = 0), bit “start-up diag busy bit” is reset when the start-up diagnostics are completed, and the I²C-bus data bits are set. Toggling the start-up diagnostics bit re-starts the start-up diagnostic. The invalid bits are set and bit “start-up diag busy bit” indicates that the start-up diagnostics are not completed.
- the start-up diagnostics are enabled (IB1[D1] = 1) and the amplifier start is enabled (IB1[D0] = 1). After the first start-up diagnostic cycle has finished, the amplifier starts and when start-up is completed, just before the start-up mute release (DC output voltage is 1.4 V below midtap voltage), bit “start-up diag busy bit” indicates that the startup diagnostic is completed. It is not necessary to toggle the start-up diagnostics and has no purpose.

The first and second stages of the start-up diagnostics can be repeated:

Start-up with the start-up diagnostics (IB1[D1] = 1 and the amplifier start enabled (IB1[D0] = 1). Wait until DB5[D5] = 0 which indicates that the start-up diagnostics cycle is completed. Read the start-up diagnostics information. Shut down the amplifier by making the start-up bit logic 0. When DB5[D0] = 0, the amplifier is completely shut down and a new start-up cycle can be programmed.

Table 5. Start-up diagnostics I²C-bus bits

DC load bits[1]		Meaning
DBx[D5]	**DBx[D4]**	
0	0	normal load
0	1	line driver mode
1	0	open load
1	1	invalid: overvoltage or undervoltage (V_P < 10 V) has occurred, or start-up diagnostics not completed, or channel has short to V_P; indicated in second stage

[1] DBx[D3] indicates a shorted load; DBx[D1] indicates a short to V_P; DBx[D0] indicates a short to ground. When set, D4, D5 have no meaning.

If during the start-up diagnostics an engine start occurs, the generated offset to measure the DC load is reduced and the start-up diagnostics cannot be performed correctly. In this case the invalid combination DBx[D4:D5] = 11 is set.

The start-up diagnostics information in the I²C-bus bits is combined with the AC load detection allowing the start-up diagnostics information to be read when IB4[D4] = 0. If IB4[D4] = 1, the stored start-up diagnostics information bits cannot be read but they will not lose their value.

Remark: the shorted load, and short to V_P or ground information from the start-up diagnostics is cleared after an I²C-bus read. This indicates the real situation: when the short is removed, the bits are cleared. The DBx[D5] and DBx[D4] information, generated at start-up, is refreshed after a new start-up diagnostics cycle.

7.6.2 DC offset detection

The offset detection can be performed with no input signal (for instance when the DSP is muted after a start-up) or with an input signal. If in I²C-bus mode an I²C-bus read of the output offset is performed, the I²C-bus DBx[D2] latches are set. If the amplifier BTL output voltage is within a window with a threshold of 1.3 V (typical), the DBx[D2] latches are reset and their setting is disabled. If for example, after 1 s another I²C-bus read is performed and the offset bits are still set, the output did not cross the offset threshold during the last 1 second; see Figure 17. This can mean either a frequency below 1 Hz was applied (1 s I²C-bus read interval) or an output offset of more than 1.3 V is present.

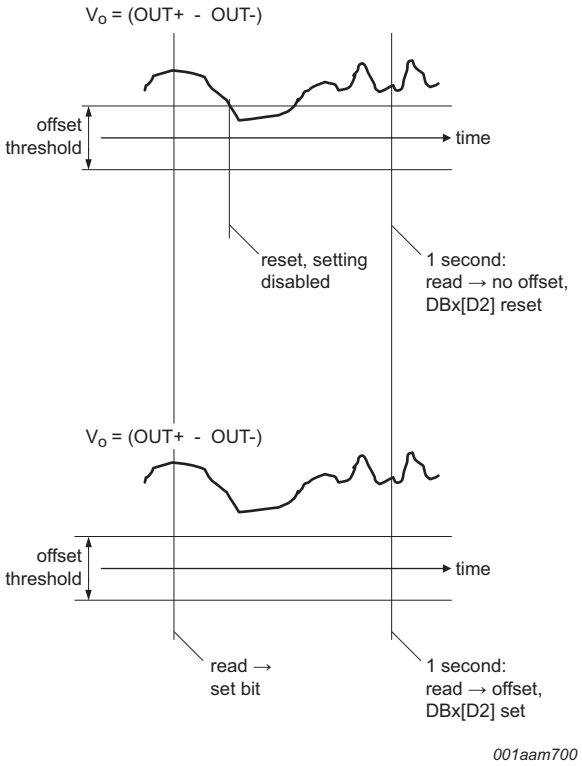


Fig 17. Offset detection

7.6.3 AC load detection

The AC load detection, set with IB1[D2] = 1, is used to detect if AC-coupled speakers such as tweeters are connected correctly. When performing the AC-load detection, the best efficiency mode must be disabled IB5[D7] = 0. The detection requires a 19 kHz sine wave to be applied to the inputs of the amplifier. A high current AC-load detection mode can be selected, for example during car assembly, or a low current AC-load detection mode, for example during switch on of car radio. The output voltage over the load impedance generates an amplifier current. If the amplifier peak current triggers 4 times a 500 mA (peak) threshold (or 275 mA (peak) in low current mode), the AC-load detection bit is set. The 4 'threshold cross' counter is used to prevent false AC-load detection caused by switching the input signal on or off.

An AC-coupled speaker reduces the impedance at the output of the amplifier in a certain frequency band. The presence of an AC-coupled speaker can be determined using a high current mode (IB4[D1] = 1, see Figure 18) or using a low current detection mode (IB4[D1] = 0; see Figure 18).

If, for instance, a 19 kHz input signal is generated with a peak output voltage of 2 V the I²C-bus bits are guaranteed to be set with a total AC + DC load less than 4 Ω and are guaranteed not set with a load of more than 9 Ω; see Figure 18.

The interpretation of the line driver and amplifier mode DC load bit for AC load detection is shown in Table 6.

Table 6. AC load detection

IB4[D4] = 1	DB1 to 4 [D4] (AC load bit)
No AC load detected	0
AC load detected	1

If IB1[D2] = 1 the AC-load detection measurement cycle is enabled, the peak counter is reset and the measuring cycle starts. The AC-load detection is only performed after the amplifier has completed its start-up cycle and when the best efficiency mode is disabled IB5[D7] = 0. Since the AC-load information in the I²C-bus bits is combined with the start-up diagnostics, the AC-load information can be read when IB4[D4] = 1. If IB4[D4] = 0, the stored AC-load bits cannot be read, but their values are preserved.

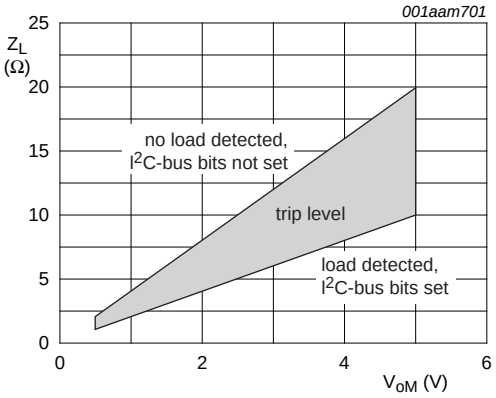


Fig 18. AC-load impedance as a function of peak output voltage (high current AC-load detection)

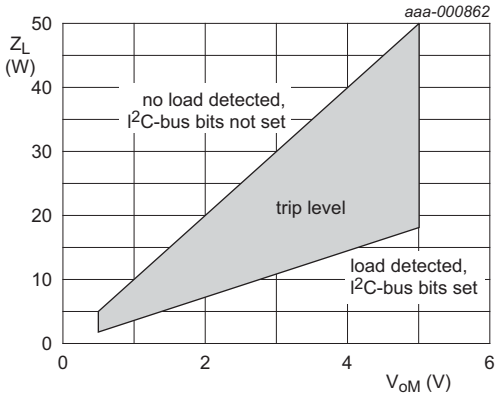


Fig 19. AC-load impedance as a function of peak output voltage (low current AC-load detection)

7.6.4 Distortion clip detection

If the amplifier output starts clipping at the supply voltage or ground, the output signal becomes distorted. If the distortion per channel exceeds a selectable threshold (2 %, 5 % or 10 %), either pin DIAG or pin STB is activated. To be able to detect if, for instance, the front channels (channels 1 and 3) or rear channels (channels 2 and 4) are clipping, the clip information per channel can be directed to either pin DIAG or pin STB.

It is possible to only have the clip information on the diagnostic pins by disabling the temperature- and load information on pin DIAG. The temperature and load protection are still functional but can only be read via the I²C-bus.

The clip detection level can be programmed via the I²C-bus. The clip information is blocked below a supply voltage of 10 V to avoid false clip detection during engine start, or can be programmed to operate at the low voltage detection level of 7.5 V or 6 V.

Since it is possible to have different amplifier gain settings between the front and rear channels and there is only one clip reference current, the clip detect levels are only accurate for the channels with the highest gain. In line driver mode the DC-output voltage is $0.23V_P$ and clip detection will still indicate a clip, but the levels will not be accurate.

7.7 Line driver mode and low gain mode

The TDF8546 can be used as a line driver or as a low gain amplifier. In both situations, the gain needs to be set to 16 dB via the I²C-bus (IB3[D5:D6] and can be independently set for the front (channels 1 and 3) and rear (channels 2 and 4). The main difference between line driver mode and low gain mode is the DC output voltage.

In line driver mode the TDF8546 is used to drive a separate amplifier or booster. In this mode the DC output voltage is set to 0.23 × battery voltage and is filtered with the capacitor connected to pin SVR (same as V_{SVR}). The reason not to set the DC output voltage to half the battery voltage is to allow engine starts at a battery voltage as low as 6 V. The DC output voltage remains approximately 3 V during engine start. If the DC output voltage is set to half the battery voltage, with an engine start the common mode voltage will change quickly from 7 V to 3 V. This drives the input stage of the booster below the ground level.

If the TDF8546 is used as a low gain amplifier in a booster, the DC output voltage is set to half of the supply voltage to ensure maximum undistorted output power.

The line driver and low gain modes can be selected with I²C-bus bit IB4[D2].

Table 7. DC output voltage as a function of different gain settings

Channels 1 and 3 gain setting (dB)	Channels 2 and 4 gain setting (dB)	Line driver/low gain mode IB4[D2][1]	All channels DC output voltage (V)
26	26	X	$0.5V_P$
16	26	X	$0.5V_P$
26	16	X	$0.5V_P$
16	16	low gain mode	$0.5V_P$
16	16	line driver mode	$0.23V_P$

[1] X = neither mode selected.

7.8 I²C-bus, legacy mode and address select pin

Pin ADSEL can select either of two amplifier modes: legacy mode or I²C-bus mode.

7.8.1 Address select (pin ADSEL)

The following amplifier functions are selected with pin ADSEL:

- Pin ADSEL shorted: (R_{ADSEL} < 470 Ω) legacy mode, no I²C-bus communication is needed
- Resistor connected between pin ADSEL and ground: where different I²C-bus addresses can be selected with resistors
- One I²C-bus address can be selected by either forcing a voltage on pin ADSEL or by connecting a high ohmic resistor between pin ADSEL and V_P.

To avoid address changes during low supply voltage, the address selected by the value of resistor connected to pin ADSEL is latched at voltages below 6 V. The consequence is, during start-up and after every power-on reset, the supply voltage must be above 6 V otherwise the address is invalid.

7.8.2 Legacy mode (R_{ADSEL} < 470 Ω)

The function of pin STB changes from off/operating to off/mute/operating and the amplifier starts immediately when pin STB is put into mute or operating mode. Mute operating is controlled via an internal timer (15 ms) to minimise mute-on plops. When pin STB is switched directly from operating to off, first the hard mute is activated (switching to mute within 400 μs) and then the amplifier shuts down. To have a plop-free shut-down, first pin STB should be switched to mute for 50 ms and then switched off.

7.8.3 I²C-bus mode

If pin STB is LOW, the total quiescent current is low, and the I²C-bus lines are not loaded. When pin STB is switched HIGH, the TDF8546 enters operating mode and performs a POR which makes pin DIAG LOW. The TDF8546 starts when IB1[D0] = 1. Bit D0 also resets the ‘power on reset occurred’ bit (DB2[D7]) and releases pin DIAG.

Soft mute and hard mute can be activated via the I²C-bus. Soft mute can be activated independently for the front (channels 1 and 3) and rear (channels 2 and 4), and mutes the audio in 15 ms. Hard mute activates the mute for all channels at the same time and mutes the audio in 400 μs. Unmuting after a hard mute will be a soft unmute of approximately 15 ms. When pin STB is switched to Off mode, and the amplifier has started, first the hard mute is activated and then the amplifier shuts down. It is possible to fully mute the amplifiers within 400 μs by making pin STB LOW, for example during an engine start.

7.8.4 I²C-bus diagnostic bits read-out/cleared after read

The amplifier's diagnostic information can be read via the I²C-bus. The I²C-bus bits are set if a failure occurs and are reset by the I²C-bus read command (cleared after read). When the failure is removed, the microcontroller knows the cause of the failure by reading the I²C-bus. The consequence of this procedure is that old information is read during the I²C-bus read. Most real information will be gathered within two consecutive read commands.

Cleared after read means that the I²C-bus bits are cleared after a read command. The Clear command is done only if all five data bytes are read. If only four data bytes are read, the I²C-bus latches are not cleared and the old value remains in the latches.

When selected, pin DIAG gives actual diagnostic information. If a failure is removed, pin DIAG is released instantly, independently of the I²C-bus latches.

7.9 Amplifier in combination with a DC-to-DC converter

The TDF8546 can be used in combination with a DC-DC up-converter as the supply for the amplifier (connected to V_P). If the DC-DC converter output voltage is controlled with the audio signal, the amplifier's dissipation can be reduced at lower output powers. To ensure that the amplifier can follow supply voltage variations, the supply voltage ripple capacitor connected to pin SVR, to filter the amplifier's common mode output voltage, must be disconnected internally. The SVR capacitor is still used to determine the DC input voltage. If I²C-bus bit IB4[D7] = 1, the common mode output voltage directly follows the supply voltage variations.

8. I²C-bus specification

Table 8. TDF8546 hardware address select

Pin ADSEL	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$	Hex	Remark
Open	1	1	0	1	1	0	0	0 = write to TDF8546; 1 = read from TDF8546	D8	reserved; instruction and data bytes have other meaning
100 kΩ ± 1 %						1	0		DC	-
30 kΩ ± 1 %						1	1		DE	-
10 kΩ ± 1 %					0	1	0		D4	-
Voltage > 4 V					1	0	1		DA	-
GND	no I²C-bus; legacy mode									-

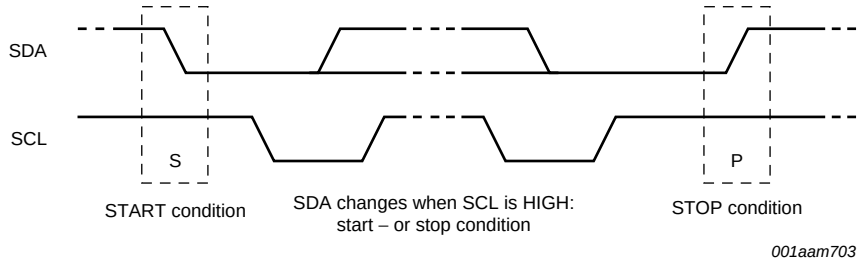


Fig 20. Definition of START and STOP conditions

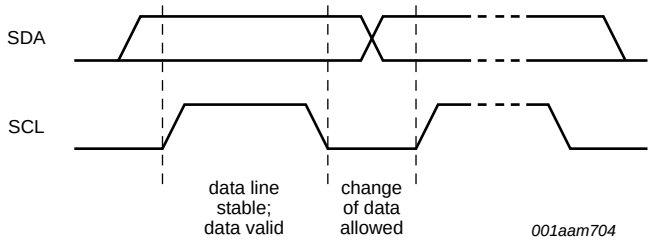


Fig 21. Bit transfer

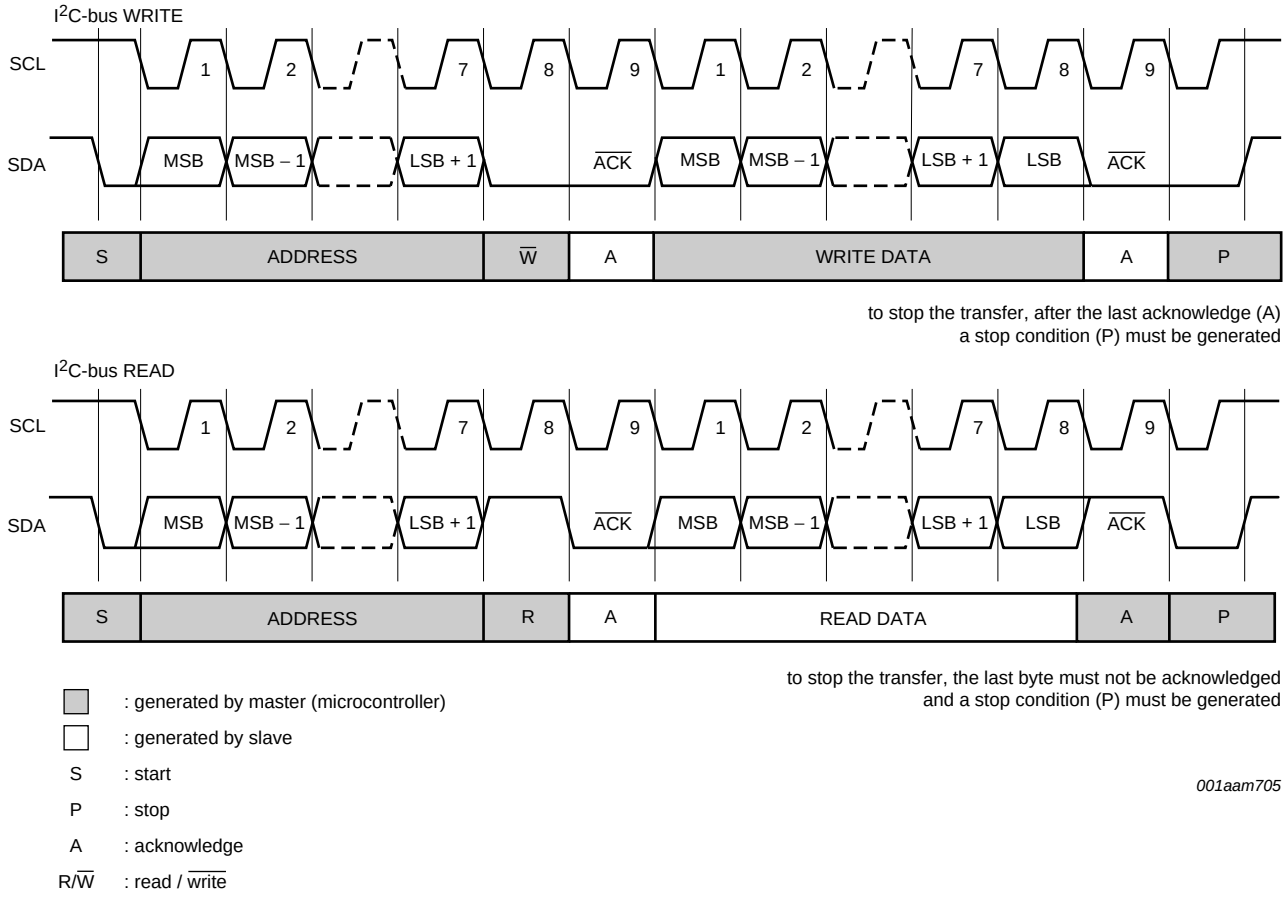


Fig 22. I²C-bus read and write modes

8.1 I²C-bus instruction bytes

I²C-bus mode:

- If R/$\overline{W}$ bit = 0, the TDF8546 expects five instruction bytes; IB1, IB2, IB3, IB4, IB5
- After a power-on reset, all instruction bits are set to zero

Legacy mode:

- All bits equal to zero define the setting, with the exception of bit IB1[D0] (see Table 9) which is ignored and IB5[D7] = 1; see Table 13.

Table 9. Instruction byte IB1

Bit	Description
D7	enable or disable clip detection below V_P = 10 V
	0 = disable clip detection below V_P = 10 V
	1 = enable clip detection below V_P = 10 V
D6	channel 3 clip information on pin DIAG or pin STB
	0 = clip information on pin DIAG
	1 = clip information on pin STB

Table 9. Instruction byte IB1 *…continued*

Bit	Description
D5	channel 1 clip information on pin DIAG or pin STB
	0 = clip information on pin DIAG
	1 = clip information on pin STB
D4	channel 4 clip information on pin DIAG or pin STB
	0 = clip information on pin DIAG
	1 = clip information on pin STB
D3	channel 2 clip information on pin DIAG or pin STB
	0 = clip information on pin DIAG
	1 = clip information on pin STB
D2	enable or disable AC load detection
	0 = AC load detection disabled
	1 = AC load detection enabled
D1	enable or disable start-up diagnostics
	0 = start-up diagnostics disabled
	1 = start-up diagnostics enabled
D0	enable or disable amplifier start
	0 = amplifier start not enabled
	1 = amplifier will start up

Table 10. Instruction byte IB2

Bit	Description
D7 and D6	clip detection level
	00 = clip detection level 2 %
	01 = clip detection level 5 %
	10 = clip detection level 10 %
	11 = clip detection level disabled
D5	temperature information on pin DIAG
	0 = temperature information on pin DIAG
	1 = no temperature information on pin DIAG
D4	load fault information (shorts) on pin DIAG
	0 = fault information on pin DIAG
	1 = no fault information on pin DIAG
D3	-
D2	soft mute channel 1 and channel 3 (mute delay 15 ms)
	0 = no soft mute
	1 = soft mute
D1	soft mute channel 2 and channel 4 (mute delay 15 ms)
	0 = no soft mute
	1 = soft mute

Table 10. Instruction byte IB2 *…continued*

Bit	Description
D0	fast mute all amplifier channels
	0 = no fast mute
	1 = fast mute

Table 11. Instruction byte IB3

Bit	Description
D7	-
D6	amplifier channel 1 and channel 3 gain select
	0 = 26 dB
	1 = 16 dB
D5	amplifier channel 2 and channel 4 gain select
	0 = 26 dB
	1 = 16 dB
D4	temperature pre-warning level
	0 = warning level at $T_{j(AV)(pwarn)}$ = 160 °C
	1 = warning level at $T_{j(AV)(pwarn)}$ = 135 °C
D3	enable or disable channel 3
	0 = channel 3 enabled
	1 = channel 3 disabled
D2	enable or disable channel 1
	0 = channel 1 enabled
	1 = channel 1 disabled
D1	enable or disable channel 4
	0 = channel 4 enabled
	1 = channel 4 disabled
D0	enable or disable channel 2
	0 = channel 2 enabled
	1 = channel 2 disabled

Table 12. Instruction byte IB4

Bit	Description
D7	use of SVR capacitor
	0 = filter common-mode voltage
	1 = SVR capacitor used in combination with a DC-to-DC converter (common-mode voltage not filtered)
D6	soft or fast mute select during shut-down via pin STB
	0 = activate fast mute during shut-down
	1 = activate slow mute during shut-down
D5	16 V overvoltage warning on pin DIAG
	0 = 16 V overvoltage warning not on pin DIAG
	1 = 16 V overvoltage warning on pin DIAG
D4	AC or DC load information on bits DBx[D5:D4]
	0 = DC load information on bits DBx[D5:D4]
	1 = AC load information on bits DBx[D5:D4]
D3	-
D2	line driver mode or low gain mode selection
	0 = line driver mode; common-mode output voltage is $0.23V_P$
	1 = low gain mode; common-mode output voltage is $0.5V_P$; only valid for channels when gain is set to 16 dB
D1	AC load detection measurement current selection
	0 = AC load detection; low measurement current
	1 = AC load detection; high measurement current
D0	low V_P mute undervoltage level setting
	0 = low V_P mute undervoltage level set to 5.5 V
	1 = low V_P mute undervoltage level set to 7.2 V

Table 13. Instruction byte IB5

Bit	Description
D7	best efficiency mode
	0 = best efficiency mode disabled
	1 = best efficiency mode enabled
D6	best efficiency mode channels
	0 = best efficiency mode in all 4 channels
	1 = best efficiency mode in 2 × 2 channels
D5	-
D4	best efficiency switch level load impedance setting
	0 = best efficiency switch level set to 2 Ω load
	1 = best efficiency switch level set to 4 Ω load
D3	-
D2	-
D1	-
D0	-

8.2 I²C-bus data bytes

I²C-bus mode:

- If R/$\overline{W}$ = 1, the TDA8546 sends five data bytes to the microprocessor: DB1, DB2, DB3, DB4 and DB5
- All bits are latched
- All bits are reset after a read operation except [D4] and [D5] in DB1 to DB4. Bit [D2] in DB1 to DB4 is set after a read operation; see Section 7.6.1 and Section 7.6.2
- For explanation of AC and DC load detection bits, see Section 7.6.3

Table 14. Data byte DB1

Bit	Description
D7	temperature pre-warning
	0 = no temperature pre-warning
	1 = temperature pre-warning has occurred
D6	speaker fault channel 2
	0 = no speaker fault, channel 2
	1 = speaker fault, channel 2
D5 and D4	channel 2 DC-load or AC-load detection
	if bit IB4[D4] = 1, AC-load detection is enabled, bit D5 does not care, bit D4 has the following meaning:
	0 = no AC-load
	1 = AC-load detected
	if bit IB4[D4] = 0, AC-load detection is disabled, bits D5 and D4 are available for DC-load detection
	00 = normal load
	01 = line driver load
	10 = open load
	11 = not valid
D3	channel 2 shorted load
	0 = no shorted load
	1 = shorted load
D2	channel 2 output offset
	0 = no output offset
	1 = output offset
D1	channel 2 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 2 short to ground
	0 = no short to ground
	1 = short to ground

Remark: Data bits are only reset (cleared after read) after reading 5 data bytes.

Table 15. Data byte DB2

Bit	Description
D7	POR and amplifier status
	0 = no POR; amplifier on
	1 = POR has occurred; amplifier off
D6	speaker fault channel 4
	0 = no speaker fault
	1 = speaker fault, channel 4
D5 and D4	channel 4 DC load or AC-load detection
	if bit IB4[D4] = 1, AC-load detection is enabled, bit D5 does not care, bit D4 has the following meaning:
	0 = no AC-load
	1 = AC-load detected
	if bit IB4[D4] = 0, AC-load detection is disabled, bits D5 and D4 are available for DC-load detection
	00 = normal load
	01 = line driver load
	10 = open load
	11 = not valid
D3	channel 4 shorted load
	0 = no shorted load
	1 = shorted load
D2	channel 4 output offset
	0 = no output offset
	1 = output offset
D1	channel 4 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 4 short to ground
	0 = no short to ground
	1 = short to ground

Remark: Data bits are only reset (cleared after read) after reading 5 data bytes.

Table 16. Data byte DB3

Bit	Description
D7	maximum temperature protection
	0 = no protection
	1 = maximum temperature protection
D6	speaker fault channel 1
	0 = no speaker fault, channel 1
	1 = speaker fault, channel 1
D5 and D4	channel 1 DC-load or AC-load detection
	if bit IB4[D4] = 1, AC-load detection is enabled, bit D5 does not care, bit D4 has the following meaning:
	0 = no AC-load
	1 = AC-load detected
	if bit IB4[D4] = 0, AC-load detection is disabled, bits D5 and D4 are available for DC-load detection:
	00 = normal load
	01 = line driver load
	10 = open load
	11 = not valid
D3	channel 1 shorted load
	0 = no shorted load
	1 = shorted load
D2	channel 1 output offset
	0 = no output offset
	1 = output offset
D1	channel 1 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 1 short to ground
	0 = no short to ground
	1 = short to ground

Remark: Data bits are only reset (cleared after read) after reading 5 data bytes.

Table 17. Data byte DB4

Bit	Description
D7	power supply 16 V overvoltage warning
	0 = no overvoltage warning
	1 = overvoltage warning occurred
D6	speaker fault channel 3
	0 = no speaker fault
	1 = speaker fault
D5 and D4	channel 3 DC-load or AC-load detection
	if bit IB4[D4] = 1, AC-load detection is enabled, bit D5 does not care, bit D4 has the following meaning:
	0 = no AC-load
	1 = AC-load detected
	if bit IB4[D4] = 0, AC-load detection is disabled, bits D5 and D4 are available for DC-load detection:
	00 = normal load
	01 = line driver load
	10 = open load
	11 = not valid
D3	channel 3 shorted load
	0 = no shorted load
	1 = shorted load
D2	channel 3 output offset
	0 = no output offset
	1 = output offset
D1	channel 3 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 3 short to ground
	0 = no short to ground
	1 = short to ground

Remark: Data bits are only reset (cleared after read) after reading all 5 data bytes.

Table 18. Data byte DB5

Bit	Description
D7	power supply undervoltage
	0 = no undervoltage
	1 = undervoltage occurred
D6	power supply overvoltage
	0 = no overvoltage
	1 = overvoltage has occurred
D5	system status with start-up diagnostics or amplifier start-up
	0 = system not busy
	1 = system busy
D4	V_P below/above 7.5 V
	0 = V_P above 7.5 V
	1 = V_P has dropped below 7.5 V
D3	V_P below/above 10 V
	0 = V_P above 10 V
	1 = V_P has dropped below 10 V
D2	undervoltage protection
	0 = no undervoltage protection occurred
	1 = undervoltage protection occurred (engine start)
D1	best efficiency protection
	0 = no best efficiency protection occurred
	1 = best efficiency protection occurred (one or several switches too hot and amplifier set to BTL mode
D0	amplifier and output stage status
	0 = amplifier switched off, output stage high impedance
	1 = amplifier switched on, output stage active

Remark: Data bits are only reset (cleared after read) after reading 5 data bytes.

9. Limiting values

Table 19. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	operating	6	18	V
		non-operating	−1	+50	V
		load dump protection; duration 50 ms, rise time > 2.5 ms	-	50	V
$V_{P(r)}$	reverse supply voltage	10 minutes maximum	-	−2	V
I_{OSM}	non-repetitive peak output current		-	13	A
I_{ORM}	repetitive peak output current		-	8	A

Table 19. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{j(max)}$	maximum junction temperature			-	150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature	heatsink of sufficient size to ensure T_j does not exceed 150 °C		–40	+105	°C
$V_{(prot)}$	protection voltage	AC and DC short-circuit voltage of output pins and across the load		-	V_P	V
$V_{i(max)}$	maximum input voltage	RMS value; before capacitor; R_S = 100 Ω		-	5	V
V_x	voltage on pin x					
	SCL and SDA			0	6.5	V
	SVR, ACGND and DIAG			0	10	V
	STB		[1]	0	24	V
P_{tot}	total power dissipation	T_{case} = 70 °C		-	80	W
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R_S = 1.5 kΩ	[2]	-	2000	V
		CDM	[3]			
		corner pins		-	750	V
		non-corner pins		-	500	V

[1] 10 kΩ series resistance if connected to V_P.

[2] Human Body Model (HBM): all pins have passed all tests to 2500 V to guarantee 2000 V, according to class II.

[3] Charged-Device Model (CDM).

10. Thermal characteristics

Table 20. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
DBS27P and RDBS27P				
$R_{th(j-c)}$	thermal resistance from junction to case		1.15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		40	K/W

11. Characteristics

Table 21. Characteristics

Refer to test circuit (see Figure 38); T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage behavior						
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω	6	14.4	18	V
		R_L = 2 Ω	6	14.4	16	V
I_q	quiescent current	no load	-	260	350	mA
		no load; V_P = 7 V	-	190	-	mA
I_{off}	off-state current	V_{STB} = 0.4 V	-	4	10	μA
V_O	output voltage	DC				
		amplifier on; high gain/low gain mode	6.6	7.1	7.6	V
		line driver mode; IB4[D2] = 0; IB3[D5:D6] = 1	3.0	3.4	3.8	V
$V_{P(low)(mute)}$	low supply voltage mute	rising supply voltage				
		IB4[D0] = 1	7.0	7.7	8.1	V
		IB4[D0] = 0	5.4	5.7	6.2	V
		falling supply voltage				
		IB4[D0] = 1	6.5	7.2	7.7	V
		IB4[D0] = 0	5.2	5.5	5.9	V
$\Delta V_{P(low)(mute)}$	low supply voltage mute hysteresis	IB4[D0] = 1	0.1	0.5	0.8	V
		IB4[D0] = 0	0.1	0.3	0.7	V
$V_{P(ovp)pwarn}$	pre-warning overvoltage protection supply voltage	rising supply voltage	15.2	16	16.9	V
		falling supply voltage	14.4	15.2	16.2	V
		hysteresis	-	0.8	-	V
$V_{th(ovp)}$	overvoltage protection threshold voltage	rising supply voltage	18	20	22	V
V_{POR}	power-on reset voltage	falling supply voltage	-	3.1	4.5	V
$V_{O(offset)}$	output offset voltage	amplifier on	−75	0	+75	mV
		amplifier mute	−25	0	+25	mV
		line driver mode	−45	0	+45	mV

Table 21. Characteristics *...continued*

Refer to test circuit (see Figure 38); T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Mode select and second clip detection: pin STB							
V_{STB}	voltage on pin STB	off-by mode selected					
		I²C-bus mode		-	-	0.8	V
		legacy mode (I²C-bus mode off)		-	-	0.8	V
		mute selected					
		legacy mode (I²C-bus mode off)		2.5	-	4.5	V
		operating mode selected					
		I²C-bus mode		2.5	-	V_P	V
		legacy mode (I²C-bus mode off)		5.9	-	V_P	V
		low voltage on pin STB when pulled LOW during clipping	[1]				
		I_{STB} = 150 µA		5.6	5.9	6.5	V
		I_{STB} = 500 µA		6.1	-	7.4	V
I_{STB}	current on pin STB	0 V < V_{STB} < 8.5 V; clip detection not active	[1]	-	5	30	µA
Start-up/shut-down/mute timing							
t_{wake}	wake-up time	time after wake-up via pin STB before first I²C-bus transmission is recognized; see Figure 3		-	300	500	µs
$I_{LO(SVR)}$	output leakage current on pin SVR			-	-	5	µA
$t_{d(mute\_off)}$	mute off delay time	time from amplifier start to 10 % of output signal; I_{LO} = 0 µA	[2]				
		I²C-bus mode; with I_{LO} = 5 µA → +15 ms; no DC-load (IB1[D1] = 0); see Figure 3		-	430	650	ms
		legacy mode; with I_{LO} = 5 µA → +20 ms; V_{STB} = 7 V; R_{ADSEL} = 0 Ω; see Figure 4		-	430	650	ms
t_{amp_on}	amplifier on time	time from amplifier start to amplifier on; 90 % of output signal; I_{LO} = 0 µA	[2]				
		I²C-bus mode; with I_{LO} = 5 µA → +30 ms; no DC-load (IB1[D1] = 0); see Figure 3		-	550	800	ms
		legacy mode; with I_{LO} = 5 µA → +20 ms; V_{STB} = 7 V; R_{ADSEL} = 0 Ω; see Figure 4		-	550	800	ms

Table 21. Characteristics *...continued*

Refer to test circuit (see Figure 38); T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{off}	amplifier switch-off time	time to DC output voltage < 0.1 V; I_{LO} = 0 μA [2]				
		I²C-bus mode; with I_{LO} = 5 μA → +0 ms; see Figure 3	250	500	750	ms
		via pin STB; (IB4[D6] = 0); with I_{LO} = 5 μA → +0 ms; see Figure 4	250	500	750	ms
$t_{d(mute-on)}$	delay time from mute to on	from 10 % to 90 % of output signal; V_i = 50 mV; I²C-bus mode (IB2[D1, D2] = 1 to 0) or IB2(D0 = 1 to 0) or legacy mode (V_{STB} = 2 V to 7 V); see Figure 4	5	15	40	ms
$t_{d(soft\_mute)}$	soft mute delay time	from 90 % to 10 % of output signal; V_i = 50 mV; I²C-bus mode (IB2[D1, D2] = 0 to 1) or legacy mode (V_{STB} = 7 V to 2 V); see Figure 4	5	15	40	ms
$t_{d(fast\_mute)}$	fast mute delay time	from 90 % to 10 % of output signal; V_i = 50 mV; I²C-bus mode (IB2[D0] = 0 to 1, or V_{STB} from > 5.9 V to < 0.8 V in 1 μs; see Figure 4	-	0.4	1	ms
$t_{(start-Vo(off))}$	engine start to output off time	V_P from 14.4 V to 5 V in 1.5 ms; V_o < 0.5 V; see Figure 5	-	0.1	1	ms
$t_{(start-SVRoff)}$	engine start to SVR off time	V_P from 14.4 V to 5 V in 1.5 ms; V_{SVR} < 0.7 V; see Figure 5	-	40	75	ms
I²C-bus interface [3]						
V_{IL}	LOW-level input voltage	pins SCL and SDA	-	-	1.5	V
V_{IH}	HIGH-level input voltage	pins SCL and SDA	2.3		5.5	V
V_{OL}	LOW-level output voltage	pin SDA; I_L = 5 mA	-	-	0.4	V
f_{SCL}	SCL clock frequency		-	400	-	kHz
V_{ADSEL}	voltage on pin ADSEL	I²C-bus address A[6:0] = 1101 101				
		$Rseries_{ADSEL}$ = 0 Ω	4	5	11	V
		$Rseries_{ADSEL}$ = 100 kΩ	-	-	V_P	V
$I_{I(ADSEL)}$	input current on pin ADSEL	V_{STB} = 5 V; V_{ADSEL} = 5 V	-	2	10	μA
R_{ADSEL}	resistance on pin ADSEL	I²C-bus address A[6:0] = 1101 110	99	100	101	kΩ
		I²C-bus address A[6:0] = 1101 111	29.7	30	30.3	kΩ
		I²C-bus address A[6:0] = 1101 010	9.9	10	10.1	kΩ
		legacy mode	-	-	0.47	kΩ
$V_{P(latch)}$	latch supply voltage	will not react to address selection changes	-	-	6	V

Table 21. Characteristics *...continued*

Refer to test circuit (see Figure 38); T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up diagnostics						
t_{sudiag}	start-up diagnostic time	from start-up diagnostic command via I²C-bus until completion of start-up diagnostic; V_O + < 0.1 V; V_O − < 0.1 V (no load) IB1[D1] = 1; see Figure 16	50	130	250	ms
$t_{d(sudiag-on)}$	start-up diagnostic to on delay time	at 90 % of output signal; IB1[D0:D1] = 11; see Figure 16	-	680	-	ms
V_{offset}	offset voltage	startup diagnostic offset voltage under no load condition	1.3	2	2.5	V
$R_{Ldet(sudiag)}$	start-up diagnostic load detection resistance	shorted load				
		high gain; IB3[D6:D5] = 00	-	-	0.5	Ω
		low gain; IB3[D6:D5] = 11	-	-	1.5	Ω
		normal load				
		high gain (IB3[D6:D5] = 00)	1.5	-	20	Ω
		low gain (IB3[D6:D5] = 11)	3.2	-	20	Ω
		line driver load	80	-	200	Ω
		open load	400	-	-	Ω
Amplifier diagnostics						
$V_{OL(DIAG)}$	LOW-level output voltage on pin DIAG	fault condition; I_{DIAG} = 1 mA	-	-	0.3	V
$V_{O(offset\_det)}$	output voltage at offset detection		±1.0	±1.3	±2.0	V
THD_{clip}	total harmonic distortion clip detection level	V_P > 10 V; IB3[D7] = 0				
		IB2[D7:D6] = 10	-	10	-	%
		IB2[D7:D6] = 01	-	5	-	%
		IB2[D7:D6] = 00	-	2	-	%
$T_{j(AV)(pwarn)}$	pre-warning average junction temperature	IB3[D4] = 0 or legacy mode	150	160	170	°C
		IB3[D4] = 1	125	135	145	°C
$T_{j(AV)(G(-0.5dB))}$	average junction temperature for 0.5 dB gain reduction	V_i = 0.05 V; best efficiency mode turns off when activated	-	175	-	°C
$\Delta G_{(th\_fold)}$	gain reduction of thermal foldback	when all channels switch off	-	20	-	dB
I_o	output current	I²C-bus mode; IB5[D7] = 0; AC load bit set; peak current				
		IB4[D1] = 1	500	-	-	mA
		IB4[D1] = 0	275	-	-	mA
		I²C-bus mode; IB5[D7] = 0; AC load bit not set; peak current				
		IB4[D1] = 1	-	-	250	mA
		IB4[D1] = 0	-	-	100	mA

Table 21. Characteristics *...continued*

Refer to test circuit (see Figure 38); T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier							
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %		18	20	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %		23	25	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 0.5 %		29	32	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %		40	44	-	W
$P_{o(max)}$	maximum output power	R_L = 4 Ω; V_P = 14.4 V; V_i = 2 V RMS square wave		37	40	-	W
		R_L = 4 Ω; V_P = 15.2 V; V_i = 2 V RMS square wave		41	45	-	W
		R_L = 2 Ω; V_P = 14.4 V; V_i = 2 V RMS square wave		58	64	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω; BTL mode		-	0.01	0.1	%
		P_o = 1 W; f_i = 1 kHz; R_L = 4 Ω; V_P = 7 V; BTL and best efficiency mode		-	0.01	0.1	%
		P_o = 4 W; f_i = 1 kHz; R_L = 4 Ω; best efficiency mode		-	0.03	0.1	%
		P_o = 1 W to 12 W; f_i = 20 kHz; R_L = 4 Ω; best efficiency mode		-	0.3	0.4	%
		V_o = 1 V (RMS) and 4 V (RMS), f_i = 1 kHz; line driver mode		-	0.02	0.05	%
		P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω; low gain mode		-	0.01	0.1	%
α_{cs}	channel separation	best efficiency mode; R_S = 1 kΩ; R_{ACGND} = 250 Ω	[4]				
		f_i = 1 kHz		65	80	-	dB
		f_i = 10 kHz		55	65	-	dB
SVRR	supply voltage ripple rejection	f_i = 1 kHz; R_S = 1 kΩ; R_{ACGND} = 250 Ω; best efficiency mode; tested at 10.5 V	[4]	55	70	-	dB
CMRR	common mode rejection ratio	amplifier mode; V_{cm} = 0.3 V (p-p); f_i = 1 kHz to 3 kHz, R_S = 1 kΩ; R_{ACGND} = 250 Ω; best efficiency mode	[4]				
		common mode input to differential output ($V_{O(dif)}$ / $V_{I(cm)}$ + 26 dB)		55	65	-	dB
		common mode input to common mode output ($V_{O(cm)}$ / $V_{I(cm)}$ + 26 dB)		50	58	-	dB

Table 21. Characteristics *...continued*

Refer to test circuit (see Figure 38); T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_o	output voltage variation	plop during switch-on and switch-off; best efficiency mode [5]				
		from off to mute and mute to off	-	-	7.5	mV
		from mute to on and on to mute (soft mute)	-	-	7.5	mV
		from off to on and on to off (start-up diagnostic enabled)	-	-	7.5	mV
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz (6th order); R_S = 1 kΩ				
		mute mode	-	15	23	μV
		line driver mode	-	25	33	μV
		amplifier mode; best efficiency mode	-	43	65	μV
		amplifier mode; best efficiency mode; R_S = 50 Ω	-	40	60	μV
$G_{v(amp)}$	voltage gain amplifier mode	single-ended in to differential out; best efficiency mode	25.5	26	26.5	dB
$G_{v(ld)}$	voltage gain line driver mode	single-ended in to differential out; best efficiency mode	15.5	16	16.5	dB
Z_i	input impedance	T_{amb} = −40 °C to +105 °C	38	62	99	kΩ
		T_{amb} = 0 °C to 105 °C	55	62	99	kΩ
α_{mute}	mute attenuation	$V_{o(on)}$ / $V_{o(mute)}$; V_i = 50 mV	80	92	-	dB
$V_{o(mute)(RMS)}$	RMS mute output voltage	V_i = 1 V RMS; filter 20 Hz to 22 kHz	-	16	29	μV
B_p	power bandwidth	−1 dB	-	20 to 20000	-	Hz
$C_{L(crit)}$	critical load capacitance	no oscillation; open load and 2 Ω load; all outputs to GND or across the load	33	-	-	nF
Best efficiency mode control						
$V_{o(swoff)be}$	best efficiency switch-off output voltage	best efficiency switch open				
		4 Ω load selected; IB5[D4] = 1	-	0.9	-	V
		2 Ω load selected; IB5[D4] = 0	-	1.7	-	V
$R_{sw(be)}$	best efficiency switch resistance		-	1.0	-	Ω

[1] V_{STB} depends on the current into pin STB: minimum = (1429 Ω × I_{STB}) + 5.4 V, maximum = (3143 Ω × I_{STB}) + 5.6 V.

[2] The times are specified without leakage current. For a leakage current of 5 μA on pin SVR, the delta time is specified. If the capacitor value on pin SVR changes ± 30 %, the specified time will also change ± 30 %. The specified times include an ESR of 15 Ω for the capacitor on pin SVR.

[3] Standard I²C-bus specification: maximum LOW-level = 0.3V_{DD}, minimum HIGH-level = 0.7V_{DD}. To comply with 5 V and 3.3 V logic the maximum LOW-level is defined by V_{DD} = 5 V and the minimum HIGH-level by V_{DD} = 3.3 V.

[4] For optimum channel separation (α_{cs}), supply voltage ripple rejection (SVRR) and common mode rejection ratio (CMRR), a resistor $R_{ACGND} = \frac{R_S}{4}$ Ω must be in series with the ACGND capacitor.

[5] The plop-noise during amplifier switch-on and switch-off is measured using an ITU-R 2 k filter; see Figure 24.

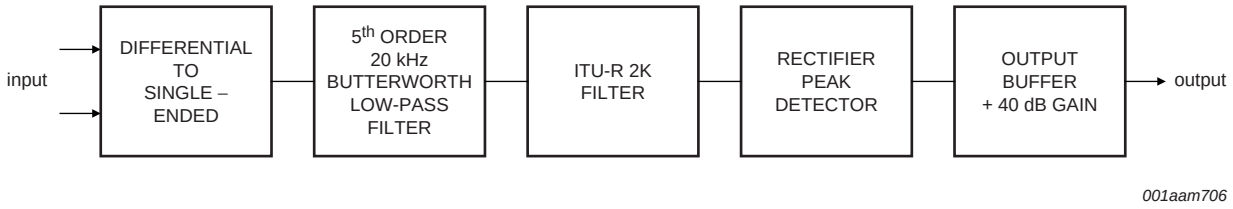
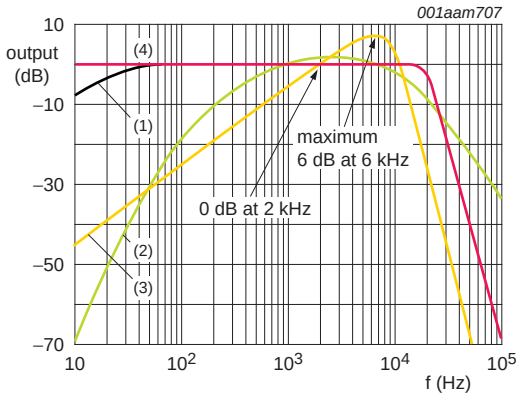


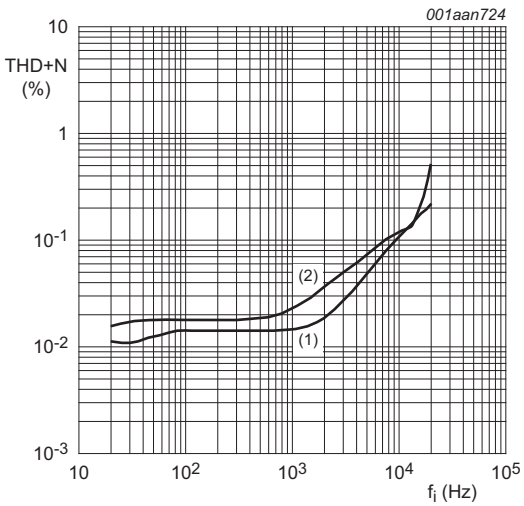
Fig 23. Location of ITU-R 2K filter



(1) 20 Hz.
(2) A-weighting.
(3) ITU-R average response meter.
(4) 20 kHz bandwidth limit.

Fig 24. Plop noise test using ITU-R 2K filter

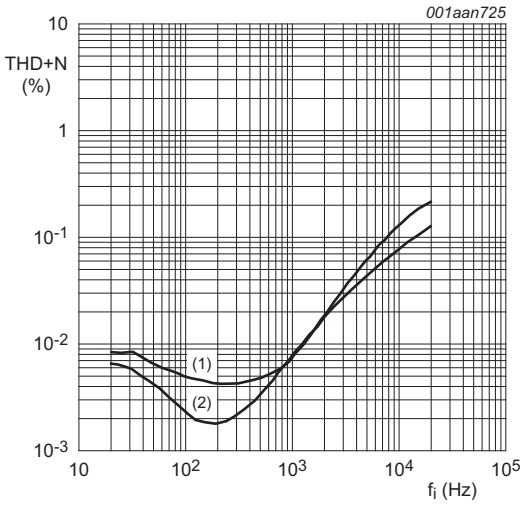
12. Performance diagrams



(1) P_o = 1 W.

(2) P_o = 10 W.

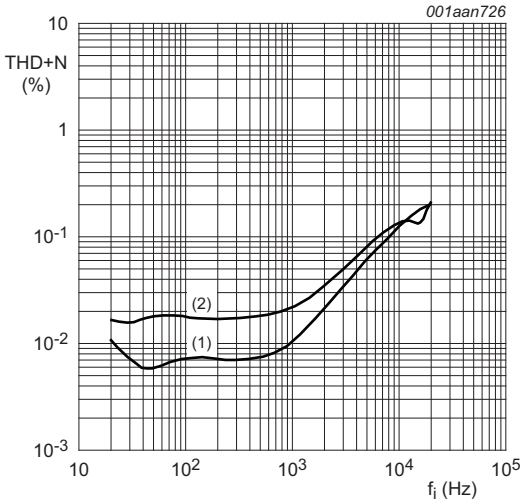
Fig 25. Total harmonic distortion as a function of input frequency; best efficiency mode (R_L = 4 Ω)



(1) P_o = 1 W.

(2) P_o = 10 W.

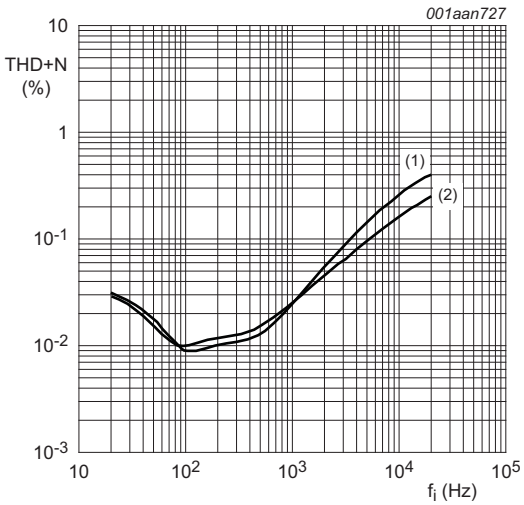
Fig 26. Total harmonic distortion as a function of input frequency; BTL mode (R_L = 4 Ω)



(1) P_o = 1 W.

(2) P_o = 10 W.

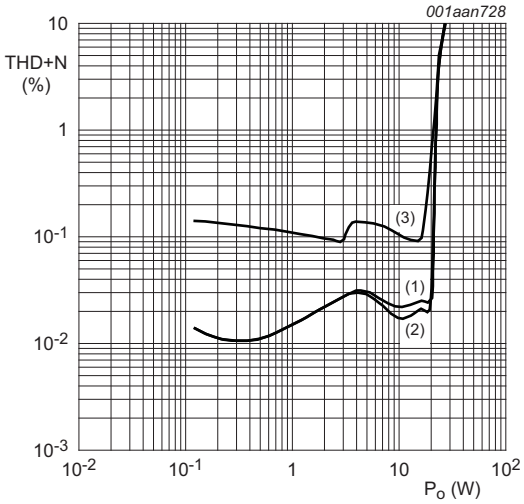
Fig 27. Total harmonic distortion as a function of input frequency; best efficiency mode (R_L = 2 Ω)



(1) P_o = 1 W.

(2) P_o = 10 W.

Fig 28. Total harmonic distortion as a function of input frequency; BTL mode (R_L = 2 Ω)

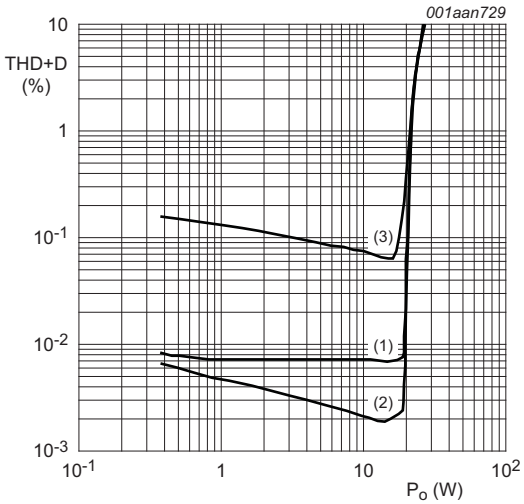


(1) f_i = 1 kHz.

(2) f_i = 100 Hz.

(3) f_i = 10 kHz.

Fig 29. Total harmonic distortion as a function of output power; best efficiency mode (R_L = 4 Ω)

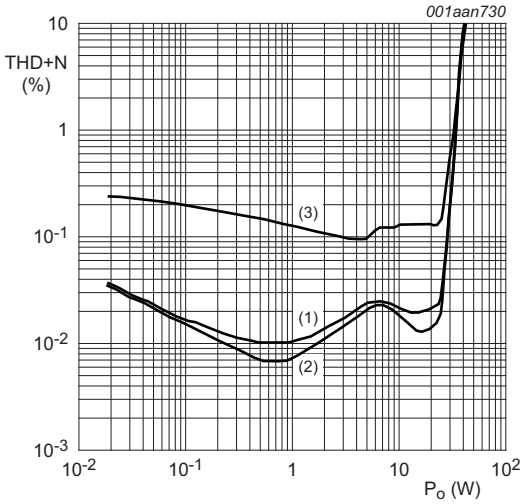


(1) f_i = 1 kHz.

(2) f_i = 100 Hz.

(3) f_i = 10 kHz.

Fig 30. Total harmonic distortion as a function of output power; BTL mode (R_L = 4 Ω)

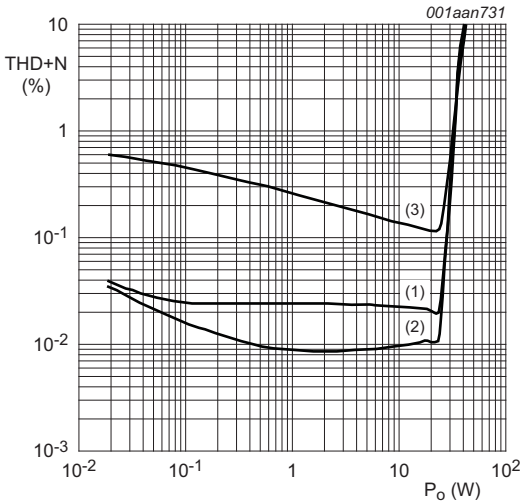


(1) f_i = 1 kHz.

(2) f_i = 100 Hz.

(3) f_i = 10 kHz.

Fig 31. Total harmonic distortion as a function of output power; best efficiency mode (R_L = 2 Ω)

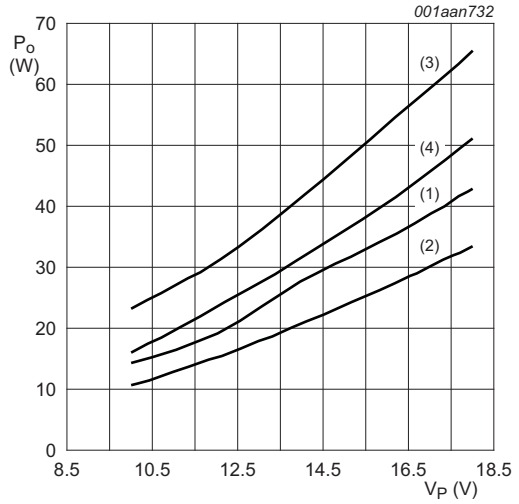


(1) f_i = 1 kHz.

(2) f_i = 100 Hz.

(3) f_i = 10 kHz.

Fig 32. Total harmonic distortion as a function of output power; BTL mode (R_L = 2 Ω)



f_i = 1 kHz.

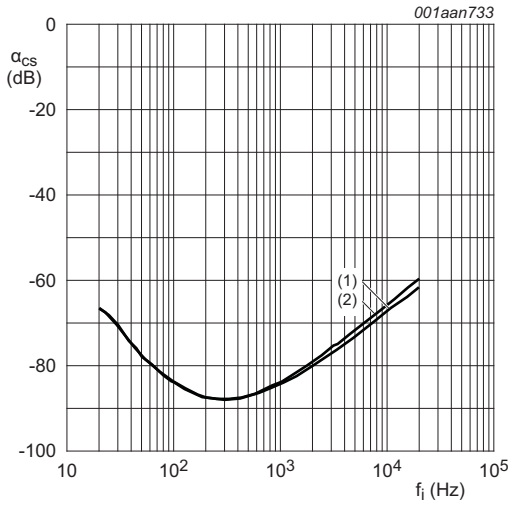
(1) THD = 10 %; 4 Ω load.

(2) THD = 0.5 %; 4 Ω load.

(3) THD = 10 %; 2 Ω load.

(4) THD = 0.5 %; 2 Ω load.

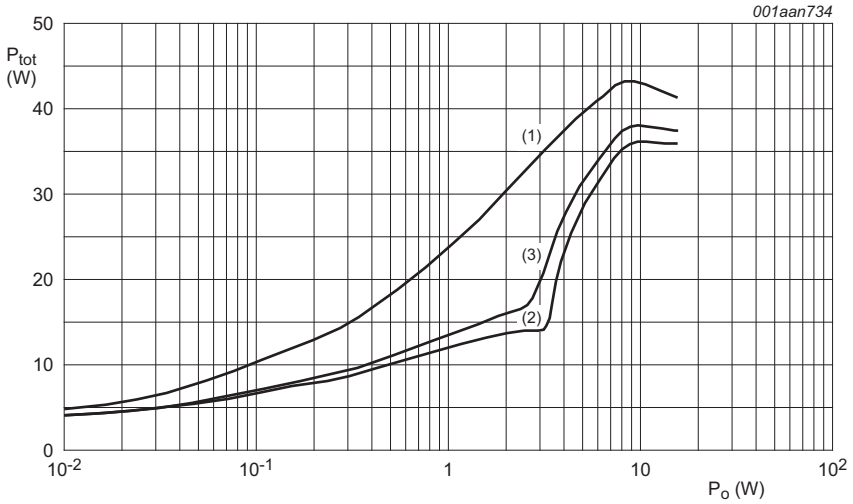
Fig 33. Output power as a function of supply voltage (R_L = 2 Ω and 4 Ω)



(1) S/N (dB) channel 1.

(2) S/N (dB) channel 2.

Fig 34. Channel separation as a function of input frequency (R_L = 4 Ω)



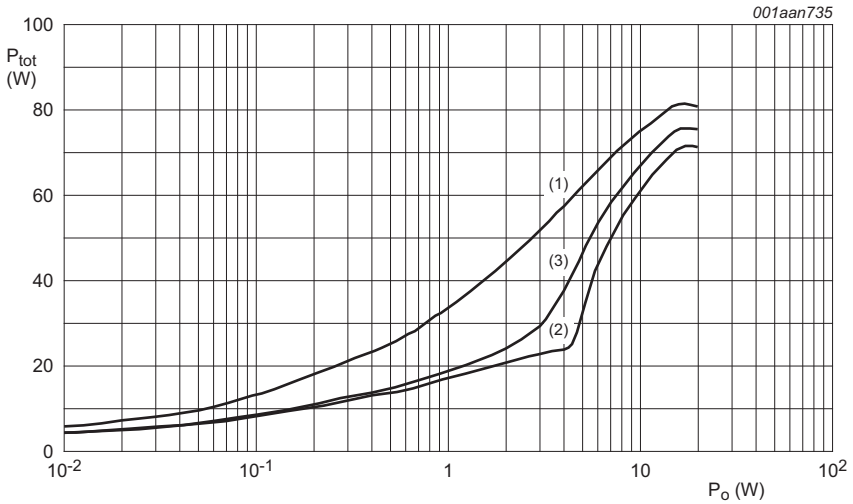
(1) BTL mode.

(2) Best efficiency mode (LF = LR = RF = RR).

(3) Best efficiency mode (LF = !LR = RF = !RR).

Best efficiency mode, LF = !LR = RF = !RR: no correlation between front and rear; full correlation between left and right.

Fig 35. Power dissipation as a function of output power; BTL and best efficiency 4-channel modes (R_L = 4 Ω)



(1) BTL mode.

(2) Best efficiency mode (LF = LR = RF = RR).

(3) Best efficiency mode (LF = !LR = RF = !RR).

Best efficiency mode, LF = !LR = RF = !RR: no correlation between front and rear; full correlation between left and right.

Fig 36. Power dissipation as a function of output power; BTL and best efficiency 4-channel modes (R_L = 2 Ω)

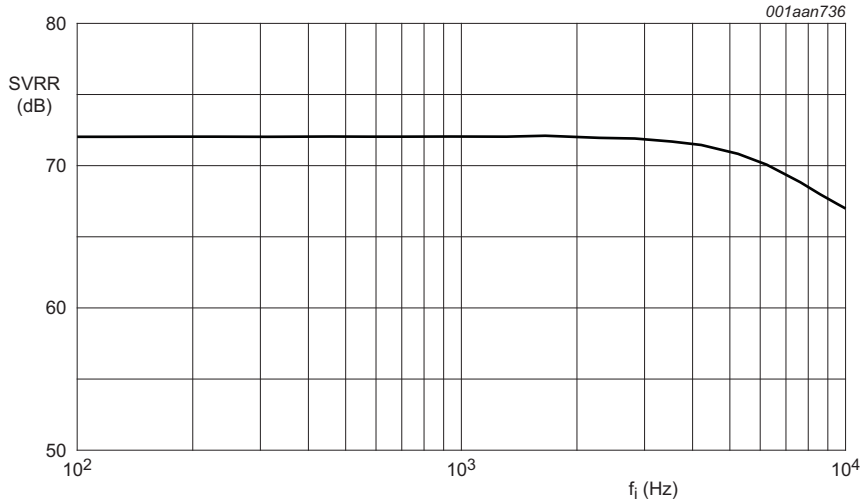
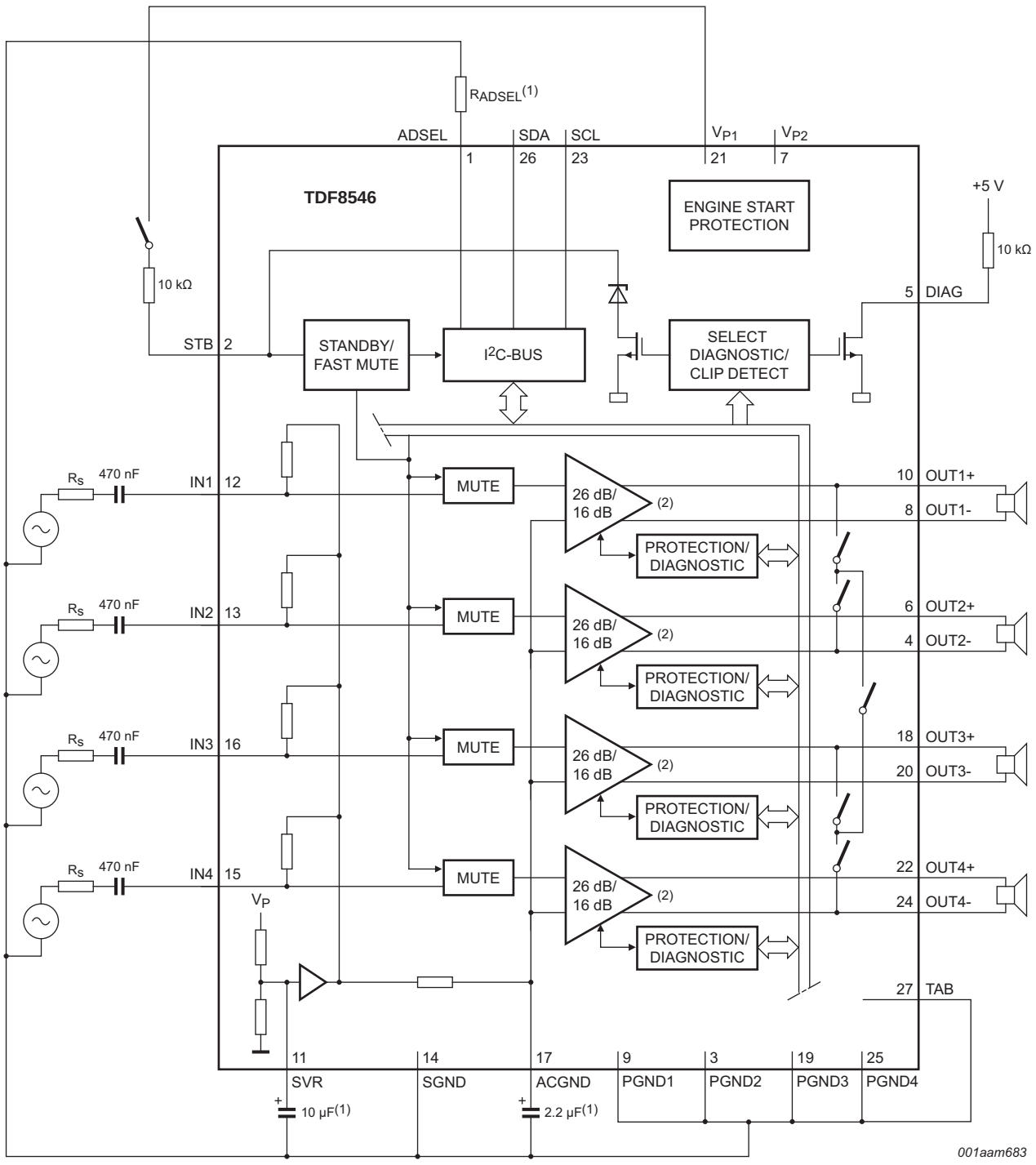


Fig 37. SVRR as a function of frequency; best efficiency mode (25 °C)

13. Application information

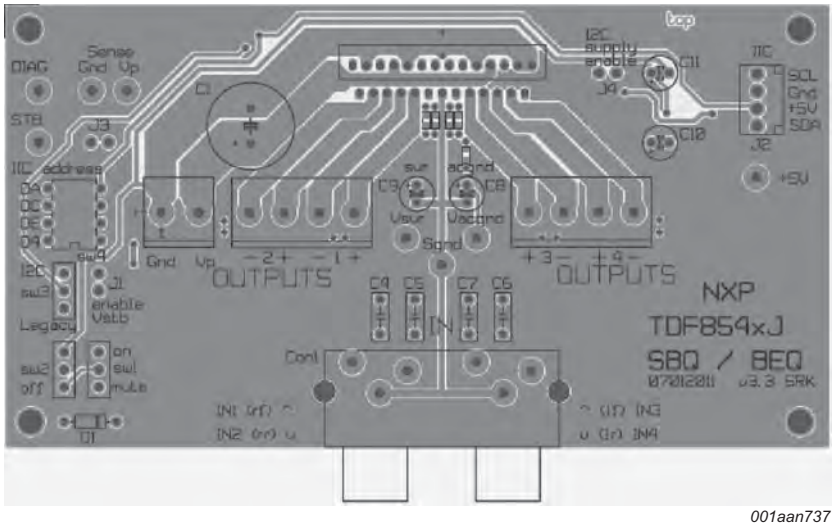


(1) The SVR and ACGND capacitors and the R_{ADSEL} resistor must be connected to pin SGND before it is connected to pin PGNDn; the ACGND capacitor value must be close to 4 × the input capacitor value. 4 × 470 nF capacitors can be used as an alternative to the 2.2 µF capacitor shown.

(2) For EMC reasons, a 10 nF capacitor can be connected between each amplifier output and ground.

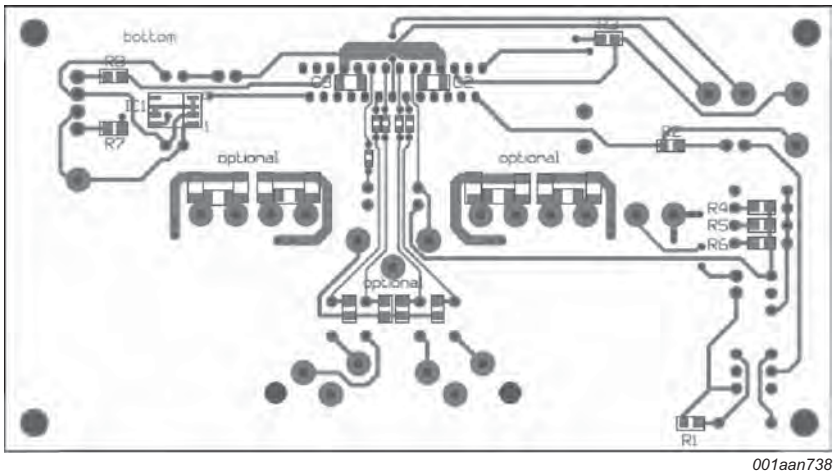
Fig 38. Test and application diagram

13.1 Application PCB layout



001aan737

Fig 39. TDF8546J PCB top view



001aan738

Fig 40. TDF8546J PCB bottom view

Remark: Please use the TDF8546J board to evaluate the TDF8546SD. The TDF8546SD does not fit on this board but is equal in behavior and performance.

13.2 Beep input

Circuit to amplify the beep signal from the microcontroller to all four amplifiers with gain set to 0 dB.

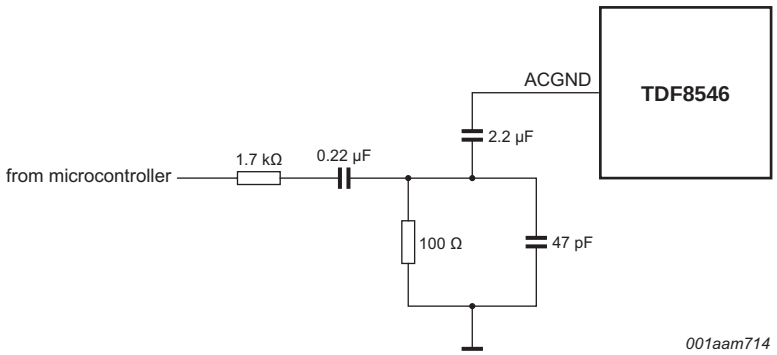


Fig 41. Beep input circuit

13.3 Clip detection on pin STB

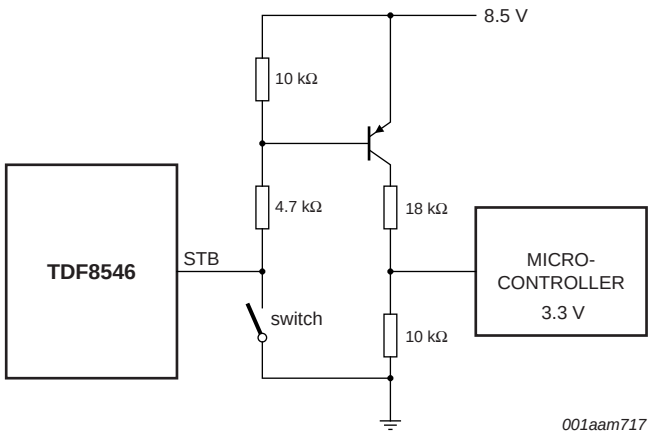


Fig 42. Circuit for testing clip detection on pin STB

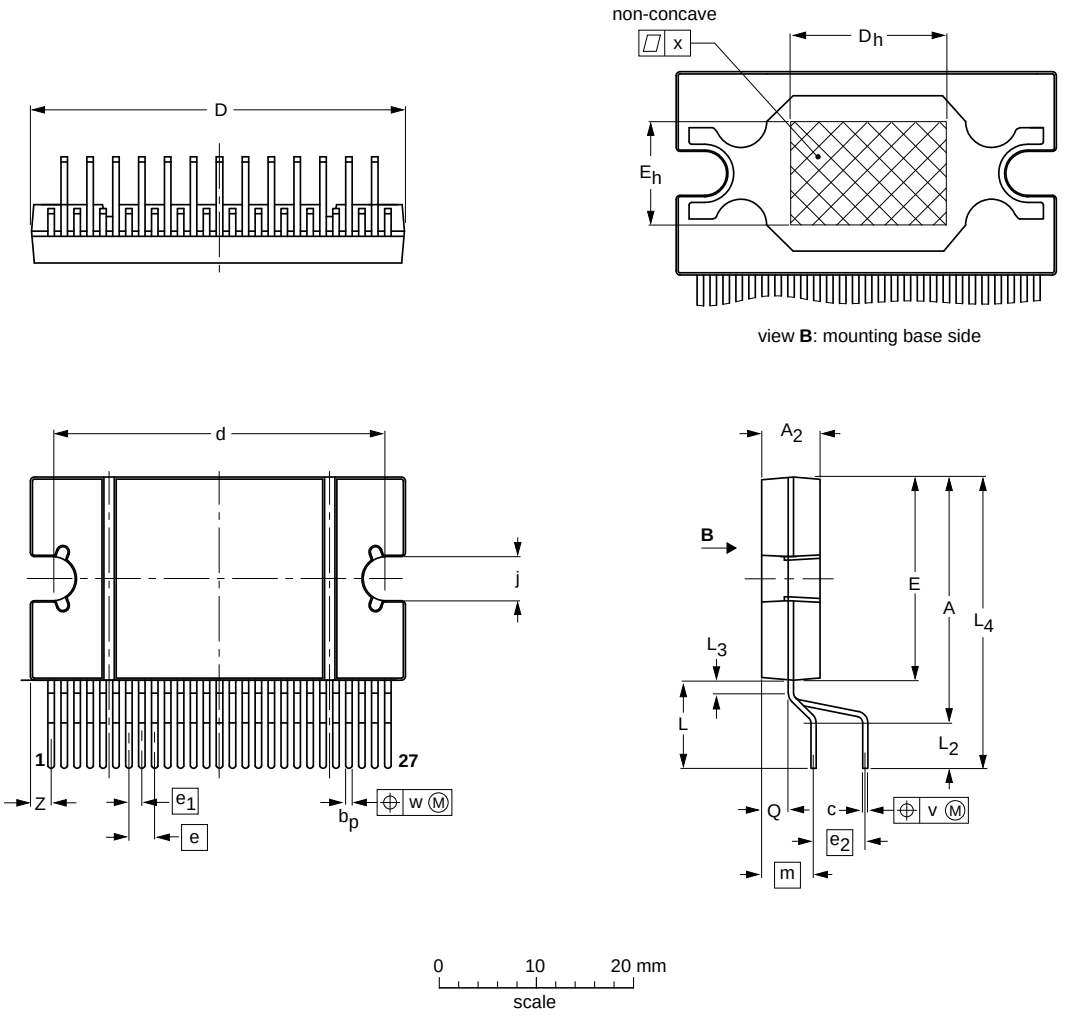
14. Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

DBS27P: plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm) **SOT827-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_2	L_3	L_4	m	Q	v	w	x	$Z^{(1)}$
mm	19	4.65 4.35	0.60 0.45	0.5 0.3	29.2 28.8	25.8 25.4	12	15.9 15.5	2	1	4	8	3.4 3.1	6.8	3.9 3.1	1.15 0.85	22.9 22.1	4	2.1 1.8	0.6	0.25	0.03	1.8 1.2

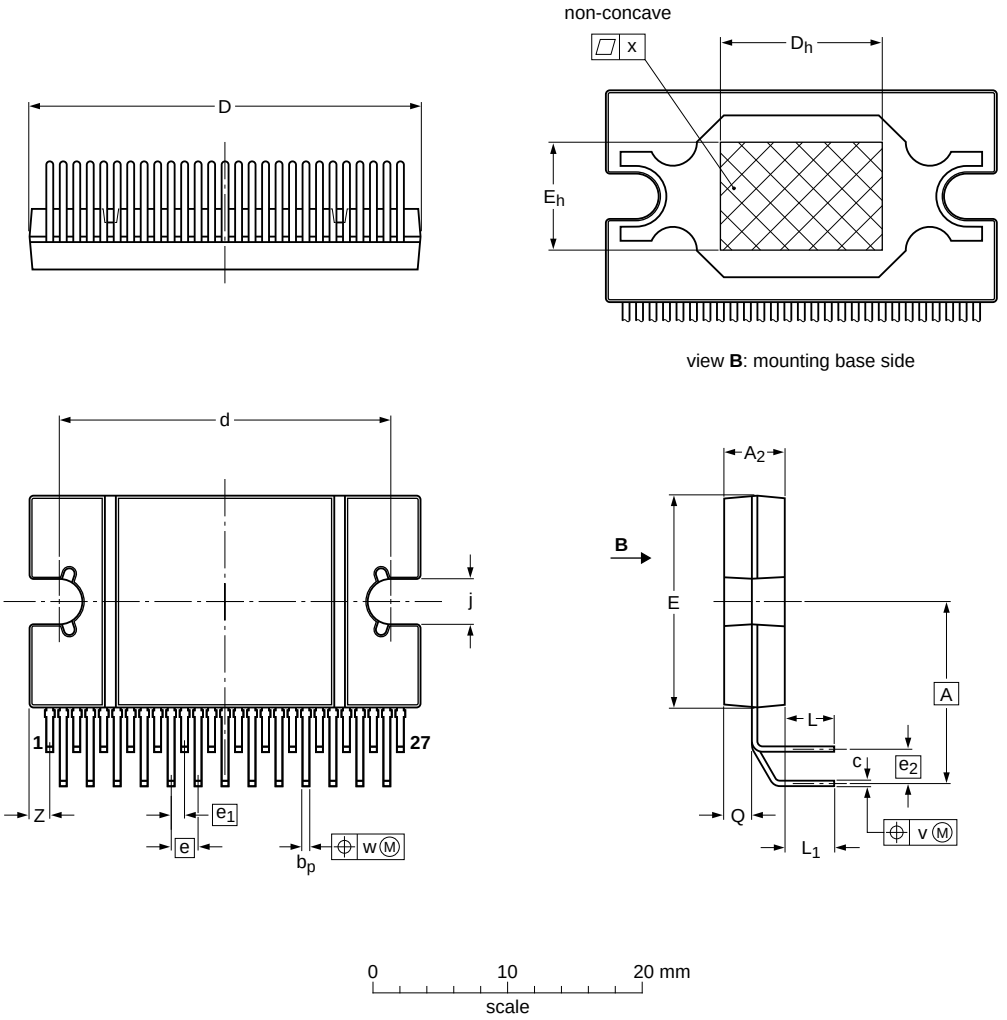
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT827-1	- - -	- - -	- - -			03-07-29

Fig 43. Package outline SOT827-1 (DBS27P)

RDBS27P: plastic rectangular-DIL-bent-SIL (reverse bent) power package; 27 leads (row spacing 2.54 mm) **SOT878-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	D(1)	d	D_h	E(1)	e	e_1	e_2	E_h	j	L	L_1	Q	v	w	x	Z(1)
mm	13.5	4.65 4.35	0.60 0.45	0.5 0.3	29.2 28.8	25.8 25.4	12	15.9 15.5	2	1	2.54	8	3.4 3.1	3.75 3.15	3.75 3.15	2.1 1.8	0.6	0.25	0.03	1.8 1.2

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT878-1						~~05-01-11~~ 05-01-26

Fig 44. Package outline SOT878-1 (RDBS27P)

16. Abbreviations

Table 22. Abbreviations

Acronym	Description
BCDMOS	Bipolar CMOS/DMOS
BEQ	Best Efficiency Quad (4 amplifiers)
BTL	Bridge Tied Load
CMOS	Complementary Metal-Oxide Semiconductor
DMOS	Diffusion Metal Oxide Semiconductor
DSP	Digital Signal Processor
EMC	ElectroMagnetic Compatibility
ESR	Equivalent Series Resistance
IPAS	Integrated Power Amplifier and Stabilizer
NMOS	Negative Metal Oxide Semiconductor
PMOS	Positive Metal Oxide Semiconductor
POR	Power-On Reset
SOAR	Safe Operating ARea
SOI	Silicon On Insulator

17. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8546 v.4	20110919	Product data sheet	-	TDF8546 v.3
Modifications:	• Section 7.6.3 “AC load detection”: added text relating to disabling best efficiency mode for AC-load detection. • Figure 19: updated. • Table 21 “Characteristics”: updated amplifier diagnostics, I_o output current.			
TDF8546 v.3	20110830	Product data sheet	-	TDF8546 v.2
Modifications:	• Updates throughout entire document • Removed references to type number TDF8546TH and TDF8546JS			
TDF8546 v.2	20100107	Objective data sheet	-	TDF8546 v.1
TDF8546 v.1	20101216	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 19 September 2011
Document identifier: TDF8546