FAIRCHILD SEMICONDUCTOR™

July 1996

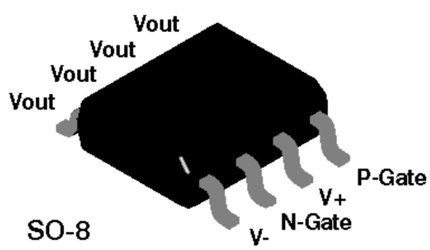
NDS8858H
Complementary MOSFET Half Bridge

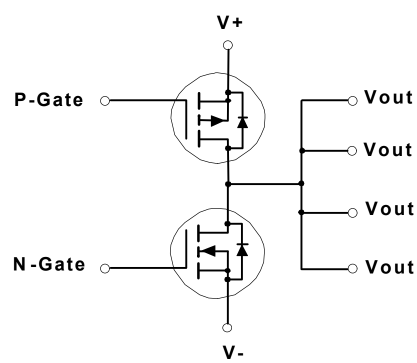
General Description

These Complementary MOSFET half bridge devices are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage half bridge applications or CMOS applications when both gates are connected together.

Features

- N-Channel 6.3A, 30V, $R_{DS(ON)}$=0.035Ω @ V_{GS}=10V.
  P-Channel -4.8A, -30V, $R_{DS(ON)}$=0.065Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Matched pair for equal input capacitance and power capability .





Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		20	-20	V
I_D	Drain Current - Continuous	(Note 1a &2)	6.3	-4.8	A
	- Pulsed		20	20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5		W
	(Single Device)	(Note 1b)	1.2		
		(Note 1c)	1		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Single Device)	(Note 1a)	50		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Single Device)	(Note 1a)	25		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Type	Min	Typ	Max	Units
OFF CHARACTERISTICS								
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA		N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA		P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V		N-Ch			1	µA
			T_J = 55°C				10	µA
		V_{DS} = -24 V, V_{GS} = 0 V		P-Ch			-1	µA
			T_J = 55°C				-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V		All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V		All			-100	nA
ON CHARACTERISTICS (Note 3)								
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA		N-Ch	1	1.6	2.8	V
			T_J = 125°C		0.7	1.2	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA		P-Ch	-1	-1.6	-2.8	
			T_J = 125°C		-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.8 A		N-Ch		0.033	0.035	Ω
			T_J = 125°C			0.046	0.063	
		V_{GS} = 4.5 V, I_D = 3.7 A				0.046	0.05	
		V_{GS} = -10 V, I_D = -4.8 A		P-Ch		0.052	0.065	
			T_J = 125°C			0.075	0.13	
		V_{GS} = -4.5 V, I_D = -3.7 A				0.085	0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V		N-Ch	20			A
		V_{GS} = -10 V, V_{DS} = -5 V		P-Ch	-20			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.8 A		N-Ch		10		S
		V_{DS} = -10 V, I_D = -4.8 A		P-Ch		7		
DYNAMIC CHARACTERISTICS								
C_{iss}	Input Capacitance	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		N-Ch		720		pF
				P-Ch		690		
C_{oss}	Output Capacitance			N-Ch		370		pF
		P-Channel V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		P-Ch		430		
C_{rss}	Reverse Transfer Capacitance			N-Ch		250		pF
				P-Ch		160		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω; P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	N-Ch		12	20	ns
			P-Ch		9	20	
t_r	Turn - On Rise Time		N-Ch		13	30	ns
			P-Ch		20	25	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		29	50	ns
			P-Ch		40	50	
t_f	Turn - Off Fall Time		N-Ch		10	20	ns
			P-Ch		19	40	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 4.8 A, V_{GS} = 10 V; P-Channel V_{DS} = -10 V, I_D = -4.8 A, V_{GS} = -10 V	N-Ch		19	30	nC
			P-Ch		21	30	
Q_{gs}	Gate-Source Charge		N-Ch		2.1		nC
			P-Ch		3.2		
Q_{gd}	Gate-Drain Charge		N-Ch		5.2		nC
			P-Ch		5.2		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			2	A
			P-Ch			-2	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 2)	N-Ch		0.9	1.2	V
		V_{GS} = 0 V, I_S = -2.0 A (Note 2)	P-Ch		-0.85	-1.2	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 2.0 A, dI_F/dt = 100 A/µs	N-Ch			100	ns
		P-Channel V_{GS} = 0 V, I_F = -2.0 A, dI_F/dt = 100 A/µs	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

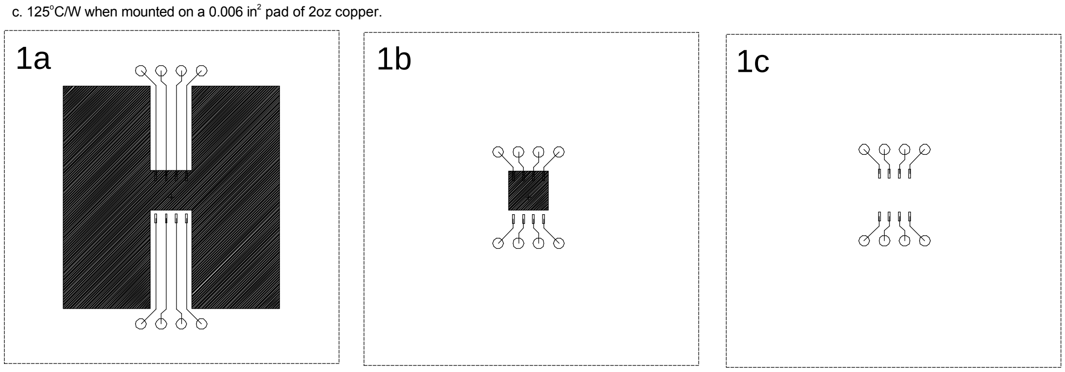
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)}@T_J$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

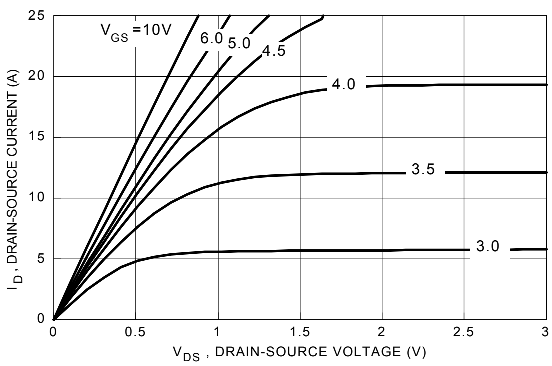


Figure 1. N-Channel On-Region Characteristics.

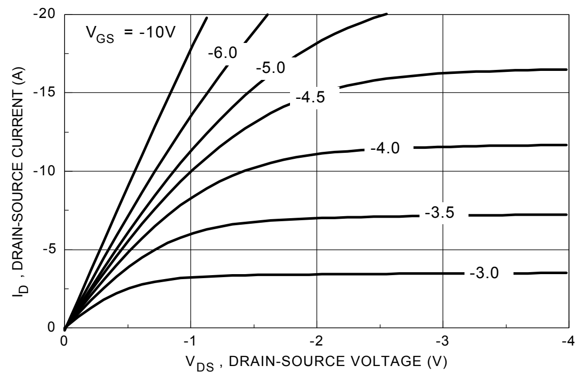


Figure 2. P-Channel On-Region Characteristics.

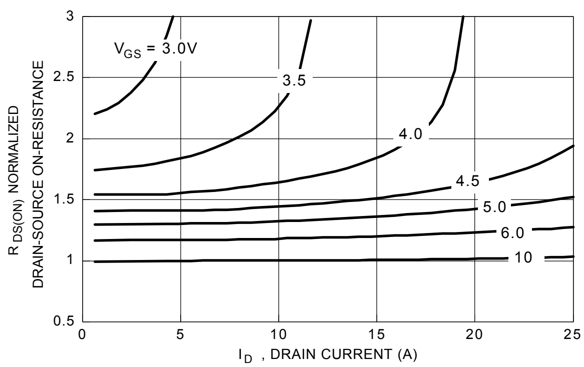


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

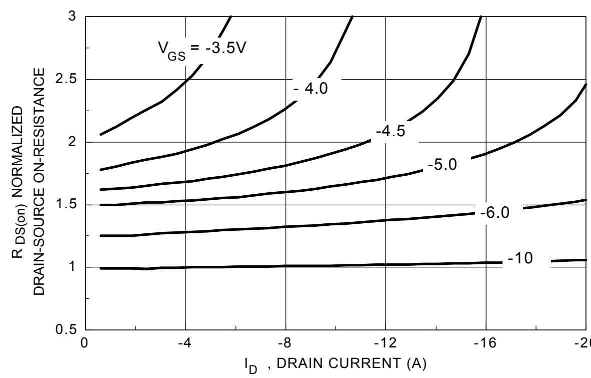


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

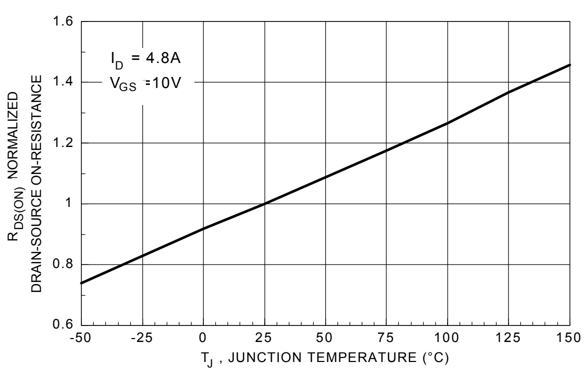


Figure 5. N-Channel On-Resistance Variation with Temperature.

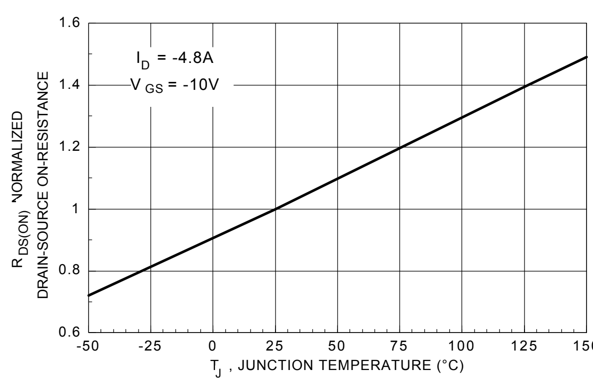


Figure 6. P-Channel On-Resistance Variation with Temperature.

Typical Electrical Characteristics

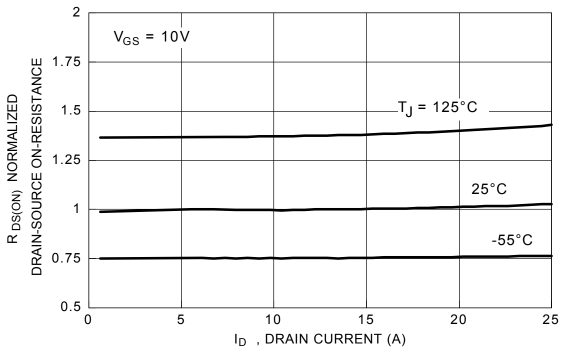


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

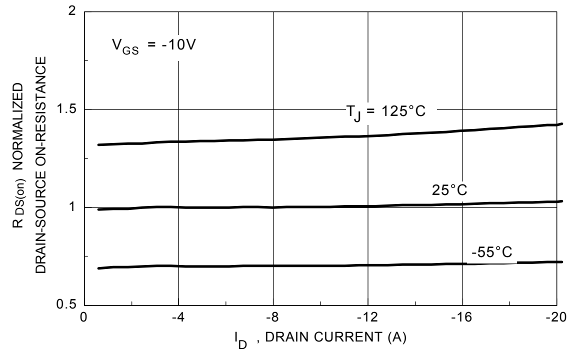


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

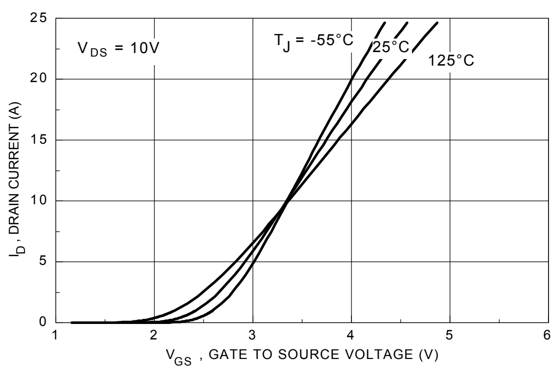


Figure 9. N-Channel Transfer Characteristics.

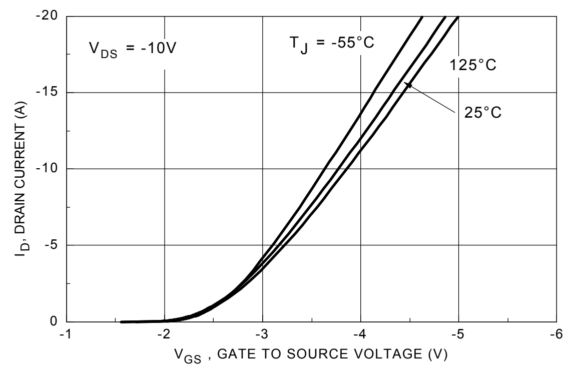


Figure 10. P-Channel Transfer Characteristics.

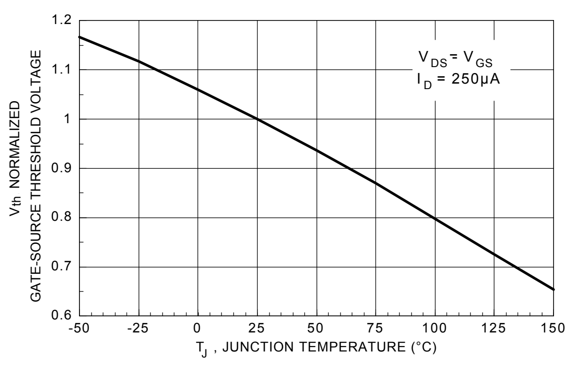


Figure 11. N-Channel Gate Threshold Variation with Temperature.

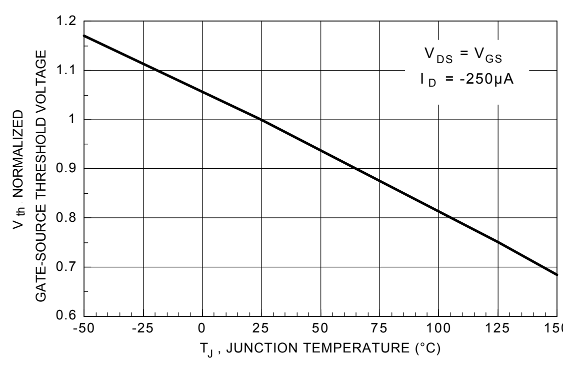


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

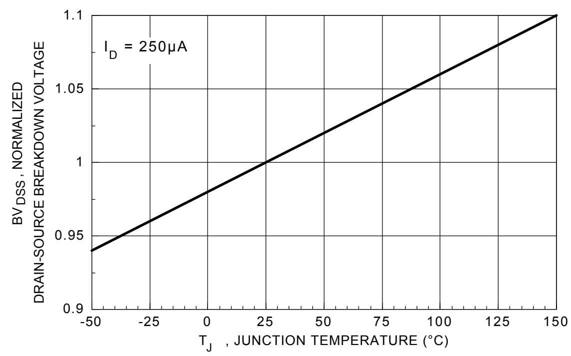


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

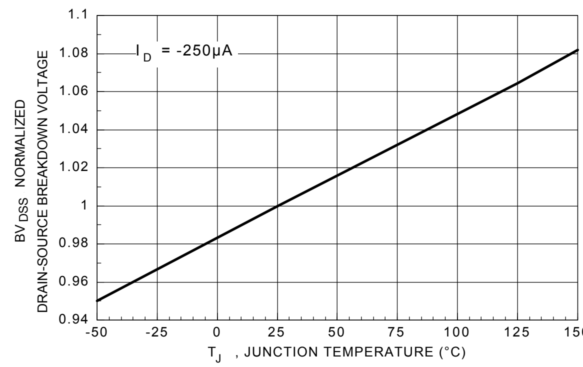


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

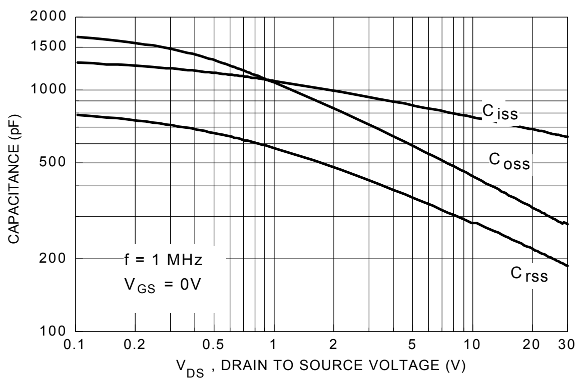


Figure 15. N-Channel Capacitance Characteristics.

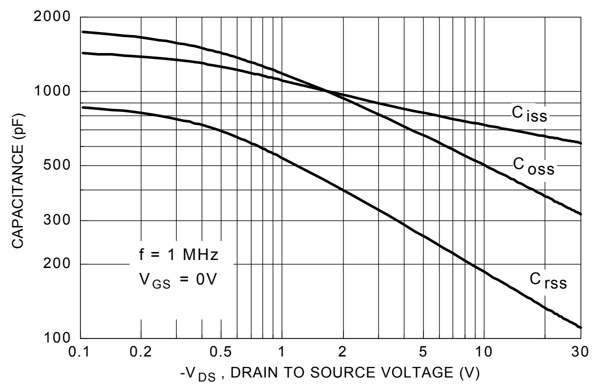


Figure 16. P-Channel Capacitance Characteristics.

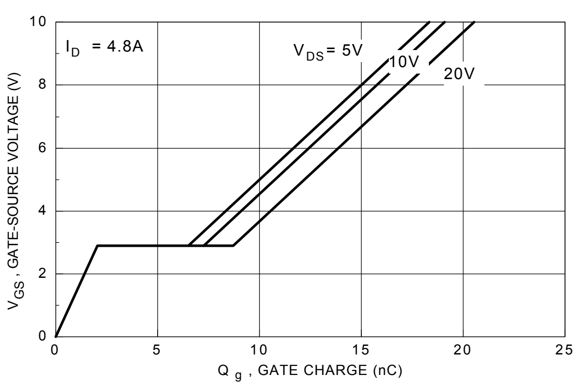


Figure 17. N-Channel Gate Charge Characteristics.

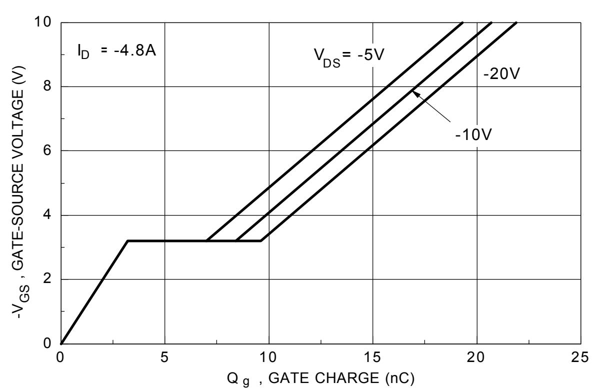


Figure 18. P-Channel Gate Charge Characteristics.

Typical Electrical and Thermal Characteristics

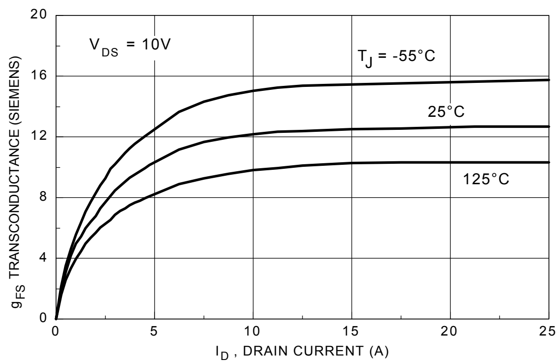


Figure 19. N-Channel Transconductance Variation with Drain Current and Temperature.

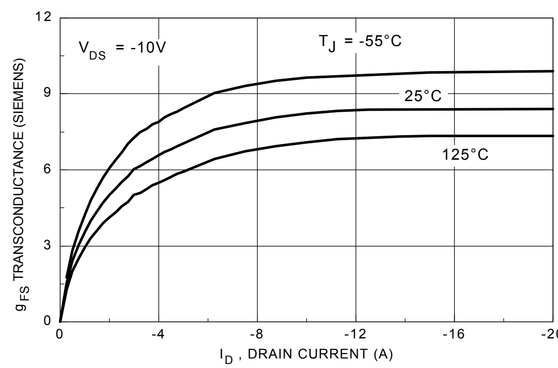


Figure 20. P-Channel Transconductance Variation with Drain Current and Temperature.

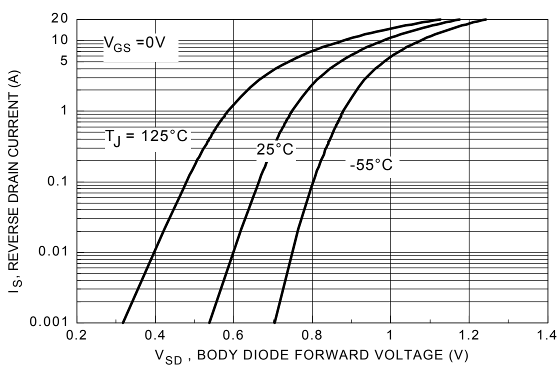


Figure 21. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

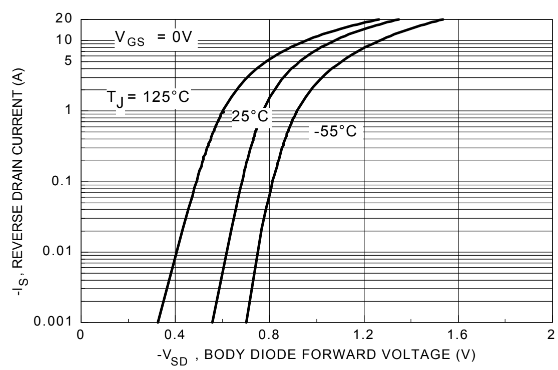


Figure 22. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

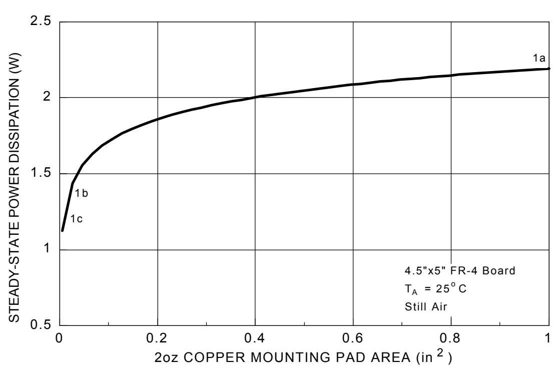


Figure 23. SO-8 Single Device DC Power Dissipation versus Copper Mounting Pad Area.

Typical Thermal Characteristics

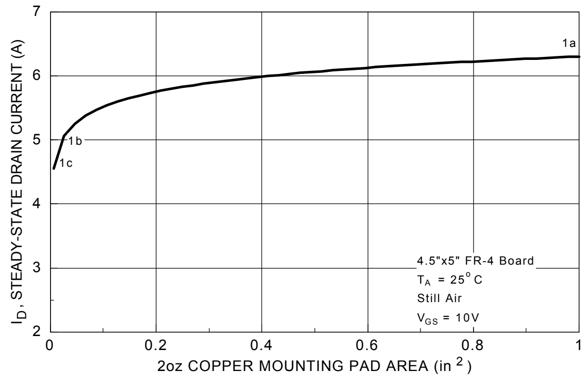


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

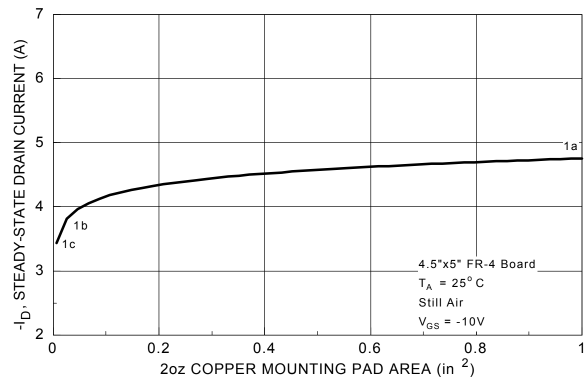


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

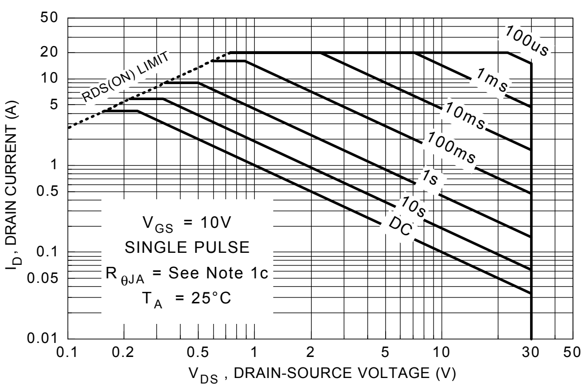


Figure 26. N-Ch Maximum Safe Operating Area.

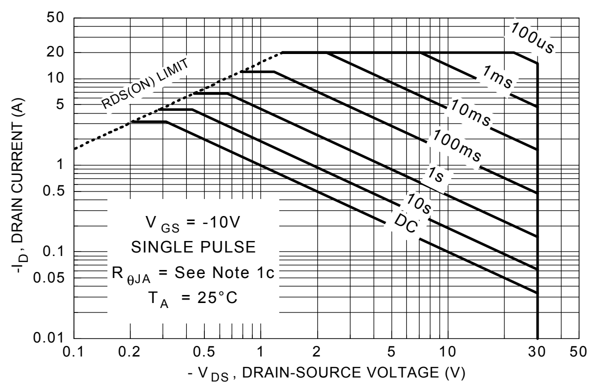


Figure 27. P-Ch Maximum Safe Operating Area.

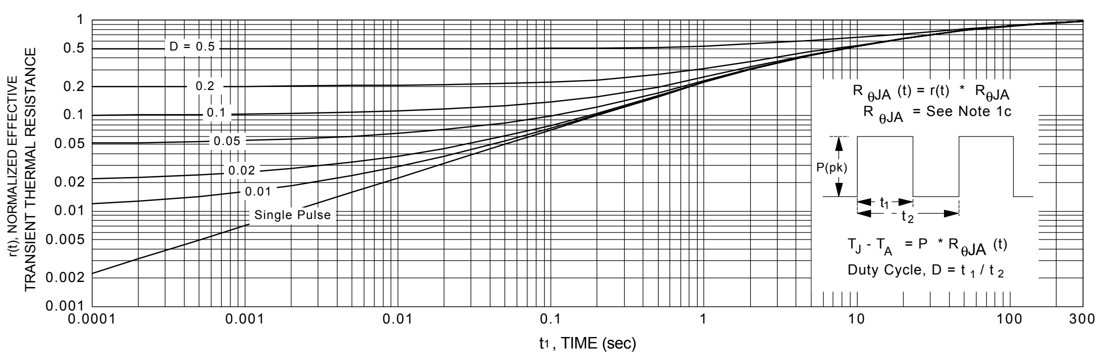


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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