Military-Standard Products

UT6764 Radiation-Hardened 8K x 8 ROM

Preliminary Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

March 1991

FEATURES

- ☐ 70 ns maximum address access time
- ☐ Asynchronous operation
- ☐ TTL-compatible input and output levels
- ☐ Three-state data bus
- ☐ Low operating and standby current
- ☐ User-defined chip select and output enable polarity
- ☐ Full military operating temperature range, −55°C to +125°C, screened to specific test methods listed in Table I MIL-STD-883 Method 5004 for Level S or Level B
- ☐ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 1.0×10^6 rads(Si)
  - Dose rate upset: 1.0×10^9 rads(Si)/sec
  - Dose rate survival: 1.0×10^{12} rads(Si)/sec
- ☐ Latchup immune
- ☐ Packaging options:
  - 28-pin 100-mil center DIP (.600 x 1.4)
  - 28-pin 50-mil center flatpack (.700 x .75)
- ☐ 5-volt operation
- ☐ Post-radiation AC/DC performance characteristics guaranteed to MIL-STD-883 Method 1019 testing

INTRODUCTION

The UT6764 ROM is a high performance, asynchronous, radiation-hardened, 8K x 8 read only memory. The UT6764 ROM features fully asynchronous operation requiring no external clocks or timing strobes. UTMC designed and implemented the UT6764 ROM using an advanced radiation-hardened twin-well CMOS process. Advanced CMOS processing along with a device enable/disable function result in a high performance, power-saving ROM. The combination of radiation-hardness, fast access time, and low power consumption make UT6764 ideal for high-speed systems designed for operation in radiation environments.

PIN NAMES

A(12:0)	Address (2)	G	Output Enable (1)
Q(7:0)	Data Output	VDD	Power
CS1	Select 1 (1)	VSS	Ground
CS2	Select 2 (1)		

Notes:
1. The polarity of the chip select and output enable is user defined. Possible combinations include 000, 001, 010, 011, 100,101, 110, and 111.
2. A12 most significant bit; A0 least significant bit.

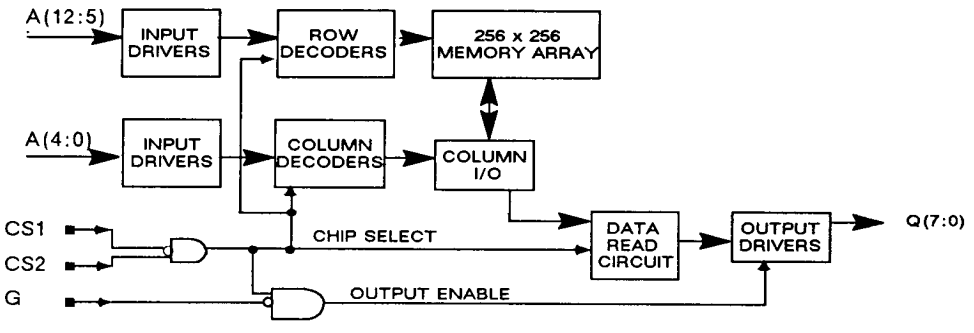


Figure 1. ROM Block Diagram

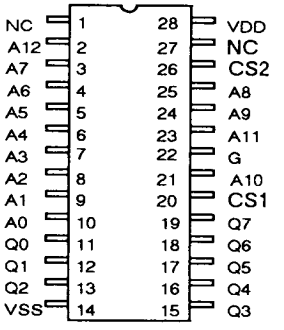


Figure 2. ROM Pinout

DEVICE OPERATION

The UT6764 has three control inputs called Chip Select 1 (CS1), Chip Select 2 (CS2), and output enable (G); thirteen address inputs, A(12:0); and eight data lines, Q(7:0). CS1 and CS2 are device enable inputs that control device selection, active, and standby modes. Asserting both CS1 and CS2 enables the device, causes IDD to rise to its active value, and decodes the thirteen address inputs to select one of 8,192 words in the memory. During a read cycle, G must be asserted to enable the outputs.

Table 1. Operation Truth Table

G	CS1	CS2	I/O Mode	Mode
X(1)	X	negated	3-state	Stand-by
X	negated	X	3-state	Stand-by
negated	asserted	asserted	3-state	Read (2)
asserted	asserted	asserted	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of G, CS1, and CS2 asserted defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

Read Cycle 1, the Address Access read in figure 3a, is initiated by a change in address inputs while the chip is selected with G asserted. Valid data appears on data outputs Q(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as the chip selects and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Figure 3b shows Read Cycle 2, the Chip Select-controlled Access. For this cycle, G remains asserted, and the addresses remain stable for the entire cycle. After the specified t_{STQV} is satisfied, the eight-bit word addressed by A(12:0) is accessed and appears at the data outputs Q(7:0).

Figure 3c shows Read Cycle 3, the Output Enable-controlled Access. For this cycle, CS1 and CS2 are asserted, and the addresses are stable before G is enabled. Read access time is t_{GLQV} unless t_{AVQV} or t_{STQV} have not been satisfied.

CHIP SELECT

User-defined chip select and output enable polarity provides a flexible system interface. Input polarity (i.e. active high vs. active low) is mask defined. Possible combinations include ($\overline{CS1}$, $\overline{CS2}$, $\overline{G}$), ($\overline{CS1}$, $\overline{CS2}$, G), ($\overline{CS1}$, CS2, $\overline{G}$), ($\overline{CS1}$, CS2, G), (CS1, $\overline{CS2}$, $\overline{G}$), (CS1, $\overline{CS2}$, G), (CS1, CS2, $\overline{G}$), (CS1, CS2, G), which correspond to 000, 001, 010, 011, 100, 101, 110, and 111.

RADIATION HARDNESS

The UT6764 ROM incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

Table 2. Radiation Hardness Design Specifications (1)

Total Dose	1.0E6	rads(Si)
Dose Rate Upset	1.0E9	rads(Si)/s 20ns pulse
Dose Rate Survival	1.0E12	rads(Si)/s 20ns pulse
Neutron Fluence	3.0E14	n/cm^2

Notes:
1. The ROM will not latch up during radiation exposure under recommended operating conditions.

ABSOLUTE MAXIMUM RATINGS (1)
(Referenced to VSS)

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 7.0
$V_{I/O}$	Voltage on any pin	-0.5 to V_{DD} +0.5
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1W
T_J	Maximum junction temperature	+175°C
Θ_{JC}	Thermal resistance, junction-to-case	10°C/W
I_{LU}	Latchup immunity (see figure 4b)	+/-150 mA
I_I	DC input current	+/-10 mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	Positive supply voltage	4.5 to 5.5	V
T_C	Case temperature range	-55 to +125	°C
V_{IN}	DC input voltage	0 to V_{DD}	V

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*
(VDD = 5.0V +/-10%; -55°C < TC < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
VIH	High-level input voltage		2.2		V
VIL	Low-level input voltage			0.8	V
VOL	Low-level output voltage	IOL = 8mA, VDD = 4.5V		0.4	V
VOH	High-level output voltage	IOH = -8mA, VDD = 4.5V	2.4		V
CIN	Input capacitance (1)	f = 1MHz @ 0V, VDD = 4.5V		15	pF
CO	Output capacitance (1)	f = 1MHz @ 0V, VDD = 4.5V		20	pF
IIN	Input leakage current	VIN = VDD and VSS	-10	10	uA
IOZ	Three-state output leakage current TTL outputs	VO = VDD and VSS VDD = 5.5V G = 5.5V	-10	10	uA
IOS	Short-circuit output current (2, 3)	VDD = 5.5V, VO = VDD VDD = 5.5V, VO = 0V	 -90	90	mA mA
IDD(OP)	Supply current operating @ f = 1MHz @ f = 14MHz	CMOS inputs (i.e. IOUT = 0) VDD = 5.5V VDD = 5.5V		 40 150	 mA mA
IDD(SB) pre-rad	Supply current standby @ f = 0Hz	CMOS inputs (i.e. IOUT = 0) CS1 = negated VDD = 5.5V CS2 = negated		200	µA
IDD(SB) post-rad	Supply current standby @ f = 0Hz	CMOS inputs (i.e. IOUT = 0) CS1 = negated VDD = 5.5V CS2 = negated		3	mA

Notes:
1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

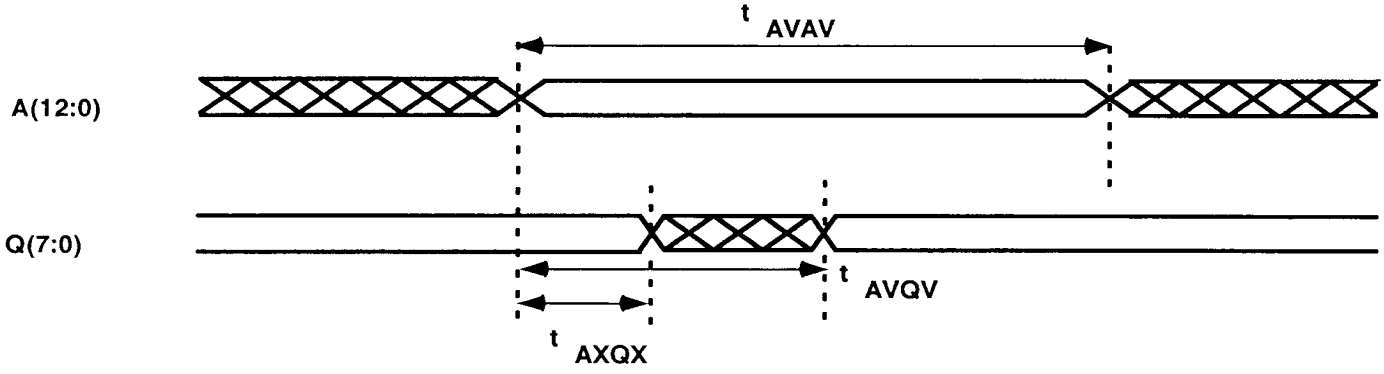
* Post-radiation performance guaranteed at 25°C to meet MIL-STD-883 Method 1019.

AC CHARACTERISTICS READ CYCLE (Pre/Post-Radiation)*
(VDD = 5.0V +/-10%; -55°C < TC < +125°C)

SYMBOL	PARAMETER	6764-70		UNIT
		MIN	MAX	
tAVAV	Read cycle time	70		ns
tAVQV	Read access time		70	ns
tAXQX	Output hold time	5		ns
tGTQX	G-controlled output enable time	0		ns
tGTQV	G-controlled access time (Read Cycle 3)		15	ns
tGFQZ	G-controlled output three-state time		15	ns
tSTQX (1)	Chip Select-controlled output enable time	0		ns
tSTQV (1)	Chip Select-controlled access time		70	ns
tSFQZ (2)	Chip Select-controlled output three-state time		20	ns

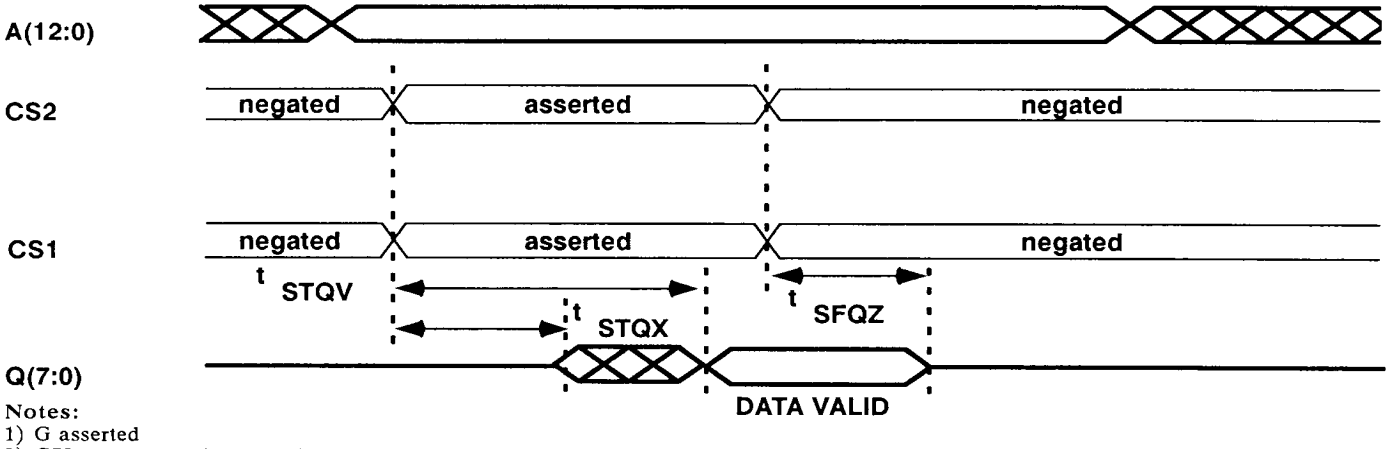
Notes:
1. The ST (select true) notation refers to the active edge of CS2 and CS1, whichever comes last.
2. The SF (select false) notation refers to the negating edge of CS2 and CS1, whichever comes first.

* Post-radiation performance guaranteed at 25°C to meet MIL-STD-883 Method 1019.



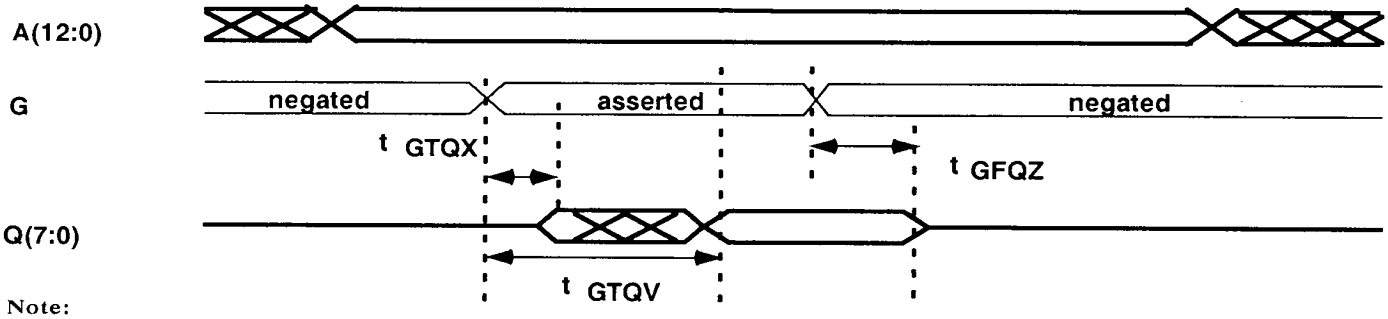
Notes:
1) G asserted
2) CS1 and CS2 asserted

Figure 3a. ROM Read Cycle 1: Address Access



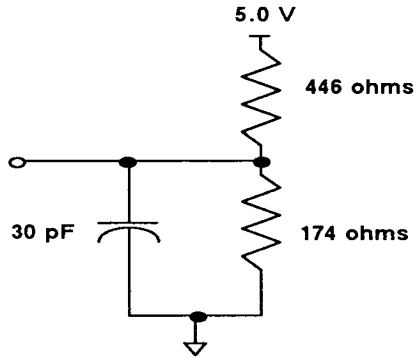
Notes:
1) G asserted
2) CS2 programmed active high
CS1 programmed active low

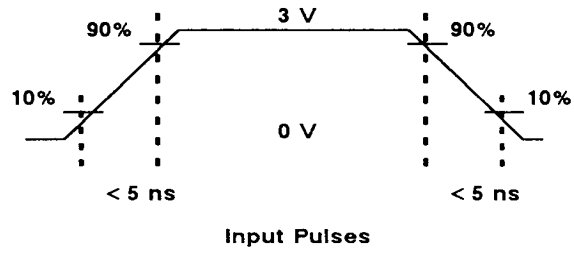
Figure 3b. ROM Read Cycle 2: Chip Select Access



Note:
1)CS1 and CS2 asserted

Figure 3c. ROM Read Cycle 3: Output Enable Access





Notes:
1. 40 pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point. (i.e. 1.4 V)
3. Or equivalent output load circuit.

Figure 4a. AC Test Loads and Input Waveforms

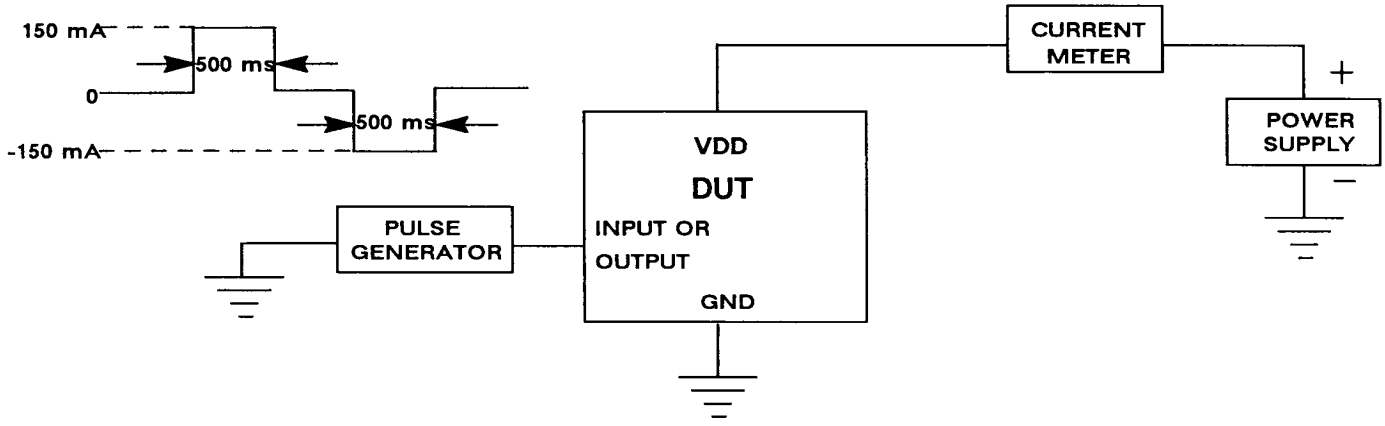
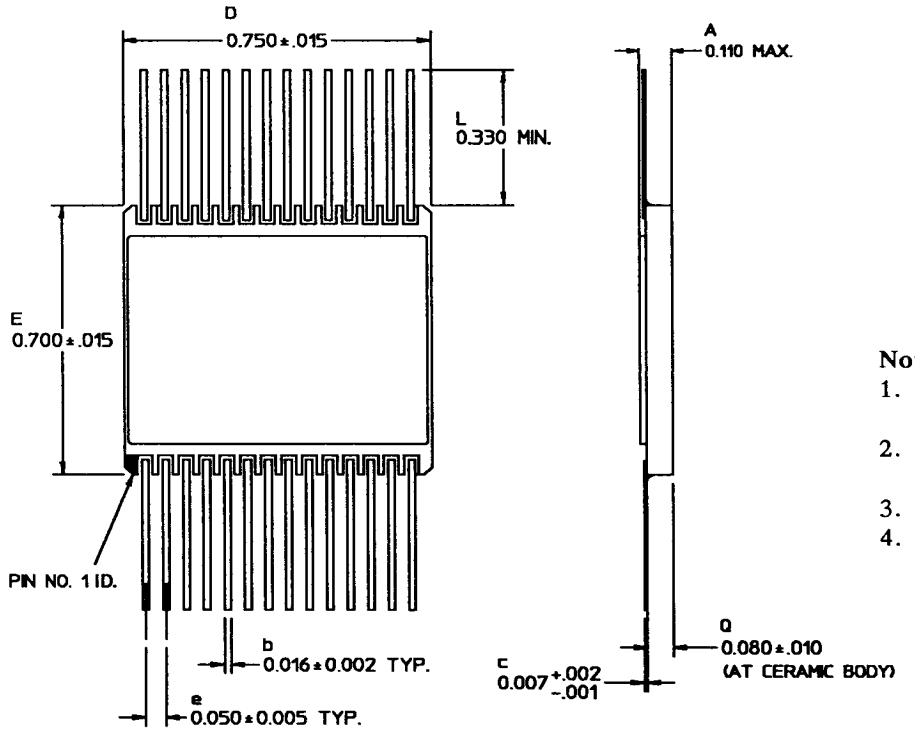


Figure 4b. Latchup Test

LATCHUP TEST CONFIGURATION

Figure 4b shows the latchup test. V_{DD} holds at +5.5 VDC, and V_{SS} holds at ground. The device test is at 125°C. Each type of I/O alternately receives a positive and then negative 150 mA pulse of 500 ms duration. The current is monitored after the pulse for latchup condition. To prevent burnout, the supply current is limited to 400 mA.

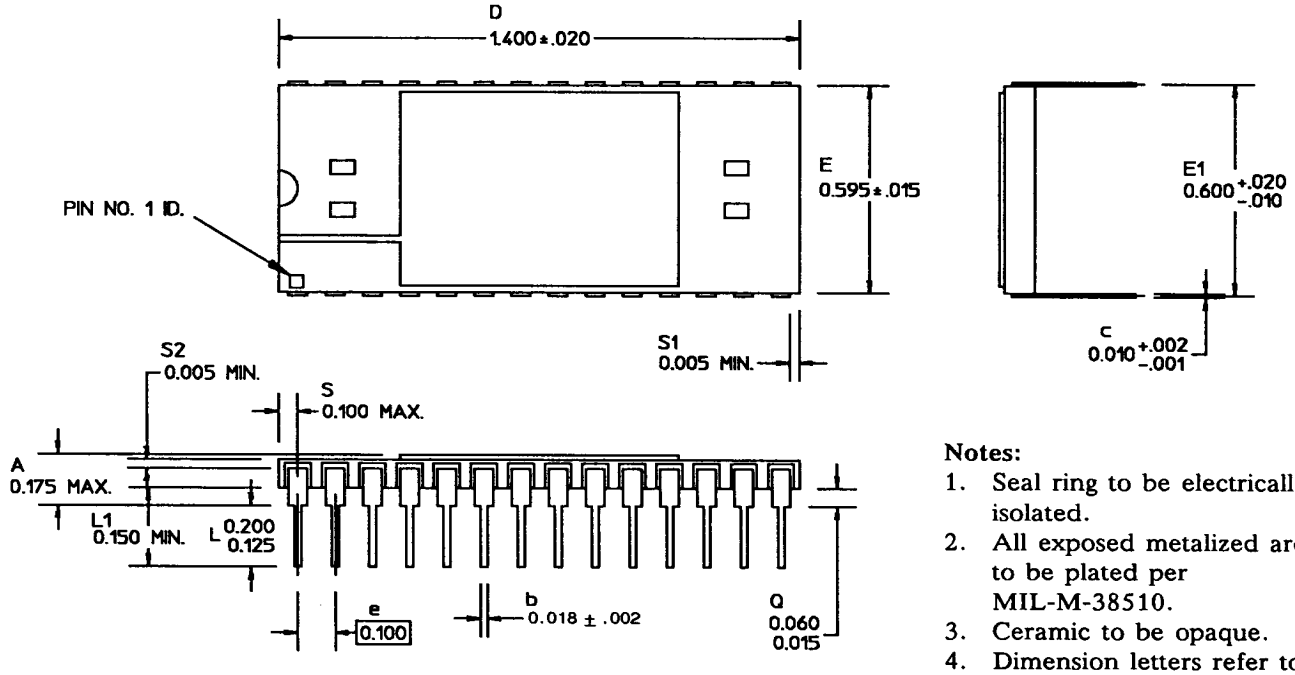
The ROM has latchup immunity in excess of +150 mA for 500 ms.



Notes:

1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-M-38510.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-M-38510.

Figure 5a. 28-pin Ceramic Flatpack



Notes:

1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-M-38510.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-M-38510.

Figure 5b. 28-pin Ceramic DIP Package

ORDERING INFORMATION

To order the UT6764 ROM, use the following part number guide:

UT6764 -- ** * * *

- (R) Radiation-Hardened 1.0 x 10^5 rads(Si)
- (H) Radiation-Hardened 1.0 x 10^6 rads(Si)
- (B) MIL-STD-883C compliant, non-JAN Class B
- (C) Modified high-reliability flow, -55°C to 125°C
- (P) Prototype (radiation performance not guaranteed)
- (S) Screened to MIL-STD-883C Level S requirements per Method 5004 and Group A only of Method 5005
- (P) 28-pin Ceramic Side-Brazed DIP (D-10, Configuration 3, MIL-M-38510, Appendix C)
- (W) 28-pin Ceramic Flatpack .050 center
- (70) 70ns Access Time

UTMC Main Office
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1-800-722-1575

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Laguna Hills, CA 92653
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