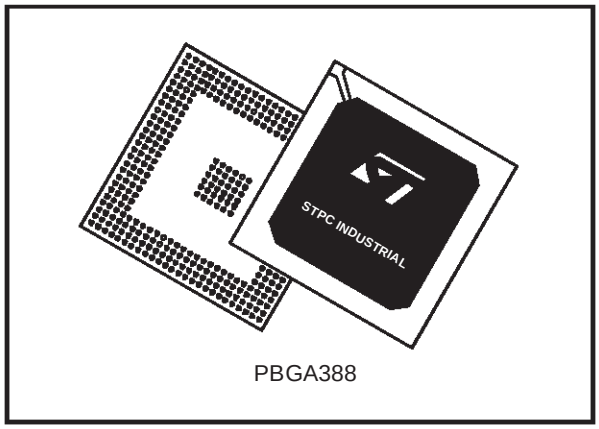
STPC INDUSTRIAL

High Performance Industrial PC on a Chip

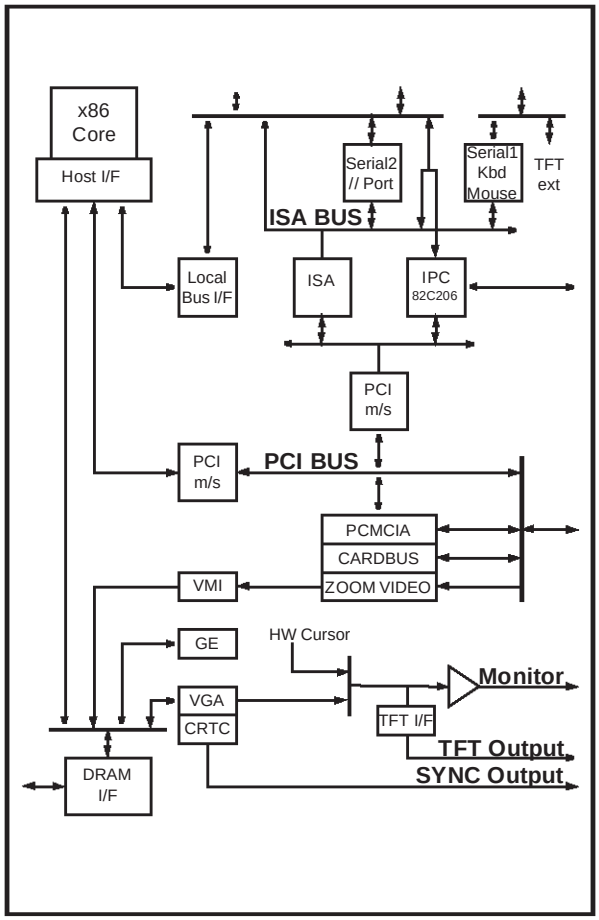
PRODUCT PREVIEW

- POWERFUL X86 PROCESSOR
- 64-BIT 66MHz INTERNAL BUS
- 64-BIT 66MHz DRAM CONTROLLER
- SVGA GRAPHICS CONTROLLER
- CRT CONTROLLER
- 135MHz RAMDAC
- UMA ARCHITECTURE
- ADVANCED GRAPHICS COMPRESSION TECHNIQUE
- TFT DISPLAY CONTROLLER
- PCI MASTER / SLAVE / ARBITER
- CARDBUS / PCMCIA INTERFACE
- PC CARD DMA SUPPORT
- ZOOM VIDEO SUPPORT
- ISA MASTER/SLAVE
- LOCAL BUS INTERFACE
- PC/AT+ KEYBOARD CONTROLLER
- PS/2 MOUSE CONTROLLER
- 2 SERIAL PORTS
- 1 UNIVERSAL PARALLEL PORT
- DMA CONTROLLER
- INTERRUPT CONTROLLER
- TIMER / COUNTERS
- POWER MANAGEMENT



PBGA388

Figure 1. Logic Diagram



DESCRIPTION

The STPC Industrial integrates a fully static x86 processor, fully compatible with standard fifth generation x86 processors, and combines it with powerful chipset, graphics, TFT, PC-Card, Local Bus, keyboard, mouse, serials and parallel interfaces to provide a single Industrial oriented PC compatible subsystem on a single device. The performance of the device is comparable with the performance of a typical P5 generation system. The device is packaged in a 388 Plastic Ball Grid Array (PBGA).

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back capability.
- Parallel processing integral floating point unit, with automatic power down.
- Clock core speeds up to of 133 MHz.
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 3.3V operation.

- **DRAM Controller**
- Integrated system memory and graphic frame memory.
- Supports up to 128-MByte system memory in 4 banks and as little as 2Mbytes.
- Supports 4-MByte, 8-MByte, 16-MByte, and 32-MByte single-sided and double-sided DRAM SIMMs.
- Four quad-word write buffers for CPU to DRAM and PCI to DRAM cycles.
- Four quad-word read prefetch buffers for PCI masters.
- Supports Fast Page Mode & EDO DRAMs.
- Programmable timing for DRAM parameters including CAS pulse width, CAS pre-charge time, and RAS to CAS delay.
- 60, 70, 80 & 100ns DRAM speeds.
- Memory hole between 1 MByte & 8 MByte supported for PCI/ISA busses.
- Hidden refresh.

- **Graphics Controller**
- 64-bit windows accelerator.
- Complete backward compatibility to VGA and SVGA standards.
- Hardware acceleration for text (generalized bit map expansion), bitblts, transparent blts and fills.
- Up to 64 x 64 bit graphics hardware cursor.
- Up to 4MB long linear frame buffer.
- 8, 16, 24 and 32 bit pixels.
- Drivers for Windows and other operating systems.

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- Requires external frequency synthesizer and reference sources.
- 8, 16, 24 and 32-bit pixels.
- Interlaced or non-interlaced output.

- **TFT Interface**
- Programmable panel size up to 1024 by 1024 pixels.
- Support for VGA and SVGA active matrix TFT flat panels with 9, 12, 18-bit interface (1 pixel per clock).
- Support for XGA and SXGA active matrix TFT flat panels with 2 x 9-bit interface (2 pixels per clock).
- Programmable image positionning.
- Programmable blank space insertion in text mode.
- Programmable horizontal and vertical image expansion in graphic mode.
- Two fully programmable PWM (Pulse Width Modulator) signals to adjust the flat panel brightness and contrast.
- Supports **PanelLink**^{TM} high speed serial transmitter externally for high resolution panel interface.

- **Local Bus interface**
- 66MHz, low latency bus.
- Asynchronous / synchronous.
- 22-bit address and 16-bit data busses.
- 2 Programmable Flash EPROM Chip Select.
- 4 Programmable I/O Chip Select.
- Separate memory and I/O address spaces.
- Memory prefetch (improved performances).

- **PCI Controller**
- Fully compliant with PCI Version 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- 0.33X and 0.5X CPU clock PCI clock.

- **PC Card / CardBus interface**
- Support one PCMCIA 2.0 / JEIDA 4.1 68-pin standard PC Card Socket.
- Power Management support.
- Support PCMCIA/ATA specifications.
- Support I/O PC Card with pulse-mode interrupts.
- Provides an ExCA™ implementation to PCMCIA 2.0 / JEIDA 4.1 standards.
- DMA support.
- Supports video part of Zoom Video.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or system clock
- Programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus. NSP compliant.

- **Universal parallel port**
- All IEEE Standard 1284 protocols supported : Compatibility, Nibble, Byte, EPP, and ECP modes.
- 16 bytes FIFO for ECP.

- **Keyboard interface**
- Fully PC/AT+ compatible

- **Mouse interface**
- Fully PS/2 compatible

- **Serial interface**
- 15540 compatible
- Programmable word length, stop bits, parity.
- 16-bit programmable baud rate generator.
- Interrupt generator.
- Loop-back mode.
- 8-bit scratch register.
- Two 16-bit FIFOs.
- Two DMA handshake lines.

- **Integrated Peripheral Controller**
- Two 8237/AT compatible 7-channel DMA controller.
- Two 8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports SMM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel ports.
- Slow system clock down to 8MHz
- Slow Host clock down to 8Hz
- Slow graphic clock down to 8Hz
- Supports APM
- Supports RTC, interrupts and DMAs wake up

ExCA is a trademark of PCMCIA / JEIDA.
PanelLink is a trademark of SiliconImage, Inc

1 GENERAL DESCRIPTION

At the heart of the STPC Industrial is an advanced 64-bit processor block, dubbed the 5ST86. The 5ST86 includes a powerful x86 processor core along with a 64-bit DRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus).

The STPC Industrial has in addition to the 5ST86 a TFT output, a Local Bus interface, PC Card and super I/O features.

The STPC Industrial makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system, and generally much better, due to the higher memory bandwidth allowed by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus.

The 64-bit wide memory array provides the system with 320MB/s peak bandwidth, double that of an equivalent system using 32 bits. This allows for higher resolution screens and greater color depth. The processor bus runs at 66Mhz further increasing “standard” bandwidth by at least a factor of two.

The ‘standard’ PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated together with the x86 processor core; additional functions such as communications ports are accessed by the STPC Industrial via internal ISA bus.

The PCI bus is the main data communication link to the STPC Industrial chip. The STPC Industrial translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports generation of Configuration cycles on the PCI bus. The STPC Industrial, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

Graphics functions are controlled through the on-chip SVGA controller and the monitor display is produced through the 2D graphics display engine. This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations which include hardware acceleration of text, bitblts, transparent blts and fills. The results of these operations change the contents of the on-screen or off-screen frame buffer areas of DRAM memory. The frame buffer can occupy a space up to 4 Mbytes anywhere in the physical main memory.

The graphics resolution supported is a maximum of 1280x1024 in 65536 colours at 75Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate above display resolution.

To generate the TFT output, the STPC Industrial extracts the digital video stream before the RAMDAC and reformats it to the TFT format. The height and width of the flat panel are programmable through configuration registers up to a size of 1024 by 1024.

By default, lower resolution images cover only a part of the larger TFT panel. The STPC Industrial allows to expand the image vertically and horizontally in text mode by inserting programmable blank pixels. It allows to expand the image vertically and horizontally in graphics mode by replicating pixels. The way of replicating J times every K pixel is programmable independently for vertical and horizontal directions.

PanelLink™ is a proprietary interconnect protocol defined by Silicon Image, Inc. It consists of a transmitter that takes parallel video/graphics data from the host LCD graphics controller and transmits it serially at high speed to the receiver which controls the TFT panel. The TFT interface is designed to support connection of its control signal to the **PanelLink**™ transmitter.

The STPC Industrial CARDBUS / PCMCIA controller has been specifically designed to provide the interface with PC-Cards which contain additional memory or I/O and provides an **ExCA**™ implementation to PCMCIA 2.0 / JEIDA 4.1 standards.

The power management control facilities include socket power control, insertion/removal capability, power saving with Windows inactivity, NCS controlled Chip Power Down, together with further controls for 3.3v suspend with Modem Ring Resume Detection.

The need for system configuration jumpers is eliminated by providing address mapping support for PCMCIA 2.0 / JEIDA 4.1 PC-Card memory together with address windowing support for I/O space.

Selectable interrupt steering from PC-Card to internal system bus is also provided.

The STPC Industrial supports the Zoom Video, cost-effective method of accessing live video through a PC Card. A ZV port-compliant PC Card, when inserted into a PC Card slot, is initialized the same way as a PC Card 16. It is then recognized as a ZV port card and programmed accordingly by card services.

The STPC Industrial implements a multi-function parallel port. The standard PC/AT compatible logical address assignments for LPT1, LPT2 and LPT3 are supported.

The parallel port can be configured for any of the following 5 modes and supports the IEEE Standard 1284 parallel interface protocol standards as follow:

-Compatibility Mode (Forward channel, standard)

-Nibble Mode (Reverse channel, PC compatible)

-Byte Mode (Reverse channel, PS/2 compatible)

-EPP Mode (Bi-directional, byte wide)

-ECP Mode (Fast bi-directional, byte wide)

The STPC Industrial BGA package has 388 balls, but this is not sufficient for all the integrated functions, therefore some features are sharing the same balls and can not be used at the same time. The STPC Industrial configuration is done by 'strap options'. It is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the STPC Industrial.

We can distinguish three main blocks ***independently configurables***: The ISA / Local Bus block, the Serial 1 / TFT block, and the PCI / PC Card block.

From the first block, we can activate either the ISA bus and some IPC additionnal features, or the Local bus, the parallel port and the second serial interface.

From the second block, we can activate either the first serial port, or the TFT extension to get from 4 bit per colour to 6 bit per colour.

From the third block, we can activate either the PCI bus, or the PC Card interface (CardBus/ PCMCIA/ZoomVideo).

The STPC Industrial core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit module (PMU) controls the power consumption providing a comprehensive set of features that control the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides following hardware structures to assist the software in managing the power consumption by the system.

- System Activity Detection.

- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power on state.

- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer period of times is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate SMI interrupt to allow the software to bring the system back up to full power on state. The chip-set supports up to three power down states: Doze state, Stand-by state and Suspend mode. These correspond to decreasing levels of power savings.

Power down puts the STPC Industrial into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost..

Figure 2. Interfaces

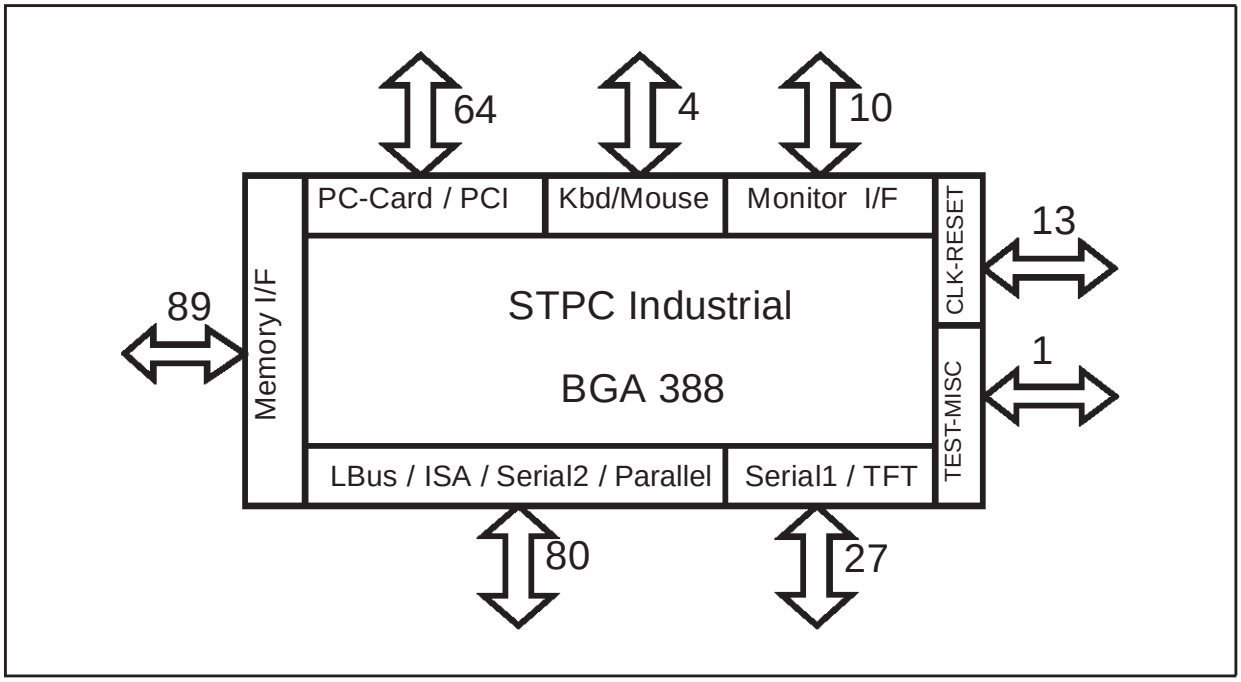


Figure 3. Die Highlight

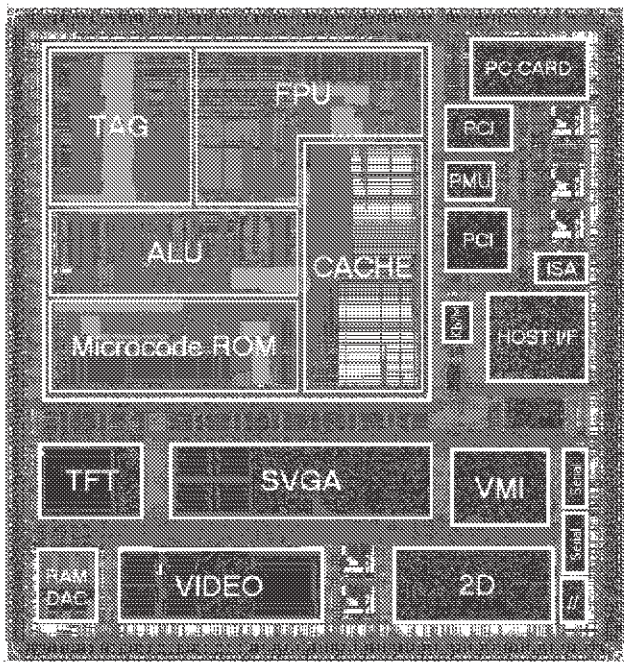


Figure 4. Functionnal description.

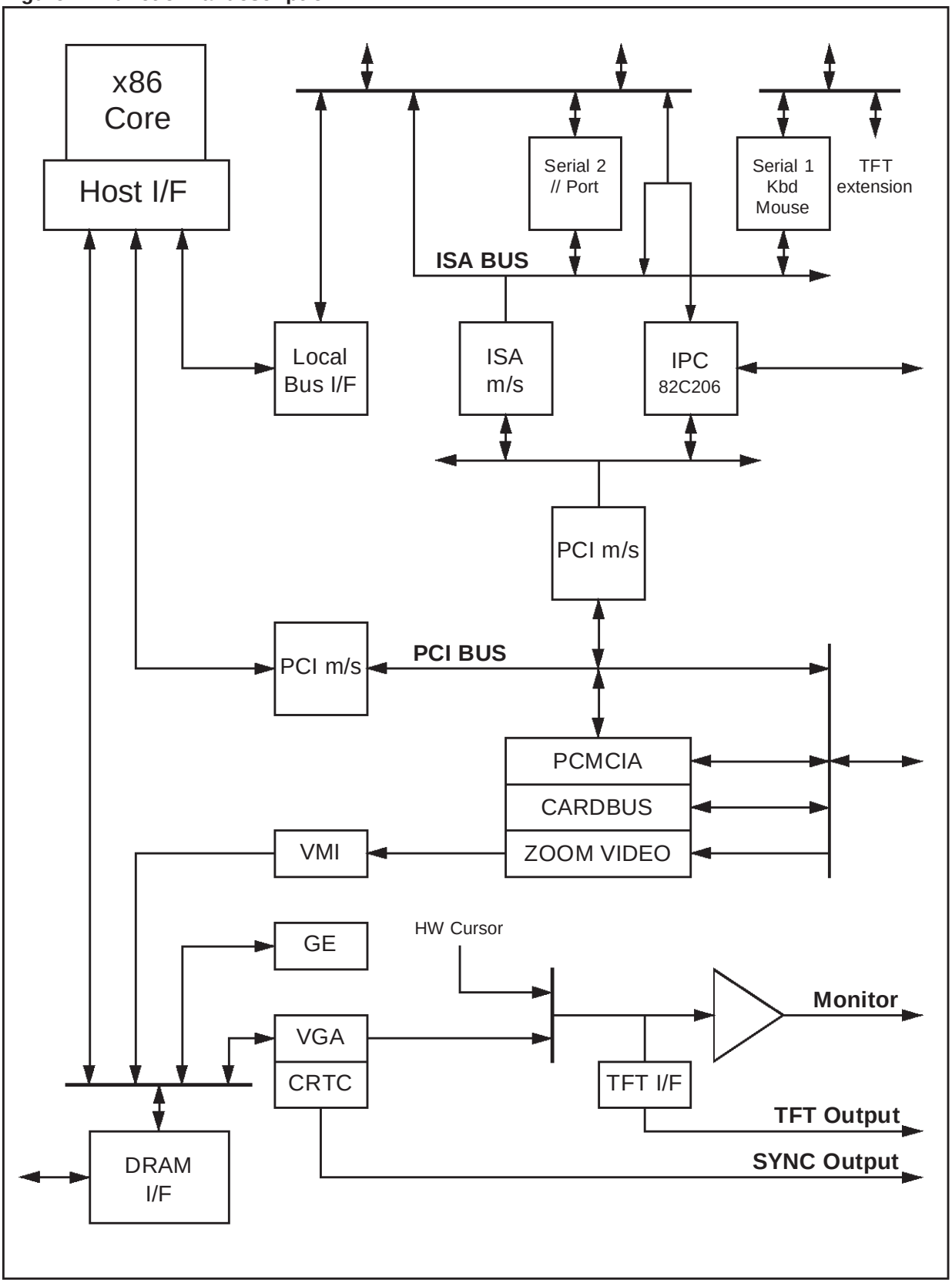


Figure 5. PCI, PCMCIA, CARDBUS, and ZoomVideo modes:

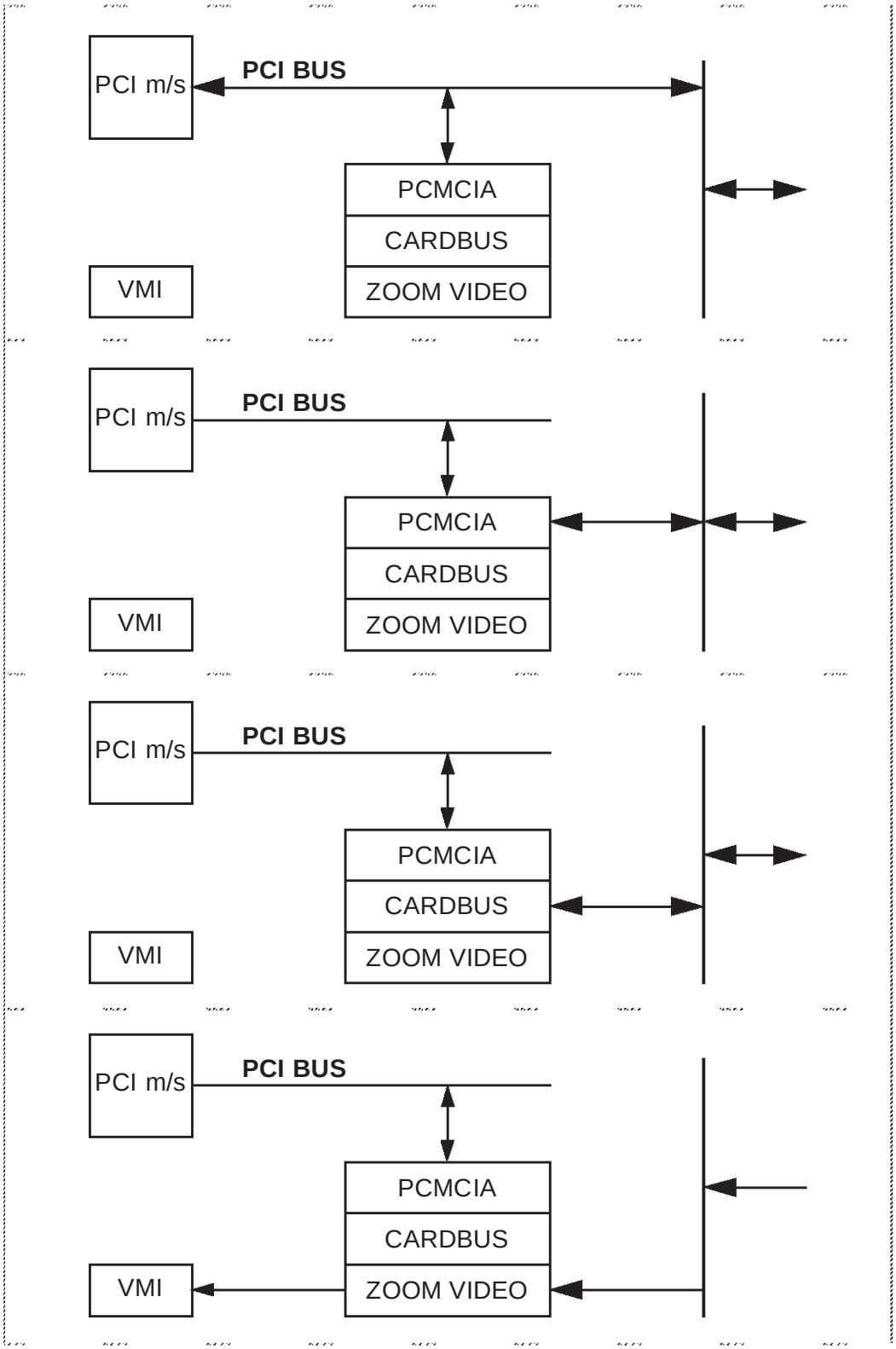


Figure 6. Local Bus and ISA bus modes:

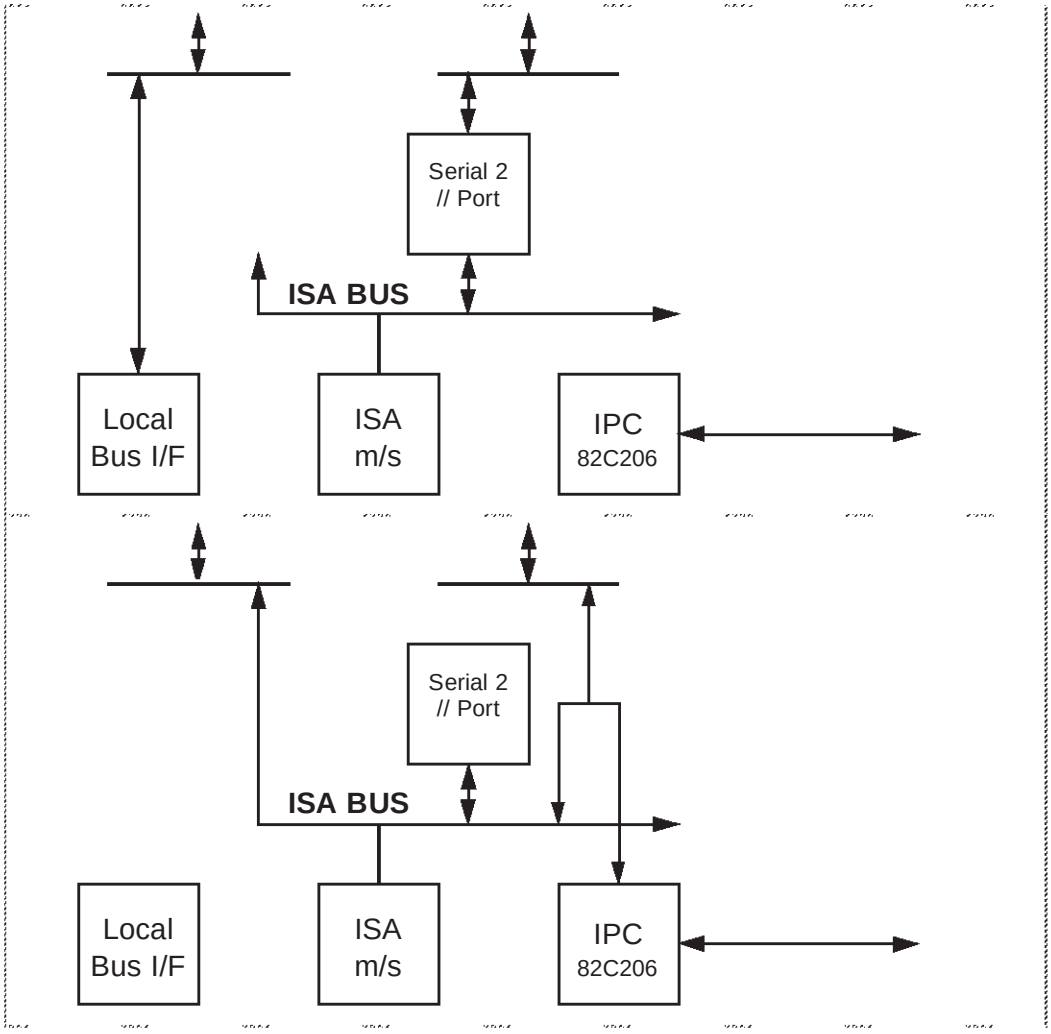


Figure 7. TFT in normal (serial 1 available) and extended modes (serial 1 unavailable)

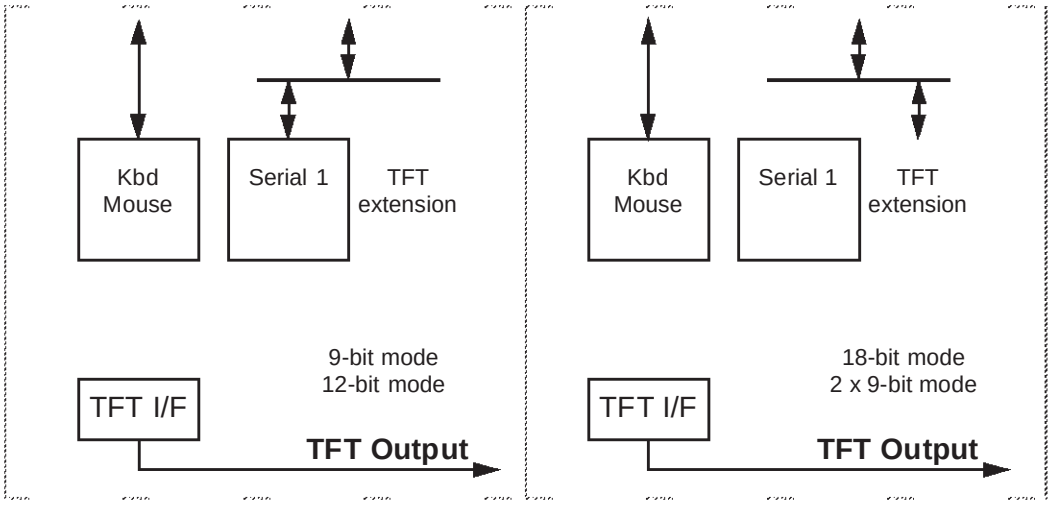


Figure 8. Pictorial Block Diagram

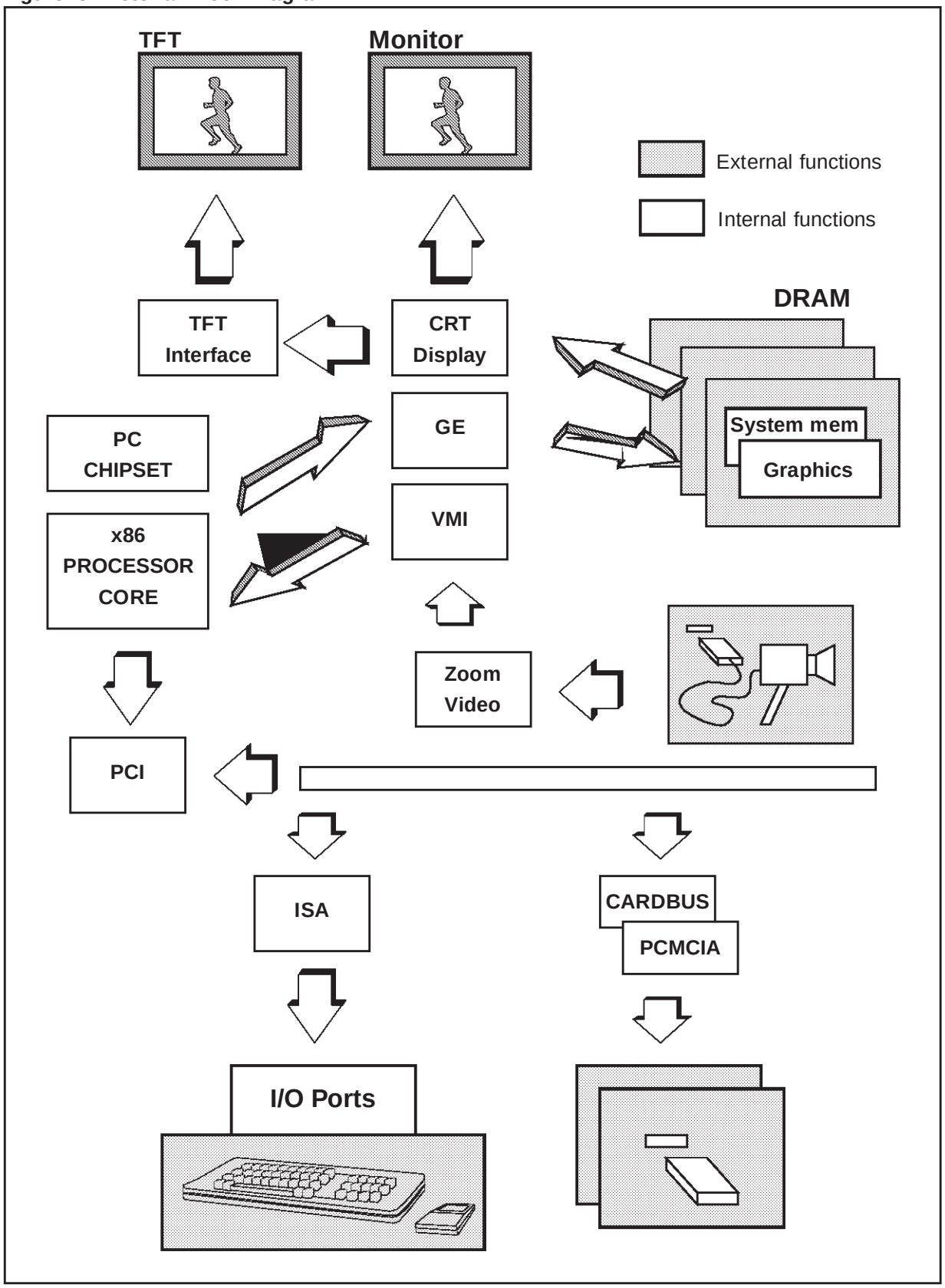


Figure 9. Typical PC oriented Application

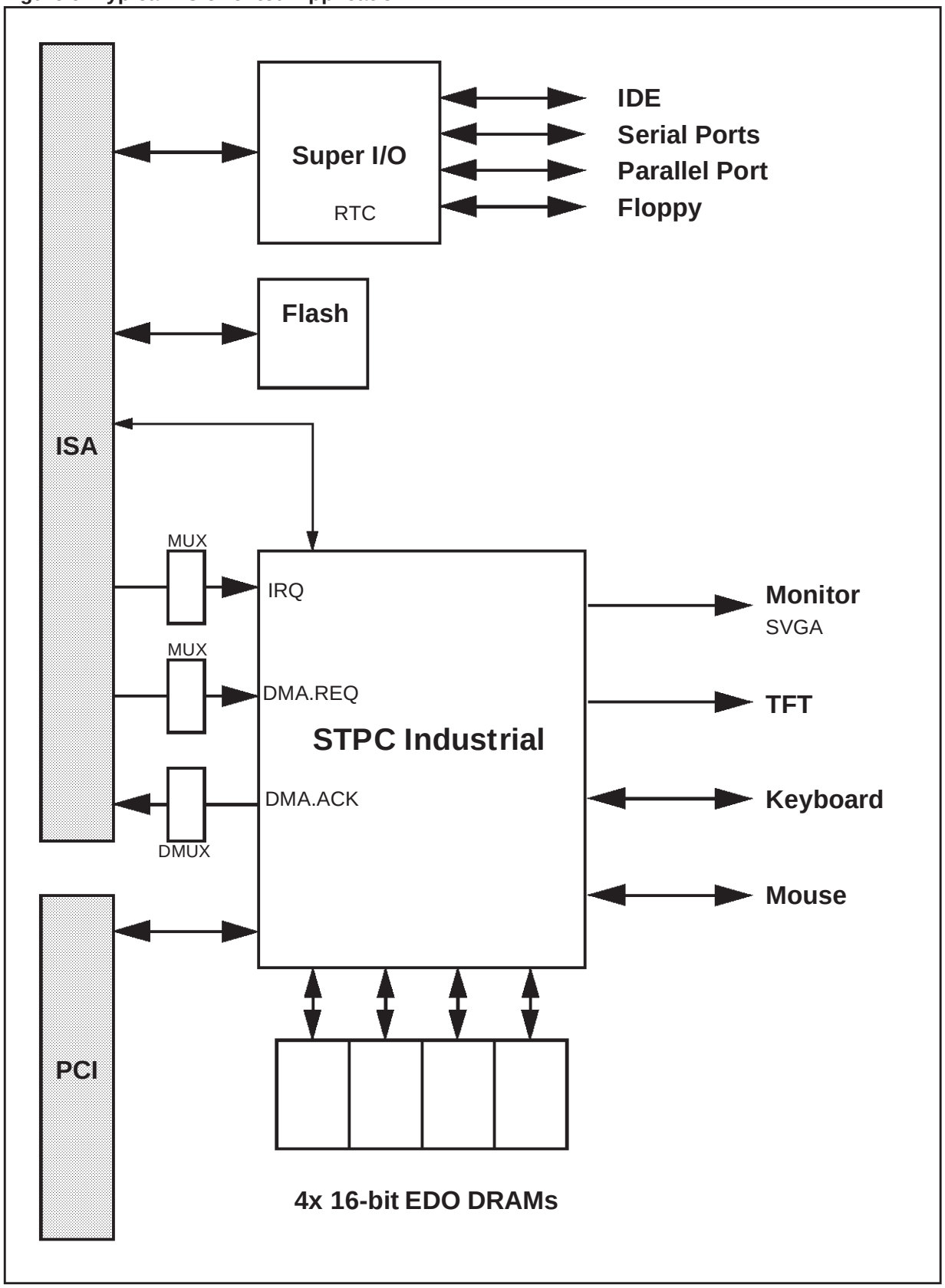
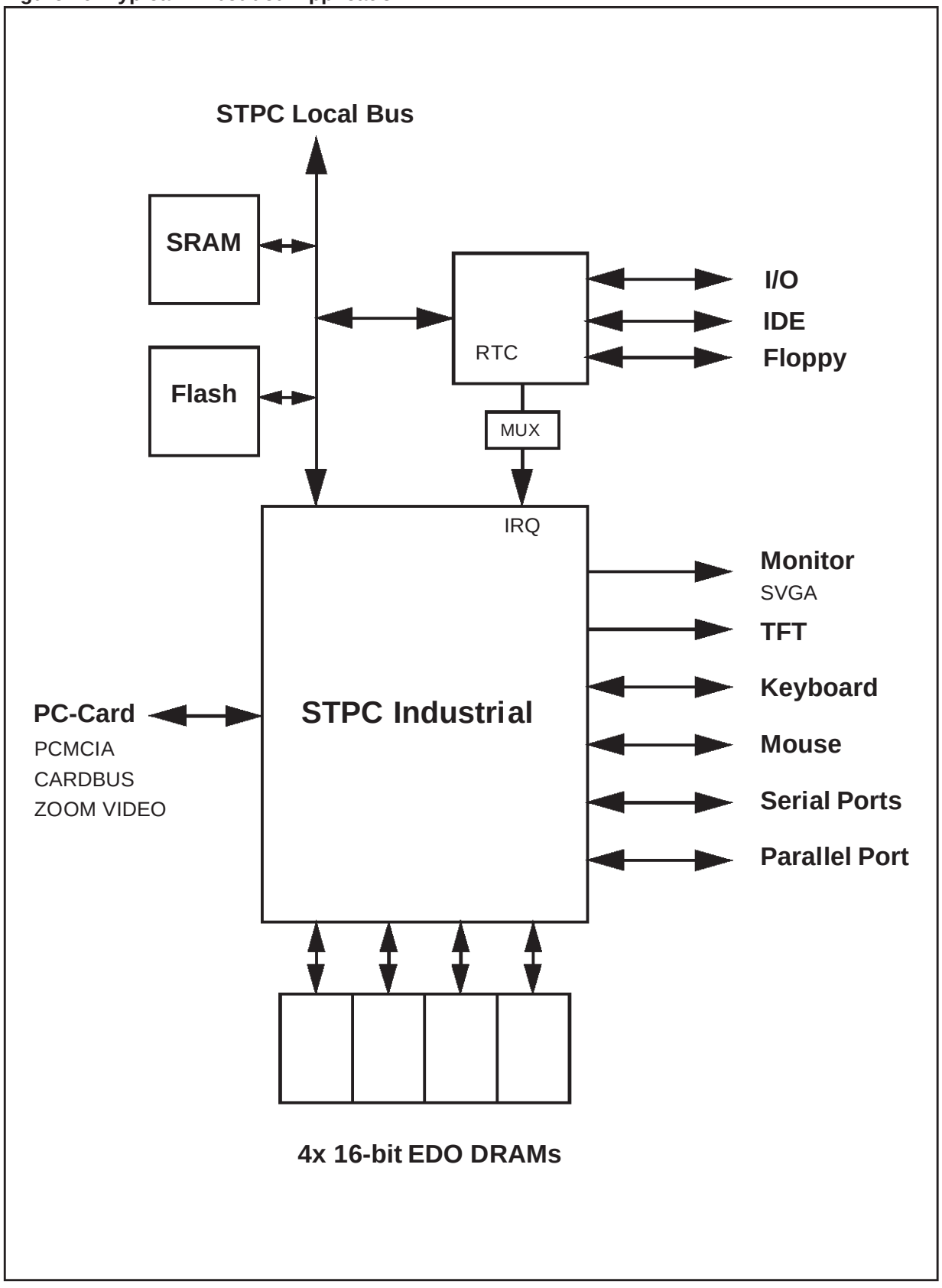


Figure 10. Typical Embedded Application



2 PIN DESCRIPTION

2.1 INTRODUCTION

The STPC Industrial integrates most of the functionalities of the PC architecture. As a result, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Industrial. This offers improved performance due to the tight coupling of the processor core and these peripherals. As a result many of the external pin connections are made directly to the on-chip peripheralfunctions.

Figure 11 shows the STPC Industrial's external interfaces. It defines the main busses and their function. Table 1 describes the physical implementation listing signals type and their functionality. Table 2 provides a full pin listing and description of pins.

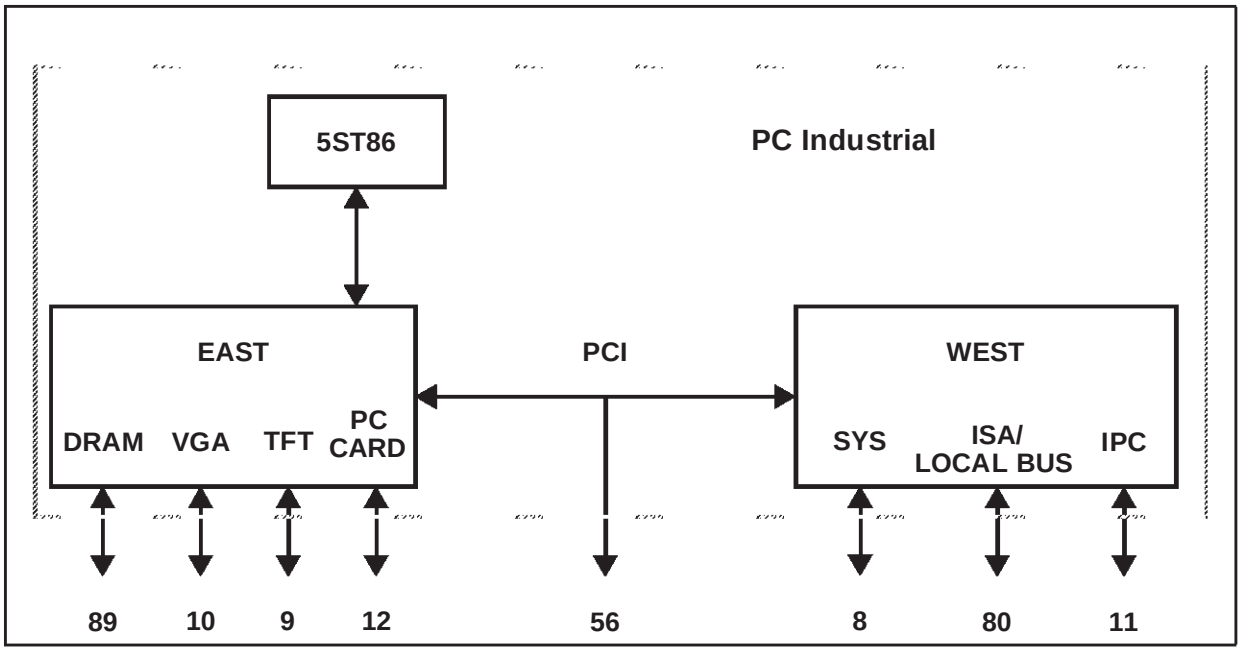
Table 4 provides a full listing of pin locations of the STPC Industrial package by physical connection. Please refer to the pin allocation drawing for reference.

Due to the number of pins available for the package, and the number of functional I/Os, some pins have several functions, selectable by strap option on Reset. Table 3 provides a summary of these pins and their functions.

Table 1. Signal Description

Group name	Qty	
Basic Clocks, Reset & Xtal		13
Memory Interface		89
PCI interface	57	64
PC Card	64	
Keyboard/Mouse		4
Local Bus, Parallel I/F, Serial 2	75	75
ISA/IPC extensions	69	
IPC		5
Serial 1	8	27
TFT output	25	
VGA Monitor interface		10
Grounds		68
V_{DD}		16
Analog specific V_{CC}/V_{DD}		16
Reserved		1
Total Pin Count		388

Figure 11. PC Industrial External Interfaces



PIN DESCRIPTION

Table 2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
BASIC CLOCKS AND RESETS			
PWERGD	I	System Reset / Power good (SYSRSTI#)	1
SYSRSTO#	O	Reset Output to System	1
XTALI	I	14.3MHz Crystal Input	1
XTALO	O	14.3MHz Crystal Output	1
PCI_CLKI	I	33MHz PCI/CardBus Input Clock	1
PCI_CLKO	O	33MHz PCI/CardBus Output Clock	1
ISA_CLK, ISA_CLK2X	O	ISA Clock x1 and x2 (also Multiplexer Select Line For IPC)	2
CLK14M	O	ISA bus synchronisation clock	1
HCLK	I/O	33 / 66MHz Host Clock (Test)	1
DEV_CLK	O	24MHz Peripheral Clock	1
GCLK2X	I/O	80MHz Graphics Clock	1
DCLK	I/O	135MHz Dot Clock	1
MEMORY INTERFACE			
MA[11:0]	I/O	Memory Address	12
RAS#[3:0]	O	Row Address Strobe	4
CAS#[7:0]	O	Column Address Strobe	8
MWEx	O	Write Enable	1
MD[63:0]	I/O	Memory Data	64
LOCAL BUS INTERFACE (COMBINED WITH ISA BUS)			
PA[21:0]	O	Address Bus [21:0]	22
PD[15:0]	I/O	Data Bus [15:0]	16
PRDY#	I	Ready	1
PWR#[0:1]	O	Memory and I/O Write signals	2
PRD#[0:1]	O	Memory and I/O Read signals	2
FCS[1:0], IOCS[3:0]	O	Flash Memory and I/O Chip Select	6
ISA BUS INTERFACE (COMBINED WITH LOCAL BUS AND PARALLEL PORT)			
LA[23:17]	O	Unlatched Address	7
SA[19:0]	O	Latched Address	20
SD[15:0]	I/O	Data Bus	16
IOCHRDY	I	I/O Channel Ready	1
ALE	O	Address Latch Enable	1
BHE#	O	System Bus High Enable	1
MEMR#, MEMW#	I/O	Memory Read & Write	2
SMEMR#, SMEMW#	O	System Memory Read and Write	2
IOR#, IOW#	I/O	I/O Read and Write	2
MASTER#	I	Add On Card Owns Bus	1
MCS16#, IOCS16#	I	Memory Chip Select 16, I/O Chip Select 16	2
REF#	I	Refresh Cycle	1
AEN	O	Address Enable	1
IOCHCK#	I	I/O Channel Check (ISA)	1
RTCRW#	O	RTC Read / Write#	1
RTCDS#	O	RTC Data Strobe	1
RTCAS#	O	RTC Address Strobe	1
RMRTCCS#	O	ROM / RTC Chip Select	1

Table 2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
IPC			
IRQ_MUX[3:0]	I	Multiplexed Interrupt Request	4
SPKRD	O	Speaker Device Output	1
IPC (COMBINED WITH SERIAL INTERFACE)			
DACK_ENC[2:0]	O	DMA Acknowledge	3
DREQ_MUX[1:0]	I	Multiplexed DMA Request	2
TC	O	ISA Terminal Count	1
KEYBOARD & MOUSE INTERFACE			
KBDATA, MDATA	I	Keyboard & Mouse Data Line	2
KBCLK, MCLK	O	Keyboard & Mouse Clock Line	2
SERIAL INTERFACE (SERIAL 1 COMBINED WITH TFT INTERFACE / SERIAL 2 COMBINED WITH IPC)			
SIN1, SIN2	I	Serial Data In (Serial 1, 2)	2
SOUT1, SOUT2	O	Serial Data Out (Serial 1, 2)	2
CTS1, CTS2	I	Clear To Send (Serial 1, 2)	2
RTS1, RTS2	O	Request To Send (Serial 1, 2)	2
DSR1, DSR2	I	Data Set Ready (Serial 1, 2)	2
DTR1, DTR2	O	Data Terminal Ready (Serial 1,2)	2
DCD1, DCD2	I	Data Carrier Detect (Serial 1, 2)	2
RI1, RI2	I	Ring Indicator (Serial 1, 2)	2
PARALLEL PORT (COMBINED WITH ISA BUS AND IPC)			
PE	I	Paper End	1
SELECT	I	SELECT	1
BUSY#	I	BUSY	1
ERROR#	I	ERROR	1
ACK#	I	Acknowledge	1
PDDIR#	O	Parallel Device Direction	1
STROBE#	O	PCS / STROBE#	1
INIT#	O	INIT	1
AUTPFDX#	O	Automatic Line Feed	1
SELCTIN#	O	SELECT IN	1
PPD[7:0]	I/O	Data Bus	8
PCMCIA INTERFACE (COMBINED WITH PCI / CARDBUS / ZOOM VIDEO)			
RESET	O	Reset	1
A[25:0]	O	Address Bus	26
D[15:0]	I/O	Data Bus	16
IORD#, IOWR#	O	I/O Read and Write	2
DREQ# / WP / IOIS16#	I	DMA Request // Write Protect // I/O Size is 16 bit	1
BVD2, BVD1	I	Battery Voltage Detect	2
READY# / IREQ#	I	Busy / Ready# // Interrupt Request	1
WAIT#	I	Wait	1
INPACK#	I	Input Port Acknowledge	1
OE# / TCw	O	Output Enable // DMA Terminal Count	1
WE# / TCr	O	Write Enable // DMA Terminal Count	1
DACK / REG#	O	DMA Acknowledge // Register	1

PIN DESCRIPTION

Table 2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
CD2#, CD1#	I	Card Detect	2
CE2#, CE1#	O	Card Enable	2
VS1#, VS2#	I	Voltage Sense	2
VCC5_EN	O	Power Switch control : 5v power	1
VCC3_EN	O	Power Switch control : 3.3v power	1
VPP_PGM	O	Power Switch control : Program power	1
VPP_VCC	O	Power Switch control : VCC power	1
CARDBUS INTERFACE (COMBINED WITH PCI / PCMCIA / ZOOM VIDEO)			
CCLK	O	Clock	1
CCLKRUN	I/O	Clock	1
CRST#	O	Reset	1
CSTSCHG#	I	System Change	1
CAD[31:0]	I/O	Address / Data	32
CBE[3:0]	I/O	Bus Commands / Byte Enables	4
CFRAME#	I/O	Cycle Frame	1
CTRDY#	I/O	Target Ready	1
CIRDY#	I/O	Initiator Ready	1
CSTOP#	I/O	Stop Transaction	1
CDEVSEL#	I/O	Device Select	1
CPAR	I/O	Parity Signal Transactions	1
CSERR#	I	System Error	1
CPERR#	I/O	Parity Error	1
CBLOCK#	I/O	PCI Lock	1
CCD[2:1]	I	Card Detect	2
CINT#	I	Interrupt Request	1
CREQ#	I	Request	1
CGNT#	O	Grant	1
PCI INTERFACE (COMBINED WITH PCMCIA / CARDBUS / ZOOM VIDEO)			
CLK	O	PCI Clock	1
PCIRST#	I/O	Reset	1
AD[31:0]	I/O	Address / Data	32
BE[3:0]	I/O	Bus Commands / Byte Enables	4
FRAME#	I/O	Cycle Frame	1
TRDY#	I/O	Target Ready	1
IRDY#	I/O	Initiator Ready	1
STOP#	I/O	Stop Transaction	1
DEVSEL#	I/O	Device Select	1
PAR	I/O	Parity Signal Transactions	1
PERR#	O	Parity Error	1
SERR#	O	System Error	1
LOCK#	I	PCI Lock	1
PCI_REQ#[2:0]	I	PCI Request	3
PCI_GNT#[2:0]	O	PCI Grant	3
PCI_INT[3:0]	I	PCI Interrupt Request	4

Table 2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
ZOOM VIDEO INTERFACE (COMBINED WITH PCI / PCMCIA / CARDBUS)			
PCLK	I/O	Pixel Clock	1
Y[7:0], UV[7:0]	I/O	YUV Data	16
HREF	I/O	Horizontal Reference	1
VSYNC	I/O	Vertical Synchronisation	1
MONITOR INTERFACE			
RED, GREEN, BLUE	O	Red, Green, Blue	3
VSYNC	I/O	Vertical Sync	1
HSYNC	I/O	Horizontal Sync	1
VREF_DAC	I	DAC Voltage reference	1
RSET	I	Resistor Set	1
COMP	I	Compensation	1
DDC[1:0]	I/O	Display Data Channel Serial Link	2
TFT INTERFACE (COMBINED WITH SERIAL 1)			
R[5:0], G[5:0], B[5:0]	O	Red, Green, Blue	18
DCLKOUT	O	Dot clock for flat panel	1
FPLINE	O	Horizontal Sync	1
FPFRAME	O	Vertical Sync	1
DE	O	Data Enable	1
ENAVDD	O	Enable Vdd of flat panel	1
ENVCC	O	Enable Vcc of flat panel	1
PWM	O	PWM back-light control	1
MISCELLANEOUS			
SCAN_ENABLE	I	Test Pin - Reserved	1

2.2 SIGNAL DESCRIPTIONS

2.2.1 BASIC CLOCKS AND RESETS

PWERGD *System Reset/Power good.* This input is low when the the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. PWGD is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of PWGD.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3MHz Crystal Input*
XTALO *14.3MHz Crystal Output.* These pins are the 14.318 MHz crystal input; This clock is used as the reference clock for the internal frequency synthesizer to generate the HCLK and CLK24M.
A 14.3xxx MHz Series Cut Quartz Crystal should be connected between these two pins. Balance capacitors of xx pF should also be added. In the event of an external oscillator providing the master clock signal to the STPC Industrial device, the TTL signal should be provided on XTALO.

PCI_CLKI *33MHz PCI Input Clock*

This signal is treated as a low true clock enable for all PCI bus signals as well as internal registers which operate in the PCI clock domain.

PCI_CLKO *33MHz PCI Output Clock.* This is the master PCI bus clock output

ISA_CLK *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces the Clock signal for the ISA bus. It is also used with ISA_CLK2X as the multiplexor control lines for the Interrupt Controller Interrupt input lines. This is divided down version of the PCICLK or OSC14M.

ISA_CLKX2 *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces a signal at twice the frequency of the Clock signal for the ISA bus. It is also used with ISA_CLK as the multiplexor control lines for the Interrupt Controller Interrupt input lines.

CLK14M *ISA bus synchronisation clock.* This is the buffered 14.318 Mhz clock to the ISA bus. This clock also provides the reference clock to the frequency synthesizer that generates GCLK2X and DCLK.

HCLK *33/66MHz Host Clock.* This is the host 1X clock. Its frequency can vary from 50 to 75 MHz. All host transactions and PCI transactions are synchronized to this clock. The DRAM controller to execute the host transactions is also driven by this clock.

DEV_CLK *24MHz Peripheral Clock (floppy drive).* This 24MHZ signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip.

GCLK2X *80MHz Graphics Clock.* This is the Graphics 2X clock, which drives the graphics engine and the the DRAM controller to execute the graphics and display cycles.
Normally GCLK2X is generated by the internal frequency synthesizer, and this pin is an output. By setting a bit in Strap Register 2, this pin can be made an input so that an external clock can replace the internal frequency synthesizer.

DCLK *135MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can be as high as 135 MHz, and it is required to have a worst case duty cycle of 60-40.

2.2.2 MEMORY INTERFACE

MA[11:0] *Memory Address.* These 12 multiplexed memory address pins support external DRAM with up to 4K refresh. These include all 16M x N and some 4M x N DRAM modules. The address signals must be externally buffered to support more than 16 DRAM chips. The timing of these signals can be adjusted by software to match the timings of most DRAM modules.

MD[63:0] *Memory Data.* This is the 64-bit memory data bus. If only half of a bank is populated, MD63-32 is pulled high, data is on MD31-0.
MD20-0 are also used as inputs at the rising edge of PWGD to latch in power-up configuration information into the ADPC strap registers.

RAS#[3:0] *Row Address Strobe.* There are 4 active low row address strobe outputs, one each for each bank of the memory. Each bank contains 4 or 8-bytes of data. The memory controller allows half of a bank (4-bytes) to be populated to enable memory upgrade at finer granularity.
The RAS# signals drive the SIMMs directly without any external buffering. These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the RAS# signals at the pins.

CAS#[7:0] *Column Address Strobe.* There are 8 active low column address strobe outputs, one each for each byte of the memory.
The CAS# signals drive the SIMMs either directly or through external buffers.
These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the CAS# signals at the pins.

MWE# *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L). This single write enable controls all DRAMs. It can be externally buffered to boost the maximum number of loads (DRAM chips) supported.
The MWE# signals drive the SIMMs directly without any external buffering.

2.2.3 LOCAL BUS INTERFACE (Combined with ISA Bus)

PA[21:0] *Memory Address.* This is the 22-bit Local Bus Address

PD[15:0] *Data Bus.* This is the 16-bit bidirectional Local Bus Data bus.

PRDY# *Ready.* This input signals the Local Bus Ready state.

PWR#1, PWR#0 *Memory and I/O Write signals.*

PRD#1, PRD#0 *Memory and I/O Read signals.*

FCS[1:0], IOCS[3:0] *Flash Memory and I/O Chip select.*

2.2.4 ISA BUS INTERFACE

LA[23:17] *Unlatched Address.* These pins ISA Bus unlatched address bits 23-17 on 16-bit devices. When ISA bus is accessed by any cycle initiated from the PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are tristated.

SA[19:0] *Unlatched Address.* These are the 20 low bits of the system address bus of ISA. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus (ISA).* These pins are the external databus to the ISA bus.

IOCHRDY *IO Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Industrial. The STPC Industrial monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh.
ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Industrial since the access to the system memory can be considerably delayed due to CRT refresh or a write back cycle.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Industrial to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Industrial.
ALE is driven low after reset.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Industrial generates SMEMR# signal of the ISA bus only when the address is below one megabyte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Industrial generates SMEMW# signal of the ISA bus only when the address is below one megabyte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Industrial ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Industrial does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Industrial is executed as an extended 8-bit IO cycle.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Industrial performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Industrial performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

RTCRW# *Real Time Clock RW#.* This pin is used as RTCRW#. This signal is asserted for any I/O write to port 71H.

RTCDS# *Real Time Clock DS.* This pin is used as RTCDS. This signal is asserted for any I/O read to port 71H.

RTCAS *Real time clock address strobe.* This signal is asserted for any I/O write to port 70H.

RMRTCCS# *ROM/Real Time clock chip select.* This pin is a multi-function pin. This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During a IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR# or IOW# signals to properly access the real time clock.

2.2.5 IPC

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They are to be encoded before connection to the STPC Industrial using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the IRQ# pin of the RTC.

SPKRD *Speaker Drive.* This the output to the speaker and is AND of the counter 2 output with bit 1 of Port 61, and drives an external speaker driver. This output should be connected to 7407 type high voltage driver.

2.2.6 IPC
(Combined with Serial Interface)

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Industrial before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Industrial using ISACLK and ISACLKX2 as the input selection strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the byte count expires.

2.2.7 KEYBOARD/MOUSE INTERFACE

KBCLK, *Keyboard Clock line.* Keyboard data is latched by the controller on each negative clock edge produced on this pin. The keyboard can be disabled by pulling this pin low by software control.

KBDATA, *Keyboard Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to KBCLK.

MCLK, *Mouse Clock line.* Mouse data is latched by the controller on each negative clock edge produced on this pin. The mouse can be disabled by pulling this pin low by software control.

MDATA, *Mouse Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to MCLK.

2.2.8 SERIAL INTERFACE
(Serial 1 combined with TFT Interface)
(Serial 2 combined with IPC)

SIN1, SIN2 *Input Serial input.* Data is clocked in using RCLK/16.

SOUT1, SOUT2 *Output Serial Output.* Data is clocked out using TCLK/16 (TCLK=BAUD#).

DCD1#, DCD1# *Input Data carrier detect.*

RI1#, RI2# *Input Ring indicator.*

DSR1#, DSR2# *Input Data set ready.*

CTS1#, CTS2# *Input Clear to send.*

RTS1#, RTS2# *Output Request to send.*

DTR1#, DTR2# *Output Data terminal read.*

2.2.9 PARALLEL PORT
(Combined with ISA Bus an IPC)

PE *Paper End.* Input status signal from printer.

SLCT *Printer Select.* Printer selected input.

BUSY *Printer Busy.* Input status signal from printer.

ERR# *Error.* Input status signal from printer.

ACK# *Acknowledge.* Input status signal from printer.

PPDIR# *Parallel Device Direction.* Bidirectional control line output.

STROBE# *PCS/Strobe#.* Data transfer strobe line to printer.

INIT# *Initialize Printer.* This output sends an initialize command to the connected printer.

AUTPFDX# *Automatic Line feed.* This output sends a command to the connected printer to automatically generate line feed on received carriage returns.

SLCTIN# *Select In.* Printer select output.

PPD[7-0] *Printer Data Lines* Data transfer lines to printer. Bidirectional depending on modes.

2.2.10 PCMCIA INTERFACE (Combined with PCI / Cardbus /ZV)

RESET *Card Reset.* This output forces a hard reset to a PC Card.

CA[25-0] *Card Address*. Used with the lower 11 bits of the ISA Address Bus to generate the Card Address.

IORD# *I/O Read.* This output is used with REG# to gate I/O read data from the PC Card, (only when REG# is asserted).

IOWR# *I/O Write*. This output is used with REG# to gate I/O write data from the PC Card, (only when REG# is asserted).

WP *Write Protect.* This input indicates the status of the Write Protect switch (if fitted) on memory PC Cards (asserted when switch set to write protect).

BVD1, BVD2 *Battery Voltage Detect.* These inputs will be generated by memory PC Cards that include batteries and are an indication of the condition of the batteries. BVD1 and BVD2 are kept asserted high when the battery is in good condition.

RDY/BSY# *Ready/busy.* This input is driven low by memory PC Cards to signal that their circuits are busy processing a previous write command.

WAIT# *Bus Cycle Wait.* This input is driven by the PC Card to delay completion of the memory or I/O cycle in progress.

OE# *Output Enable.* OE# is an active low output which is driven to the PC Card to gate Memory Read data from memory PC Cards.

WE#/PRGM# *Write Enable.* This output is used by the host for gating Memory Write data. WE# is also used for memory PC Cards that have programmable memory.

REG# *Attribute Memory Select.* This output is inactive (high) for all normal accesses to the Main Memory of the PC Card. I/O PC Cards will only respond to IORD# or IOWR# when REG# is active (low).

CD#1, CD#2 *Card Detect.* These inputs provide for the detection of correct card insertion. CD#1 and CD#2 are positioned at opposite ends of the connector to assist in the detection process. These inputs are internally grounded on the PC Card therefore they will be forced low whenever a card is inserted in a socket.

CE#1, CE#2 *Card Enable*. These are active low output signals provided from the PCIC. CE#1 enables even bytes, CE#2 odd bytes.

ENABLE# *Enable.* This output is used to activate/ select a PC Card socket. ENABLE# controls the external address buffer logic.C card has been detected (CD#1 and CD#2 = '0').

ENIF# *ENIF*. This output is used to activate/select a PC Card socket.

EXT_DIR *EXternal Transreceiver Direction Control.* This output is high during a read and low during a write. The default power up condition is write (low). Used for both Low and High Bytes of the Data Bus.

VCC_EN#, VPP1_EN0, VPP1_EN1, V 2_EN0, VPP2_EN1 *Power Control.* Five output signals used to control voltages (VPP1, VPP2 and VCC) to a PC Card socket.

GPI# *General Purpose Input.*

2.2.11 CARDBUS INTERFACE (Combined with PCI / PCMCIA / ZV)

Please refer to the documention by Mindshare and Intel.

2.2.12 PCI INTERFACE

PCIRST# *PCI Bus Reset.*

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

BE[3:0]# *Bus Commands/Byte Enables.* These are the multiplexed command and byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the byte enable information. These pins are inputs when a PCI master other than the STPC Industrial owns the bus and outputs when the STPC Industrial owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Industrial owns the PCI bus.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Industrial is the target of the current bus transaction. It is used as an input when STPC Industrial initiates a cycle on the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Industrial initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Industrial to determine when the current PCI master is ready to complete the current transaction.

STOP# *Stop Transaction.* Stop is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Industrial and is used as an output when a PCI master cycle is targeted to the STPC Industrial.

DEVSEL# *I/O Device Select.* This signal is used as an input when the STPC Industrial initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Industrial is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE[3:0]#, and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

PERR# *Parity Error.*

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Industrial initiated PCI transaction. Its assertion by either the STPC Industrial or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

PCI_REQ#[2:0] *PCI Request.* This pin are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

PCI_GNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCI_REQ#.

PCI_INT[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals. They are to be encoded before connection to the STPC Industrial using ISACLK and ISACLKX2 as the input selection strobes.

2.2.13 ZOOM VIDEO INTERFACE (Combined with PCI/PCMCIA/Cardbus)

PCLK *Pixel Clock.* Video Data Pixel synchronization clock.

Y[7:0], UV[7:0] *YUV Video Data.*

HREF *Horizontal Reference.* Horizontal synch timing strobe.

VSYNC *Vertical Reference.* Vertical synch timing strobe.

2.2.14 MONITOR INTERFACE

RED, GREEN, BLUE *RGB Video Outputs.* These are the 3 analog color outputs from the RAMDACs

VSYNC *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

HSYNC *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

VREF_DAC *DAC Voltage reference.* Normally, the internal voltage reference is used as an input to the internal RAMDAC. In this case the VREF pin is an output driven by the internal voltage reference. A mode exists whereby the internal voltage reference is disabled and this pin becomes an input driving the digital to analog converters. This allows an external voltage reference source to be used.

RSET *Resistor Current Set.* This is reference current input to the RAMDAC is used to set the full-scale output of the RAMDAC.

COMP *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and V_{DD} to damp oscillations.

DDC[1:0] *Direct Data Channel Serial Link.* These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I^2C electrical specifications, they have open-collector output drivers which are internally connected to V_{DD} through pull-up resistors.

2.2.15 FLAT PANEL INTERFACE SIGNALS (Combined with Serial 1)

DCLKOUT, *Dot Clock for Flat panel Output.*
FPFRAME, *Vertical Sync. pulse Output.*
FPLINE, *Horizontal Sync. Pulse Output.*
DE, *Data Enable.*
R5-0, *Red Output.*
G5-0, *Green Output.*
B5-0, *Blue Output.*
ENAVDD *Enable VDD of Flat Panel.*
ENVCC *Enable VCC of Flat Panel.*
PWM *PWM Back-Light Control.*

2.2.16 MISCELLANEOUS

SCAN_ENABLE *Reserved.* This pin is reserved for Test and Miscellaneous functions)

Table 3. Signals sharing the same pin

ISA BUS / IPC	LOCAL BUS	PARALLEL PORT	SERIAL INTERFACE
LA[23:22]	FCS#[0], PRD#[1]		
LA[21:20]	PA[21:20]		
LA[19:17]	PRD#[0], PWR#[1:0]		
SA[19:1]	PA[19:1]		
SA[0]	PRDY#		
SD[15:0]	PD[15:0]		
BHE#	FCS#[1]		
MEMR#, MEMW#	IOCS[3:2]		
SMEMR#, SMEMW#	IOCS[1:0]		
GPIO#		PE	
IOCHRDY		SELECT	
IOR#		BUSY#	
IOW#		ERROR#	
MASTER#		ACK#	
MCS16#		PDDIR	
IOCS16#		INIT#	
REF#		AUTPFDX#	
AEN		SELCTIN#	
IOCHCK#		PPD[7]	
ISAOE#		PPD[6]	
RTCRW#		PPD[5]	
RTCDS#		PPD[4]	
RTCAS#		PPD[3]	
RMRTCCS#		PPD[2]	
ALE		PPD[1]	
DACK_ENC[0:2]			DCD2, DSR2, SIN2
DREQ_MUX[0:1]			CTS2, RTS2
TC			SOUT2

TFT INTERFACE	SERIAL 1
B[0,1]	DCD1, CTS1
G[0,1]	DSR1, RTS1
R[0,1]	SIN1, SOUT1

PCI	CARDBUS	PCMCIA	ZOOM VIDEO
CLK	CCLK	A[16]	UV[2]
PCIRST#	CRST#	RESET	
AD[31:27]	CAD[31:27]	D[10,9,1,8,0]	

AD[26:20]	CAD[26:20]	A[0:6]	
AD[19]	CAD[19]	A[25]	UV[7]
AD[18]	CAD[18]	A[7]	
AD[17]	CAD[17]	A[24]	UV[5]
AD[16]	CAD[16]	A[17]	Y[1]
AD[15]	CAD[15]	IOWR#	
AD[14]	CAD[14]	A[9]	Y[0]
AD[13]	CAD[13]	IORD#	
AD[12]	CAD[12]	A[11]	VSYNC
AD[11]	CAD[11]	OE# / TCw	
AD[10]	CAD[10]	CE[2]	
AD[9]	CAD[9]	A[10]	HREF
AD[8:0]	CAD[8:0]	D[15,7,13,6,12,5,11,4,3]	
BE[3]	CBE[3]	DACK/REG#	
BE[2]	CBE[2]	A[12]	UV[6]
BE[1]	CBE[1]	A[8]	Y[2]
BE[0]	CBE[0]	CE[1]	
FRAME#	CFRAME#	A[23]	UV[3]
TRDY#	CTRDY#	A[22]	UV[1]
IRDY#	CIRDY#	A[15]	UV[4]
STOP#	CSTOP#	A[20]	Y[7]
DEVSEL#	CDEVSEL#	A[21]	UV[0]
PAR	CPAR	A[13]	Y[4]
PERR#	CPERR#	A[14]	Y[6]
SERR#	CSERR#	WAIT	
LOCK#	CBLOCK#	A[19]	Y[5]
PCIREQ#[2]	CREQ#	INPACK#	
PCIREQ#[1]	CCD1	CD1#	
PCIREQ#[0]	CSTSCHG#	BVD1	
PCIGNT#[2]	CGNT#	WE# / TCr	
PCIGNT#[1]	CCD2	CD2#	
PCIGNT#[0]		BVD2	
PCI_INT[3]		VCC3_EN	
PCI_INT[2]		VCC5_EN	
PCI_INT[1]		VPP_PGM	
PCI_INT[0]	CINT#	READY#	
	CLKRUN	DREQ# / WP / IOIS16#	PCLK
		A[18]	Y[3]

Table 4. Pinout.

Pin #	Pin name
C4	PWERGD
A3	SYSRSETO#
AB25	XTALI
AB23	XTALO
G25	PCI_CLKI
H23	PCI_CLKO
B20	ISA_CLK
A20	ISA_CLK2X
AC26	CLK14M
H26	HCLK
J26	DEV_CLK
AC15	GCLK2X
AD16	DCLK
AE13	MA[0]
AC12	MA[1]
AF13	MA[2]
AD12	MA[3]
AE14	MA[4]
AC14	MA[5]
AF14	MA[6]
AD13	MA[7]
AE15	MA[8]
AD14	MA[9]
AF15	MA[10]
AE16	MA[11]
AD15	RAS#[0]
AF16	RAS#[1]
AC17	RAS#[2]
AE18	RAS#[3]
AD17	CAS#[0]
AF18	CAS#[1]
AE19	CAS#[2]
AF19	CAS#[3]
AD18	CAS#[4]
AE20	CAS#[5]
AC19	CAS#[6]
AF20	CAS#[7]
AD19	MWE#
AE21	MD[0]
AC20	MD[1]
AF21	MD[2]
AD20	MD[3]

Pin #	Pin name
AE22	MD[4]
AF22	MD[5]
AD21	MD[6]
AE23	MD[7]
AC22	MD[8]
AF23	MD[9]
AD22	MD[10]
AE24	MD[11]
AD23	MD[12]
AF24	MD[13]
AE26	MD[14]
AD25	MD[15]
AD26	MD[16]
AC25	MD[17]
AC24	MD[18]
AB24	MD[19]
AB26	MD[20]
AA25	MD[21]
Y23	MD[22]
AA24	MD[23]
AA26	MD[24]
Y25	MD[25]
Y26	MD[26]
Y24	MD[27]
W25	MD[28]
V23	MD[29]
W26	MD[30]
W24	MD[31]
V25	MD[32]
V26	MD[33]
U25	MD[34]
V24	MD[35]
U26	MD[36]
U23	MD[37]
T25	MD[38]
U24	MD[39]
T26	MD[40]
R25	MD[41]
R26	MD[42]
T24	MD[43]
P25	MD[44]
R23	MD[45]
P26	MD[46]
R24	MD[47]

Pin #	Pin name
N25	MD[48]
N23	MD[49]
N26	MD[50]
P24	MD[51]
M25	MD[52]
N24	MD[53]
M26	MD[54]
L25	MD[55]
M24	MD[56]
L26	MD[57]
M23	MD[58]
K25	MD[59]
L24	MD[60]
K26	MD[61]
K23	MD[62]
J25	MD[63]
B1	PA[0]
P1	LA[17] / PWR#[0]
N3	LA[18] / PWR#[1]
R2	LA[19] / PRD#[0]
C1	LA[20] / PA[20]
C2	LA[21] / PA[21]
P3	LA[22] / PRD#[1]
R1	LA[23] / FCS#[0]
P4	SA[0] / PRDY#
J2	SA[1] / PA[1]
H3	SA[2] / PA[2]
H1	SA[3] / PA[3]
J4	SA[4] / PA[4]
H2	SA[5] / PA[5]
G3	SA[6] / PA[6]
G1	SA[7] / PA[7]
G2	SA[8] / PA[8]
F1	SA[9] / PA[9]
F3	SA[10] / PA[10]
G4	SA[11] / PA[11]
F2	SA[12] / PA[12]
E1	SA[13] / PA[13]
E3	SA[14] / PA[14]
E4	SA[15] / PA[15]
E2	SA[16] / PA[16]
D1	SA[17] / PA[17]

PIN DESCRIPTION

Pin #	Pin name
D3	SA[18] / PA[18]
D2	SA[19] / PA[19]
P2	SD[0] / PD[0]
M3	SD[1] / PD[1]
N1	SD[2] / PD[2]
M4	SD[3] / PD[3]
N2	SD[4] / PD[4]
L3	SD[5] / PD[5]
M1	SD[6] / PD[6]
M2	SD[7] / PD[7]
L1	SD[8] / PD[8]
K3	SD[9] / PD[9]
L2	SD[10] / PD[10]
K4	SD[11] / PD[11]
K1	SD[12] / PD[12]
J3	SD[13] / PD[13]
K2	SD[14] / PD[14]
J1	SD[15] / PD[15]
T2	BHE# / FCS#[1]
R3	MEMR# / IOCS#[3]
T1	MEMW# / IOCS#[2]
R4	SMEMR# / IOCS#[1]
U2	SMEMW# / IOCS#[0]
AB2	IOCHRDY / SELECT
AB1	IOR# / BUSY#
Y3	GPIO# / PE
AA3	IOW# / ERROR#
AC2	MASTER# / ACK#
AB4	MCS16# / PDDIR
AB3	IOCS16# / INIT#
AD2	REF# / AUTPFDX#
AC3	AEN / SELCTIN#
E25	IOCHCK# / PPD[7]
E26	ISAOE# / PPD[6]
F24	RTCRW# / PPD[5]
D25	RTCDS# / PPD[4]
E23	RTCAS# / PPD[3]
D26	RMRTCCS# / PPD[2]
E24	ALE / PPD[1]
C25	PPD[0]
AC1	STROBE#
D5	IRQ_MUX[0]
A4	IRQ_MUX[1]

Pin #	Pin name
C5	IRQ_MUX[2]
B3	IRQ_MUX[3]
AD1	SPKRD
V3	DACK_ENC[0] / DCD2
Y2	DACK_ENC[1] / DSR2
W4	DACK_ENC[2] / SIN2
Y1	DREQ_MUX[0] / CTS2
W3	DREQ_MUX[1] / RTS2
AA2	TC / SOUT2
Y4	DTR2
AA1	RI2
U4	SIN1 / R[0]
V1	SOUT1 / R[1]
V2	CTS1 / B[1]
U3	RTS1 / G[1]
U1	DSR1 / G[0]
W2	DTR1
T3	DCD1 / B[0]
W1	RI1
F25	KBCLK
F26	KBDATA
G24	MCLK
G23	MDATA
D18	RESET
C18	A[0]
A17	A[1]
D17	A[2]
B16	A[3]
C17	A[4]
A16	A[5]
B15	A[6]
A15	A[7]
C16	A[8]
B14	A[9]
D15	A[10]
A14	A[11]
C15	A[12]
B13	A[13]
D13	A[14]
A13	A[15]
C14	A[16]

Pin #	Pin name
B12	A[17]
C13	A[18]
A12	A[19]
B11	A[20]
A11	A[21]
D12	A[22]
B10	A[23]
C11	A[24]
A10	A[25]
D10	D[0]
B9	D[1]
C10	D[2]
A9	D[3]
B8	D[4]
C9	D[5]
B7	D[6]
D8	D[7]
A7	D[8]
B6	D[9]
D7	D[10]
A6	D[11]
C7	D[12]
A5	D[13]
C6	D[14]
B4	D[15]
B22	IORD#
D22	IOWR#
D24	WP
A18	BVD1
C26	BVD2
A21	READY#
C19	WAIT#
A25	INPACK#
C22	OE#
B18	WE#
B19	REG#
B24	CD1#
A24	CD2#
B23	CE1#
C23	CE2#
C20	VS1#
A19	VS2#
D20	VCC5_EN
C21	VCC3_EN

Pin #	Pin name
B21	VPP_PGM
A22	VPP_VCC
AD4	RED
AF4	GREEN
AE5	BLUE
AF3	VSYNC
AE4	HSYNC
AF5	VREF_DAC
AE6	RSET
AF6	COMP
AE3	DDC[1]
AF2	DDC[0]
AE7	B[2]
AF7	G[2]
AD7	R[2]
AE8	B[3]
AC9	G[3]
AF8	R[3]
AD8	B[4]
AE9	G[4]
AF9	R[4]
AE10	B[5]
AD9	G[5]
AF10	R[5]
AC10	DCLKOUT
AD10	FPLINE
AE11	FPFRAME
AF11	DE
AE12	ENAVDD
AF12	ENVCC
AD11	PWM
C8	SCAN_ENABLE
AD5	VDD_DAC1
AC5	VDD_DAC2
AE17	VDD_GCLK_PLL
AF17	VDD_DCLK_PLL
K24	VDD_ZCLK_PLL
H25	VDD_DEVCLK_PLL
J24	VDD_HCLK_PLL

Pin #	Pin name
A8	VDD5
A23	VDD5
B5	VDD5
B17	VDD5
C12	VDD5
D6	VDD
D11	VDD
D16	VDD
D21	VDD
F4	VDD
F23	VDD
L4	VDD
L23	VDD
T4	VDD
T23	VDD
AA4	VDD
AA23	VDD
AC6	VDD
AC11	VDD
AC16	VDD
AC21	VDD
AC7	VSS_DAC1
AD6	VSS_DAC2
G26	VSS_DLL
H24	VSS_DLL
A1	VSS
A2	VSS
A26	VSS
B2	VSS
B25	VSS
B26	VSS
C3	VSS
C24	VSS
D4	VSS
D9	VSS
D14	VSS
D19	VSS
D23	VSS
H4	VSS
J23	VSS
L11:16	VSS
M11:16	VSS
N4	VSS

Pin #	Pin name
N11:16	VSS
P11:16	VSS
P23	VSS
R11:16	VSS
T11:16	VSS
V4	VSS
W23	VSS
AC4	VSS
AC8	VSS
AC13	VSS
AC18	VSS
AC23	VSS
AD3	VSS
AD24	VSS
AE1	VSS
AE2	VSS
AE25	VSS
AF1	VSS
AF25	VSS
AF26	VSS

3 ELECTRICAL SPECIFICATIONS

3.1 Introduction

The electrical specifications in this chapter are valid for the STPC Industrial.

3.2 Electrical Connections

3.2.1 Power/Ground Connections/Decoupling

Due to the high frequency of operation of the STPC Industrial, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the STPC Industrial and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

3.2.2 Unused Input Pins

All inputs not used by the designer and not listed in the table of pin connections in Chapter 3 should be connected either to VDD or to VSS. Connect active-high inputs to VDD through a 20 kΩW (±10%) pull-down resistor and active-low inputs to VSS and connect active-low inputs to VCC through a 20 kΩW (±10%) pull-up resistor to prevent spurious operation.

3.2.3 Reserved Designated Pins

Pins designated reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

3.3 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the STPC Industrial device. Stresses beyond those listed under Table 5 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section ”Operating Conditions”.

Exposure to conditions beyond Table 5 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 5) may also result in reduced useful life and reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DDx}	DC Supply Voltage	-0.3, 4.0	V
V_I, V_O	Digital Input and Output Voltage	-0.3, VDD + 0.3	V
T_{STG}	Storage Temperature	-40, +150	°C
T_{OPER}	Operating Temperature	0, +70	°C
P_{TOT}	Total Power Dissipation	4.8	W

3.4 DC Characteristics

Table 6. DC Characteristics

Recommended Operating conditions : VDD = 3.3V±0.3V, Tcase = 0 to 100°C unless otherwise specified

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
P_{DD}	Supply Power	V_{DD} = 3.3V, H_{CLK} = 66Mhz		3.2	3.9	W
H_{CLK}	Internal Clock	(Note 1)			75	Mhz
V_{REF}	DAC Voltage Reference		1.215	1.235	1.255	V
V_{OL}	Output Low Voltage	I_{Load} =1.5 to 8mA depending of the pin			0.5	V
V_{OH}	Output High Voltage	I_{Load} =-0.5 to -8mA depending of the pin	2.4			V
V_{IL}	Input Low Voltage	Except XTALI	-0.3		0.8	V
		XTALI	-0.3		0.9	V
V_{IH}	Input High Voltage	Except XTALI	2.1		V_{DD}+0.3	V
		XTALI	2.35		V_{DD}+0.3	V
I_{LK}	Input Leakage Current	Input, I/O	-5		5	µA
C_{IN}	Input Capacitance	(Note 2)				pF
C_{OUT}	Output Capacitance	(Note 2)				pF
C_{CLK}	Clock Capacitance	(Note 2)				pF

Notes:

1. MHz ratings refer to CPU clock frequency.
2. Not 100% tested.

3.5 AC Characteristics

Table 8 through Table 11 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 12 and Figure 13. The rising clock edge reference level VREF , and other reference levels are shown in Table 7 below for the STPC Industrial. Input or output signals must cross these levels during testing.

Figure 12 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 7. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	3.0	V
V_{ILD}	0.0	V

Note: Refer to Figure 12.

Figure 12. Drive Level and Measurement Points for Switching Characteristics

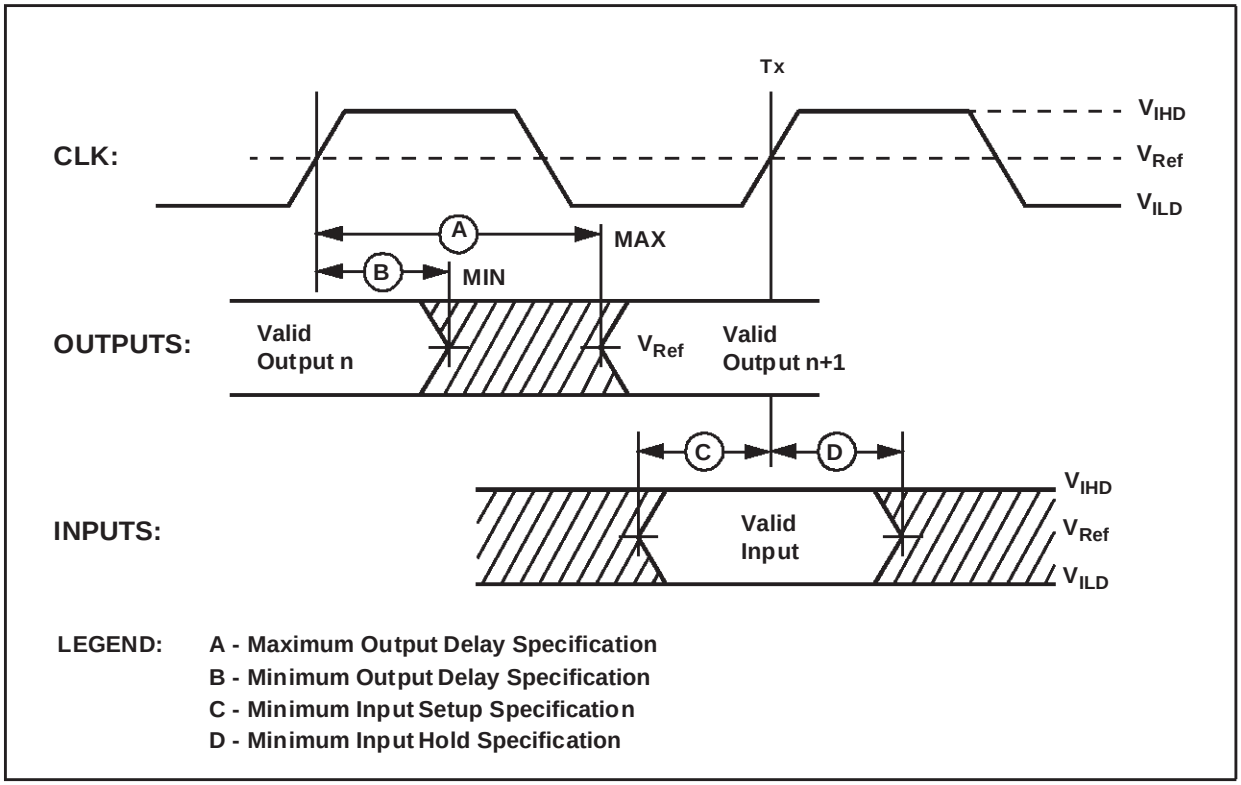


Figure 13. CLK Timing Measurement Points

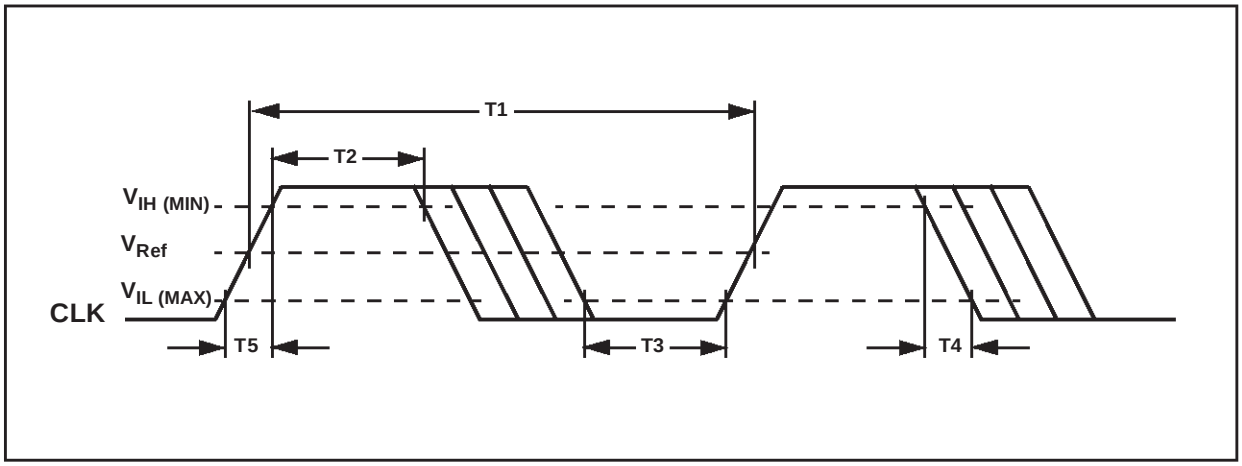


Table 8. PCI Bus AC Timing

Name	Parameter	Min	Max	Unit
t1	PCI_CLKI to AD[31:0] valid	2	11	ns
t2	PCI_CLKI to FRAME# valid	2	11	ns
t3	PCI_CLKI to CBE#[3:0] valid	2	11	ns
t4	PCI_CLKI to PAR valid	2	11	ns
t5	PCI_CLKI to TRDY# valid	2	11	ns
T6	PCI_CLKI to IRDY# valid	2	11	ns
T7	PCI_CLKI to STOP# valid	2	11	ns
T8	PCI_CLKI to DEVSEL# valid	2	11	ns
T9	PCI_CLKI to PCI_GNT# valid	2	12	ns
t10	AD[31:0] bus setup to PCI_CLKI	7		ns
t11	AD[31:0] bus hold from PCI_CLKI	0		ns
t12	PCI_REQ#[2:0] setup to PCI_CLKI	10		ns
t13	PCI_REQ#[2:0] hold from PCI_CLKI	0		ns
t14	CBE#[3:0] setup to PCI_CLKI	7		ns
t15	CBE#[3:0] hold to PCI_CLKI	0		ns
t16	IRDY# setup to PCI_CLKI	7		ns
t17	IRDY# hold to PCI_CLKI	0		ns
t18	FRAME# setup to PCI_CLKI	7		ns
t19	FRAME# hold from PCI_CLKI	0		ns

Table 9. DRAM Bus AC Timing

Name	Parameter	Min	Max	Unit
t22	HCLK to RAS#[3:0] valid		15	ns
t23	HCLK to CAS#[7:0] bus valid		15	ns
t24	HCLK to MA[11:0] bus valid		15	ns
t25	HCLK to MWE# valid		15	ns
t26	HCLK to MD[63:0] bus valid		19	ns
t27	MD[63:0] Generic setup			ns
t28	GCLK2X to RAS#[3:0] valid		15	ns
t29	GCLK2X to CAS#[7:0] valid		15	ns
t30	GCLK2X to MA[11:0] bus valid		15	ns
t31	GCLK2X to MWE# valid		15	ns
t32	GCLK2X to MD[63:0] bus valid		18	ns
t33	MD[63:0] Generic hold			ns

Table 10. Graphics Adapter (VGA) AC Timing

Name	Parameter	Min	Max	Unit
t43	DCLK to VSYNC valid		45	ns
t44	DCLK to HSYNC valid		45	ns

Table 11. ISA Bus AC Timing

Name	Parameter	Min	Max	Unit
t45	XTALO to LA[23:17] bus active		60	ns
t46	XTALO to SA[19:0] bus active		60	ns
t47	XTALO to BHE# valid		62	ns
t48	XTALO to SD[15:0] bus active		35	ns
t49	PCI_CLKI to ISAOE# valid		28	ns
t50	XTALO to GPIOCS# valid		60	ns
t51	XTALO to ALE valid		62	ns
t52	XTALO to MEMW# valid		50	ns
t53	XTALO to MEMR# valid		50	ns
t54	XTALO to SMEMW# valid		50	ns
t55	XTALO to SMEMR# valid		50	ns
t56	XTALO to IOR# valid		50	ns
t57	XTALO to IOW# valid		50	ns

4 MECHANICAL DATA

4.1 388-Pin Package

The pin numbering for the STPC 388-pin Plastic BGA package is shown in Figure 14.

Dimensions are shown in Figure 15, Table 12 and Figure 16, Table 13.

Figure 14. 388-Pin PBGA Package - Top View

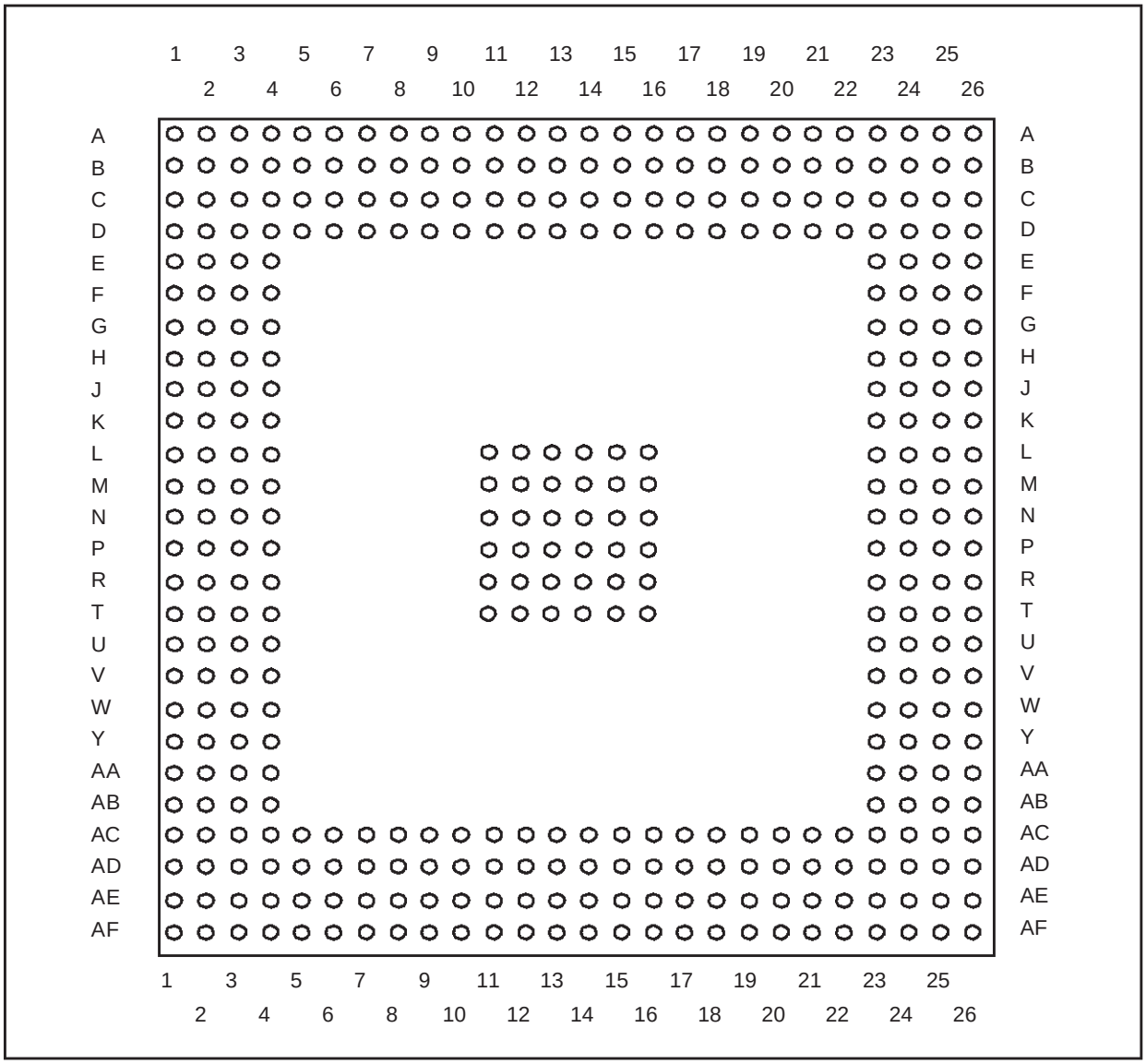


Figure 15. 388-Pin PBGA Package - Dimensions

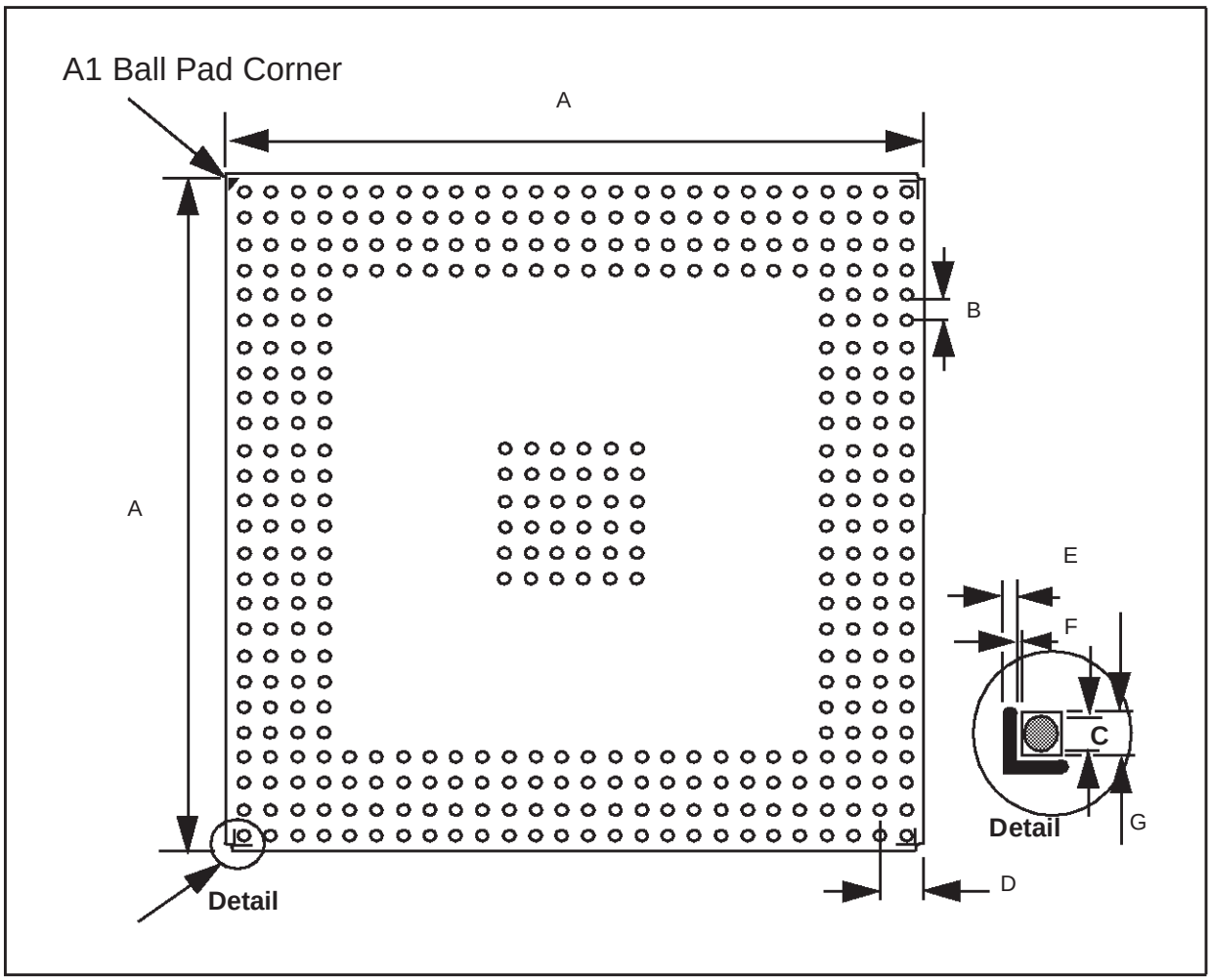


Table 12. PBGA388 - 388 Solder Ball Plastic 35mm x 35mm

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	34.95	35.00	35.05	1.375	1.378	1.380
B	1.22	1.27	1.32	0.048	0.050	0.052
C	0.58	0.63	0.68	0.023	0.025	0.027
D	1.57	1.62	1.67	0.062	0.064	0.066
E	0.15	0.20	0.25	0.006	0.008	0.001
F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 16. 388-Pin PBGA Package - Dimensions (Continued)

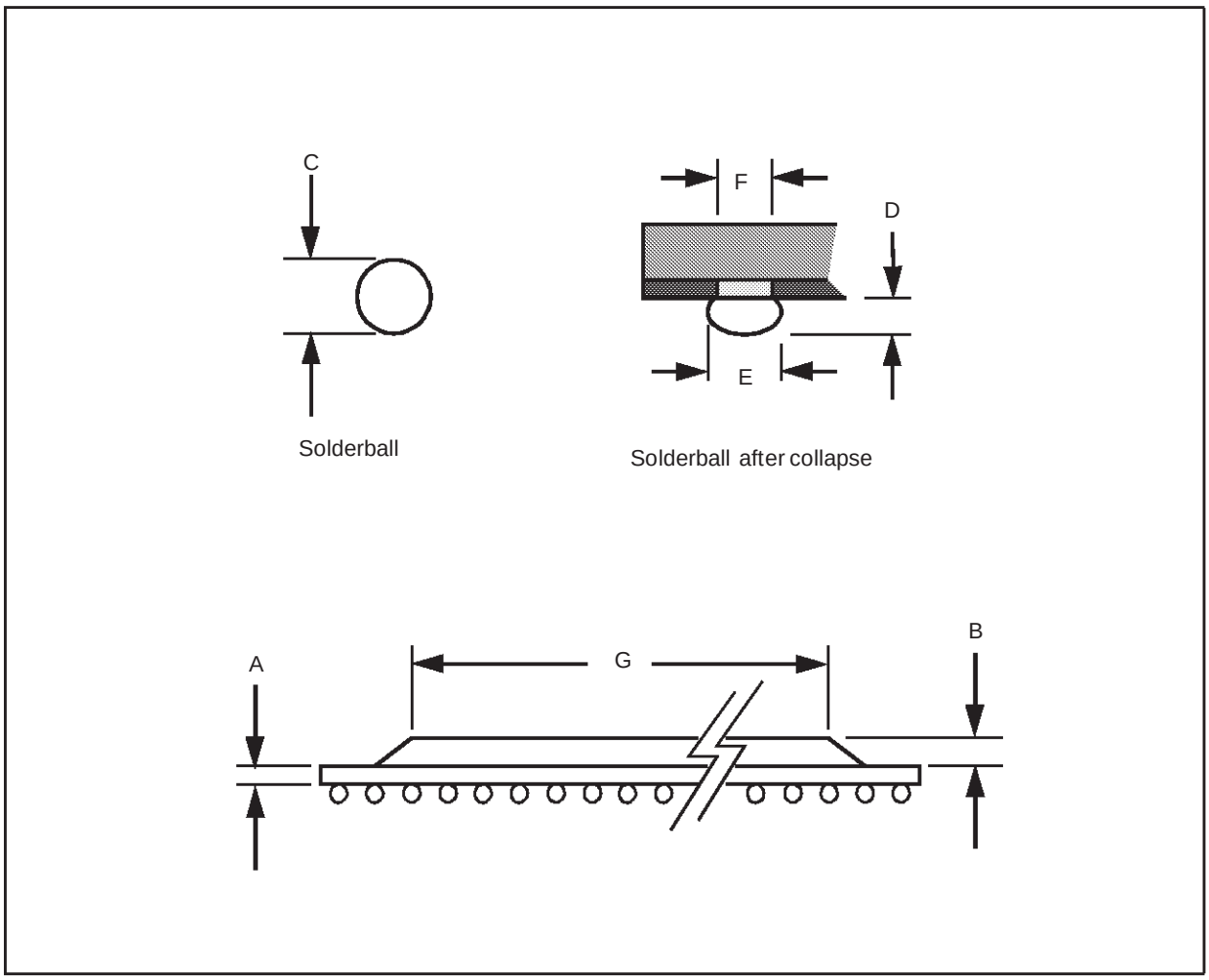
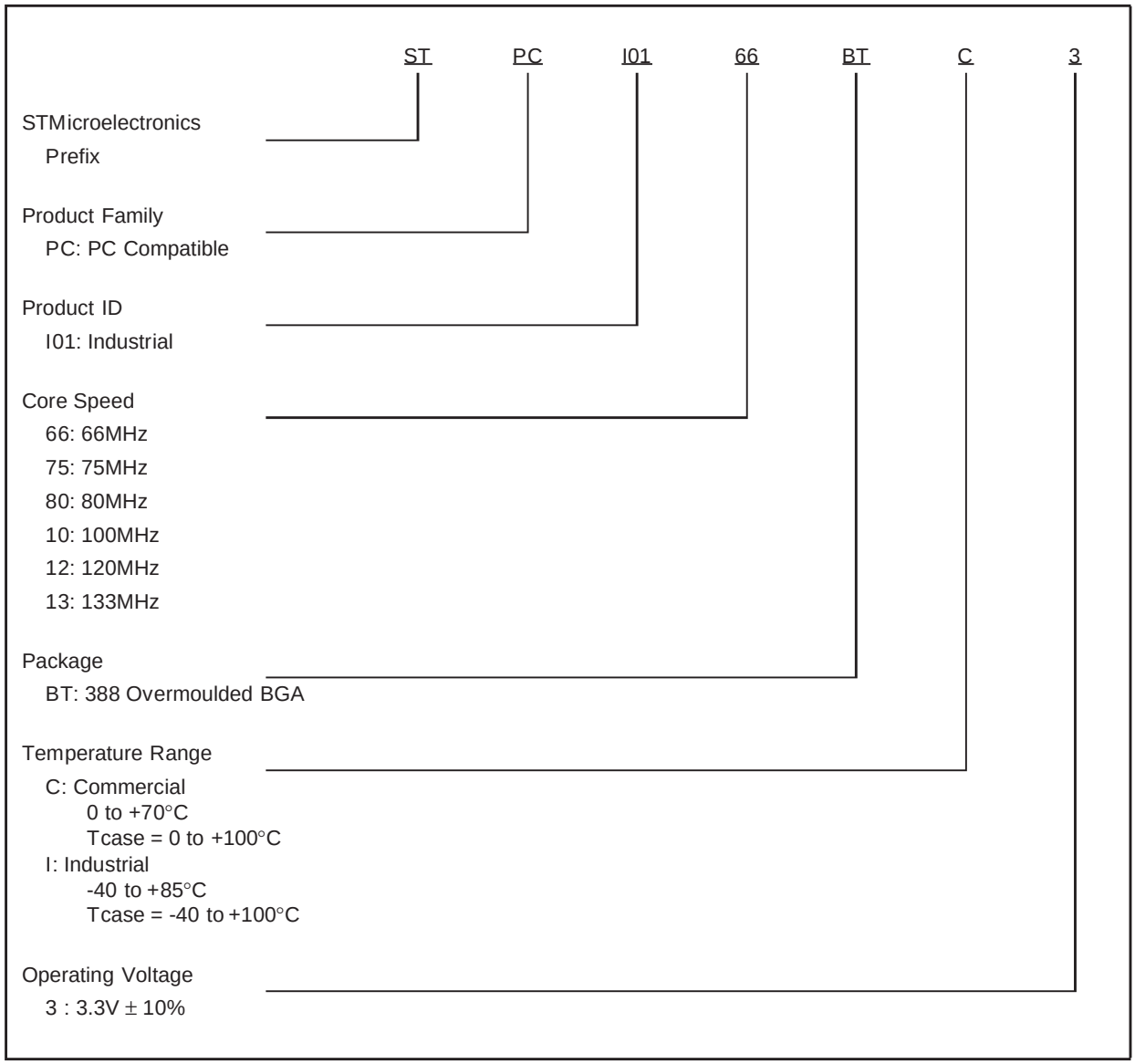


Table 13. PBGA388 - 388 Solder Ball Plastic 35mm x 35mm (Continued)

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

5 ORDERING DATA

5.1 Ordering Codes



5.2 Available Part Numbers

Part Number	Core Frequency (MHz)	Temperature Range (C)	Operating Voltage (V)
STPCI0166BTC3	66	0 to + 70°	3.3V ± 10%
STPCI0175BTC3	75		
STPCI0180BTC3	80		
STPCI0110BTC3	100		
STPCI0112BTC3	120		

5.3 Customer Service

More informations are available on STMicroelectronics internet site *http:// www.st.com/stpc*.

For technical support, a mail-box is in place at *stpc.support@st.com*.