STEL-1173
Data Sheet

STEL-1173RH

48-Bit Resolution Rad Hard CMOS Numerically Controlled Oscillator

STANFORD TELECOM®

RAD HARDNESS CAPABILITIES

- **TOTAL DOSE – 1 MRAD (Si)**
- **DOSE RATE**
  - **UPSET > 10^9 RADS (Si)/SEC**
  - **LATCHUP > $2x10^{11}$ RADS (Si)/SEC**
- **PROJECTED NEUTRON FLUENCE > 10^{14} N/CM^2**

FEATURES

- **48-BIT FREQUENCY RESOLUTION**
  - **CASCADABLE FOR HIGHER RESOLUTION**
- **12-BIT SINE OR COSINE OUTPUT**
- **HIGH SPECTRAL PURITY**
  - **ALL SPURS < –75 dBc**
- **40 MHz MAXIMUM CLOCK FREQUENCY (POST RADIATION)**
- **MICROPROCESSOR COMPATIBLE INPUTS**
- **2's COMPLEMENT OR OFFSET BINARY CODE**
- **LOW POWER DISSIPATION**
- **TEMPERATURE RANGE: –55 TO +125 ° C**
- **84-PIN FLAT PACKAGE (PREFERRED) OR CERAMIC PGA**

FUNCTIONAL DESCRIPTION

The STEL-1173RH Numerically Controlled Oscillator (NCO) uses digital techniques to provide the aerospace industry with a cost-effective solution to low noise signal sources. The NCO device combines a low power, rad-hard, 1.5µ bulk CMOS technology with a unique architectural design, resulting in a power efficient, high-speed sinusoidal waveform generator providing finer tuning resolution and higher spectral purity than was previously available in a single chip solution. This performance is enhanced by rapid switching capability and the use of a microprocessor control interface.

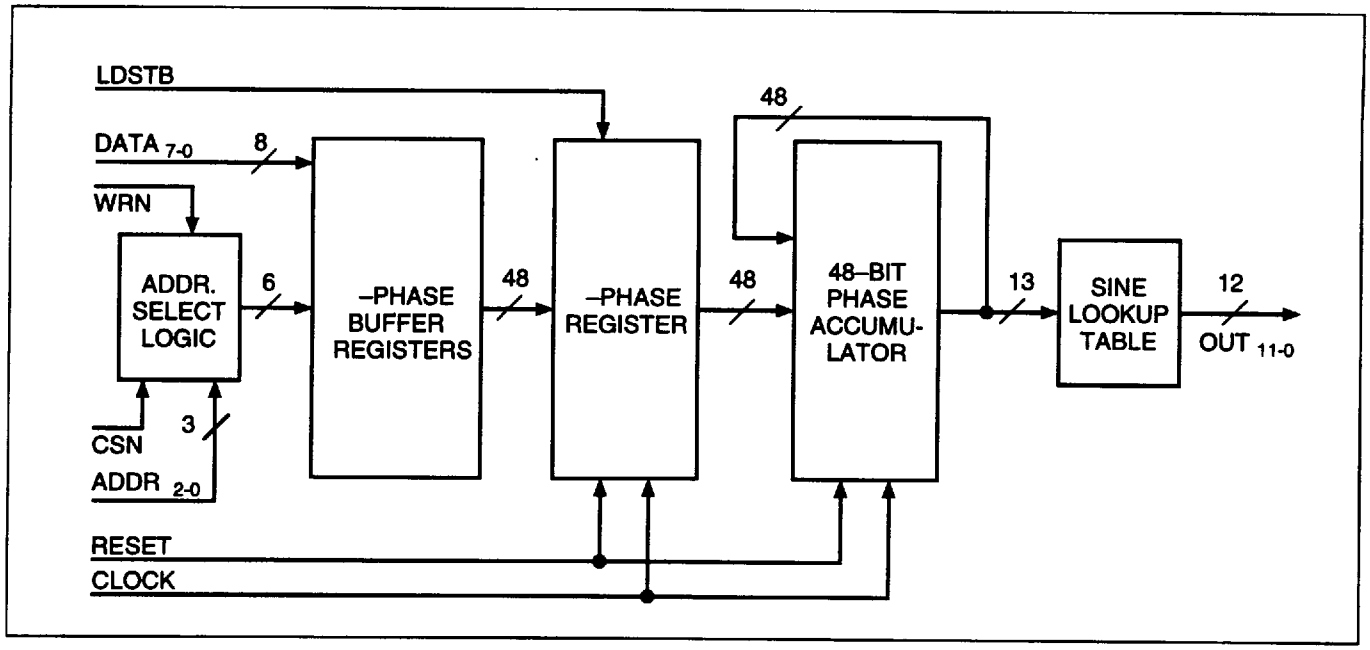
The STEL-1173RH is a rad-hard version of the STEL-1173. The two devices are functionally identical, but the maximum operating frequency of the STEL-1173RH is degraded to 40 MHz because of the military temperature range specification. The output frequency can be calculated from the following equation:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{48}}$$

where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

The sine and cosine functions are generated from the 13 most significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ-Phase register which may be programmed by an eight-bit microprocessor.

BLOCK DIAGRAM



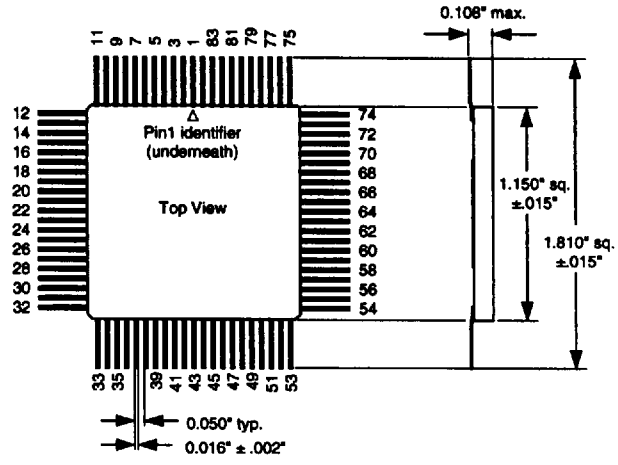
The frequency programming capability of the NCO is analogous to sampling a sine wave where the sampling function is the clock. If the output frequency is very low with respect to the clock ($< f_c/8096$), then the NCO output will sequence through each of the 8096 states of the sine function. As the output frequency is increased with respect to the clock the sine function will appear to be more discontinuous since there will be fewer samples in each cycle. At the Nyquist limit, when the output frequency is exactly half the clock, the output waveform reduces to a square wave. The practical upper limit of the NCO output frequency is about 40% of the clock frequency because spurious components created by sampling, which are at a frequency greater than half the clock frequency, become difficult to remove by filtering.

The phase noise of the NCO output signal may be determined by knowing the phase noise of the clock signal input, and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 20 clock cycles. This effectively limits the minimum possible frequency switching period of the NCO. After new frequency data is entered, the load command is given. After the 20 cycle pipeline delay, the output will instantaneously switch frequency while maintaining phase coherence. After this, the next new frequency may be entered. If a 40 MHz clock were utilized, the NCO could be continuously switched between programmed frequencies with a minimum practical average switching time of about 0.5 µsec.

PIN CONFIGURATION

Package: 84-pin flat pack
Notes:
1. Tolerance on pin spacing is not cumulative.
2. I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.
3. N.C. denotes No Connection. These pins may be used for vias.



PIN CONNECTIONS

1	V_{SS}	18	N.C.	35	V_{SS}	52	V_{DD}	69	OUT_8
2	N.C.	19	N.C.	36	N.C.	53	RESET	70	N.C.
3	N.C.	20	N.C.	37	SINE	54	OUT_0	71	V_{SS}
4	$ADDR_0$	21	$DATA_4$	38	N.C.	55	OUT_1	72	OUT_9
5	N.C.	22	V_{SS}	39	N.C.	56	OUT_2	73	OUT_{10}
6	$ADDR_1$	23	V_{DD}	40	N.C.	57	N.C.	74	OUT_{11} (MSB)
7	N.C.	24	$DATA_6$	41	TWOSCOMP	58	V_{SS}	75	SYNC
8	V_{SS}	25	N.C.	42	V_{SS}	59	N.C.	76	V_{SS}
9	$ADDR_2$	26	$DATA_5$	43	V_{DD}	60	OUT_3	77	V_{SS}
10	CARRY IN	27	N.C.	44	N.C.	61	OUT_4	78	N.C.
11	$DATA_0$	28	$DATA_7$	45	N.C.	62	OUT_5	79	N.C.
12	$DATA_1$	29	V_{SS}	46	LDSTB	63	V_{SS}	80	N.C.
13	$DATA_2$	30	I. C.	47	N.C.	64	V_{DD}	81	CLOCK
14	V_{SS}	31	WRN	48	CARRY OUT	65	OUT_6	82	N.C.
15	$DATA_3$	32	V_{DD}	49	N.C.	66	N.C.	83	N.C.
16	N.C.	33	I. C.	50	CSN	67	OUT_7	84	V_{DD}
17	N.C.	34	V_{SS}	51	V_{SS}	68	N.C.		

INPUT SIGNALS

RESET
The **RESET** input is asynchronous and active low. When **RESET** goes low, all registers including the 48-bit input buffer are cleared within 40 nsecs. The data on the **OUT11-0** bus will then be invalid for 5 rising clock edges, and thereafter will remain at the value corresponding to zero phase, i.e., 2049 (801H), until a new frequency is loaded into the Δ-Phase register with a **LDSTB** command after the **RESET** returns to a logic one.

CLOCK
All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 40 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 10 nanoseconds. At each positive transition of the **CLOCK** signal, the number stored in the Δ-Phase register is added to the contents of the phase accumulator and the result is placed in the phase accumulator.

$DATA_0$ through $DATA_7$
The eight bit $DATA_0$ through $DATA_7$ bus is used to program the 48 bit Δ-Phase register. $DATA_0$ is the least significant bit of the bus.

$ADDR_0$ through $ADDR_2$
The three address lines **ADDR2-0** control the use of the **DATA7-0** bus for writing frequency data to the Δ-Phase buffer registers as shown in the table below:

$ADDR_2$	$ADDR_1$	$ADDR_0$	Δ-Phase Register Field
0	0	0	Bits0 (LSB) –7
0	0	1	Bits 8–15
0	1	0	Bits 16–23
0	1	1	Bits 24–31
1	0	0	Bits 32–39
1	0	1	Bits 40–47 (MSB)

To write to all 48 bits of the phase write registers, the **DATA7-0** bus must be used 6 times. Note that it is not necessary to reload unchanged bytes, and that the byte loading sequence may be random.

WRN
On the rising edge of the **WRN** input, the information on the 8-bit data bus is transferred to the buffer register selected by the **ADDR2-0** bus.

CSN
The **CSN** (Chip Select) input is active low and can be used to control the writing of data into the chip. When this input is high all data writing via the **DATA7-0** bus is inhibited.

LDSTB
On the rising edge of the clock following the falling edge of the **LDSTB** input, the information in the 48-bit buffer register is transferred to the Δ-Phase register. The frequency of the NCO output will change 20 rising clock edges cycles after the **LDSTB** command due to pipelining delays.

CARRY IN
Normal operation of the NCO requires that **CARRY IN** be set at a logic 0. When **CARRY IN** is a logic 1, the effective value of the Δ-Phase register is increased by one. Two NCOs can be cascaded together to obtain 96 bits of frequency resolution by using the **CARRY OUT** of the lower order NCO and the **CARRY IN** of the higher order NCO.

TWOSCOMP
When the **TWOSCOMP** input is set high, the data appearing on the **OUT11-0** bus is presented in two's complement code, and when it is set low, the data is presented in offset binary code. The limits of the data values in both codes is shown below:

Code →	Offset binary	2's Complement
Minimum value	+1 (001_H)	– 2047 (801_H)
Maximum value	+4095 (FFF_H)	+2047 ($7FF_H$)
Mean value	+2048 (800_H)	0 (000_H)

Both number formats produce sine or cosine waves which are symmetrical about the phase quadrant axis and the mean-value magnitude axis.

SINE
When the **SINE** input signal is set to a logic low level, the output signal appearing on the **OUT11-0** bus is the cosine of the 48-bit accumulator's 13 most significant bits (bits 47-35, with 47 being the MSB). Normally set high, this signal allows the NCO to generate either sine or cosine signals. By using two devices, one set in the sine mode and the other set in the cosine mode, quadrature outputs may be obtained. The quadrature phase relationship of the two outputs will be maintained at all times provided the two devices are

reset simultaneously and operate from a common clock signal.

A high level on the **SINE** input sets the output to be the sine of the 48-bit accumulator's 13 most significant bits. The value of the output for a given phase value follows the relationship:

2's comp = 2047 x sin (360 x phase)

offset bin = 2047 x sin (360 x phase) +2048

The result is accurate to within 1 LSB.

When this input is set low the output will be the cosine of the 48-bit accumulator's 13 most significant bits. The value of the output for a given phase value follows the relationship:

2's comp = 2047 x cos (360 x phase)

offset bin = 2047 x cos (360 x phase) +2048

again, accurate to within 1 LSB.

OUTPUT SIGNALS

OUT_{11-0}

The signal appearing on the OUT_{11-0} bus is derived from the 13 most significant bits of the phase accumulator. The 12-bit sine or cosine function is presented in offset binary or two's complement format, depending on the status of the **TWOSCOMP** input. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 in offset binary and 1 in two's complement. The nominal phase (in degrees) of the sine wave output may be determined at any point by multiplying the decimal equivalent of the 13 most significant bits of the phase accumulator by (360/8192) and then adding (360/16384). OUT_{11} is the MSB, and OUT_0 is the LSB.

CARRY OUT

Each time the contents of the phase accumulator exceeds the maximum value that can be represented by a 48 bit number the **CARRY OUT** signal goes high for one clock cycle.

SYNC

The normally high **SYNC** output goes low for one clock cycle, 20 clock cycles after a **LDSTB** command, to indicate the end of the pipeline delay and the start of the new steady state condition.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–65 to +150	°C
T_a	Operating Temperature	–55 to +125	°C
V_{DDmax}	Max. voltage between V_{DD} and V_{SS}	–0.3 to +7.0	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DD}+0.3	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{SS}–0.3	volts

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 10%	volts
T_a	Storage Temperature (Ambient)	–55 to +150	°C
T_a	Operating Temperature (Ambient)	–55 to +125	°C

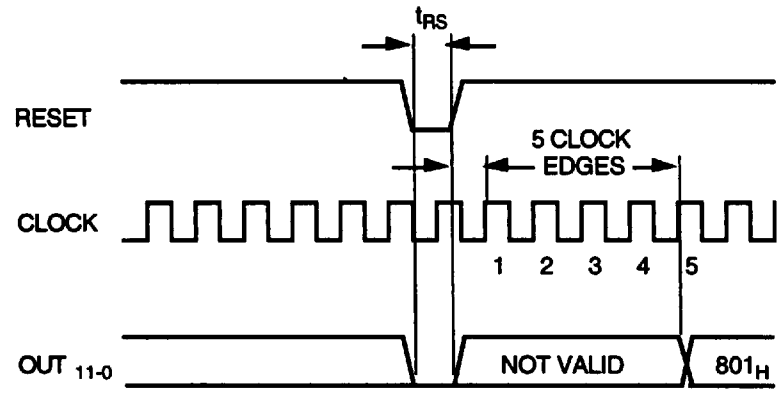
D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C

Symbol	Parameter	Min.	Max.	Units	Conditions
VIH (min)	Min. High Level Input Voltage	2.2		volts	Guaranteed Logic '1'
VIL (max)	Max. Low Level Input Voltage		0.8	volts	Guaranteed Logic '0'
VIHC (min)	Min. High Level Input Voltage,	0.7x		volts	Guaranteed Logic '1'
	High **CLOCK** Input	VDD			
VILC (max)	Max. Low Level Input Voltage,		0.3x	volts	Guaranteed Logic '0'
	Low **CLOCK** Input		VDD		
VOH1(min)	Min. High Level Output Voltage	2.4		volts	IOH1 = -2.6 ma
	High **DATA (0-7)** Outputs				
VOL1(max)	Max. Low Level Output Voltage		0.4	volts	IOL1 = 2.6 ma
	Low **DATA (0-7)** Outputs				
VOH2(min)	Min. High Level Output Voltage	2.4		volts	IOH2 = -4.0 ma
	All Other Outputs				
VOL2(max)	Max. Low Level Output Voltage		0.4	volts	IOL2 = 4.0 ma
	All Other Outputs				
IIHC	High Level Input Current	–	10	µA	Vin = VDD (pure input)
	CLOCK Input				
IILC	Low Level Input Current	–	-10	µA	Vin = VSS (pure input)
	Clock Input				
IIH	High Level Input Current				
	ADDR1, CARRY IN and **CSN**	150	900	µA	Vin = VDD (pulldown)
	All Other Inputs	-10	10	µA	Vin = VDD (pullup)
IIL	Low Level Input Current				
	ADDR1, CARRY IN and **CSN**	-10	10	µA	Vin = VSS (pulldown)
	All Other Inputs	-900	-150	µA	Vin = VSS (pullup)

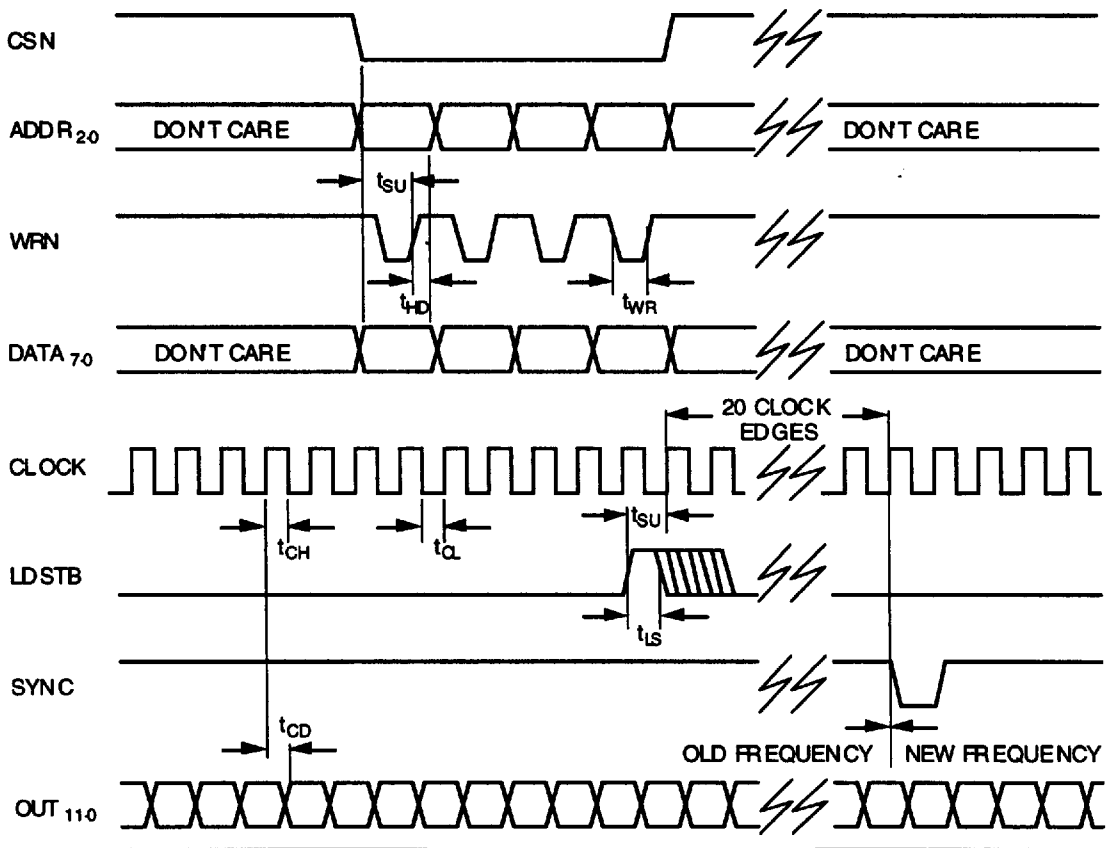
A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{RS}	RESET pulse width	30		nsec.	
t_{SU}	DATA, ADDR or CSN to WRN Setup	18		nsec.	
t_{HD}	DATA, ADDR or CSN to WRN Hold	12		nsec.	
t_{CH}	CLOCK high	10		nsec.	f_{CLK}= 40 MHz
t_{CL}	CLOCK low	10		nsec.	f_{CLK}= 40 MHz
t_{WR}	WRN pulse width	24		nsec.	
t_{LS}	LDSTB pulse width	24		nsec.	
t_{CD}	CLOCK to output delay	2	20	nsec.	Load = 20 pF max.

NCO RESET SEQUENCE



NCO FREQUENCY CHANGE



SPECTRAL PURITY

In many applications the NCO is used with a digital to analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

The sine and cosine signals generated by the STEL-1173 have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically about –75 dBc. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the NCO approaches f_c /2, the "image" spur at $f_c–f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a 10-bit DAC (Sony CX20202A-1) is shown below.

In this case, the clock frequency is 50 MHz and the output frequency is programmed to 6.789 MHz. (Note: Maximum post total dose guaranteed clock speed is 40 MHz.) The maximum non-harmonic spur level observed over the entire useful output frequency range in this case is –74 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c– 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to select a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency:	6.7 MHz
Frequency Span:	10.0 MHz
Reference Level:	–5 dBm
Resolution Bandwidth:	1 KHz
Video Bandwidth:	3 kHz
Scale:	Log, 10 dB/div
Output frequency:	6.789 MHz
Clock frequency:	50 MHz