ABRIDGED VERSION

SSI 33P3701

silicon systems®
A TDK Group Company

8-48 Mbit/s Magneto Optical Read Channel with PPM/PWM Pulse Qualification

Advance Information

February 1996

DESCRIPTION

The SSI 33P3701 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto optical (MO) drive systems, compatible with PWM signals and backwards compatible with PPM signals. Functional blocks include sum and difference amplifier, input attenuator, sag canceller, pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 48 Mbit/s for (1,7) code, 6 to 36 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3701 are controlled through a bidirectional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The 33P3701 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL

- **Programmable MO/EMBOSS data rate of 8 to 48 Mbit/s for (1,7 RLL) code, 6 to 36 Mbit/s for (2,7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (600 mW typical @ 5V)**
- **Bidirectional serial port register access**
- **Register programmable power management (sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 80-lead TQFP package**

PULSE DETECTOR

- **Provides the head amplifiers difference for MO and sum for emboss signals**
- **Dual programmable attenuator (min-24 dB, 4-bit resolution) for MO and emboss data with Low-Z switch and internal multiplexer**
- **Dual sag canceller for MO and emboss data**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO and emboss**
- **Separate MO and emboss AGC levels (4-bit DAC)**
- **Optimized user selectable pulse qualification circuitries for pit mark/edge recording**
- **Internal fast decay timing**
- **External $\overline{LOW\_Z}$ control pin**
- **Data synchronizer input (RDI/RDI2)**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 24 MHz**
- **Programmable boost/equalization of 0 to 12 dB**
- **Matched normal and differentiated outputs**
- **High resolution fc accuracy**
- **Minimum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **No external filter components required**

(continued)

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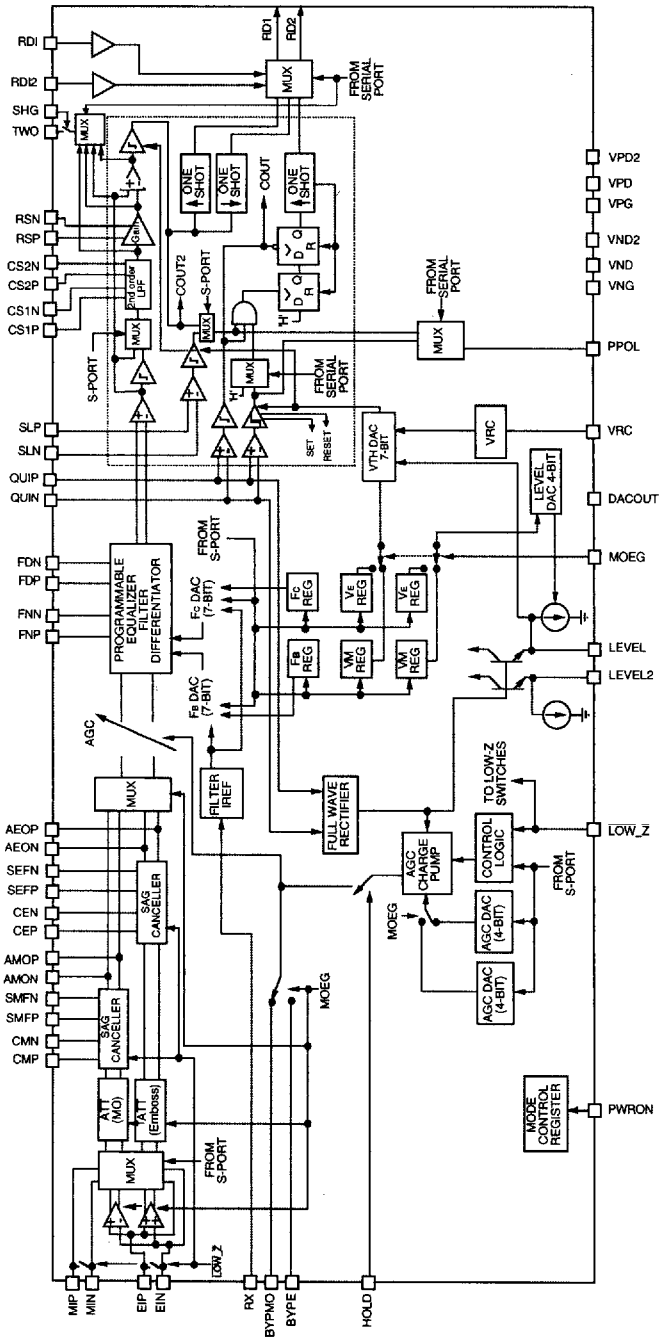
FEATURES (continued)

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent divide-by M and N registers
- VCO center frequency matched to data synchronizer VCO
- VCO (FOUT) output available
- Can be used as a Data Syncronizer for trailing edge in PWM read mode

DATA SYNCHRONIZER

- User selectable PPM and PWM synchronizer circuitries
- Dual PLL for leading and trailing edge in PWM read mode
- Fast acquisition phase lock loop with zero phase restart technique
- Fully integrated data synchronizer
  - No external delay lines, active devices, or active PLL components
- Programmable decode window symmetry control via serial port
  - Window shift control ±30% (4-bit)
  - Includes delayed read MO/emboss data and VCO clock monitor points



Block Diagram - Front End

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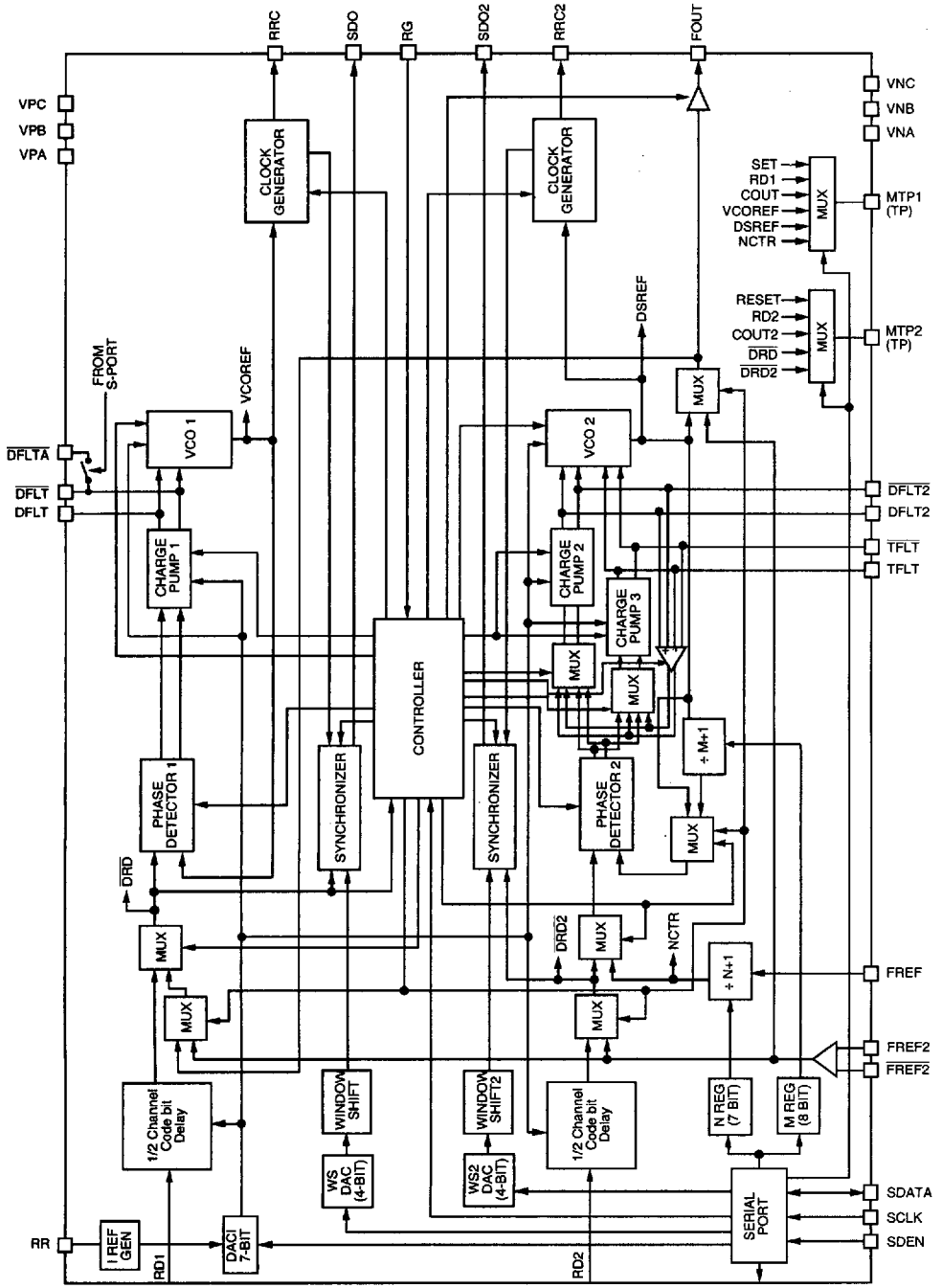

Block Diagram -Back End

FUNCTIONAL DESCRIPTION

The SSI 33P3701 implements a high performance complete read channel, including head amplifiers, dual programmable attenuator & sag canceller, multiplexer, pulse detector, programmable active filter, time base generator, and data synchronizer, at data rates up to 48 Mbit/s for (1,7) code, 36 Mbit/s for (2,7) code. A circuit diagram is shown in Figure 1.

INPUT INTERFACE & PULSE DETECTOR CIRCUIT DESCRIPTION

This device provides 2 types of interfaces to the pulse detector, which are selected by MOEG and PDCR bit 1 for customer applications. One is the RF signal interface (EIP/EIN), which provides two types of head amplifiers with a dual attenuator for the signal from the I-V converter outputs. The second is the programmable attenuator interface(MIP/MIN, EIP/EIN), which provides a dual attenuator for MO and emboss signals. The AC coupled connections are necessary for these input interfaces. When the $\overline{\text{LOW\_Z}}$ pin is driven low, the input impedance at these input interfaces are reduced to allow for quick recovery of AC coupling capacitors. This Low_Z mode enables cancellation of the offset occurring at the beginning of MO and emboss signals.

The pulse detector, in conjunction with the programmable filter, provides all the MO data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide bandwidth full wave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

HEAD AMPLIFIER

Two types of head amplifiers are provided: the difference amplifier for MO signals and the summing amplifier for emboss signals. The gain of the difference amplifier is 5x and the summing one is 0.5x. Therefore the input ranges of EIP/EIN are 40-220 mVp-pd in MO mode (MOEG=low), 100-1100 mVp-p in emboss mode (MOEG=high) when PDCR bit 1 is low. In this interface, bypass head amplifier mode is selectable by CAR bit 4 for connection with SSI Preamplifier 33R3750. When PDCR bit 1 goes high, these head amplifiers are disabled and MIP/MIN (MOEG=low) or EIP/EIN (MOEG=high) input is active.

PROGRAMMABLE ATTENUATOR

Dual attenuators are provided for the input signal swing variations of MO and emboss signals dependent on the zone and media. The maximum input range is 1.1 Vp-pd and programmable range is 1 to 1/16 by 1/16 step.

ATT Gain (MO) = (16-ATTMO)/16 V/V

ATT Gain (emboss) = (16-ATTEM)/16 V/V

where ATTMO is the lower 4 bits of Attenuator Gain Register (ATGR) and ATTEM is the upper 4 bits.

SAG CANCELLER

Dual sag cancellers are provided for MO and emboss signals with a LOW_Z switch and an internal multiplexer for the AGC stage. This circuit compensates for the low frequency components of the input signal suppressed by the input high pass filter (AC coupling capacitor and internal input resistance) to cancel the sag. Feedback capacitors are necessary. Their value must be the same as the input AC coupling capacitor's value. By connecting a resistor in parallel with the feedback capacitor, it is possible to suppress the low frequency component again at a new cutoff frequency (e.g., to avoid the influence of the birefrengence).

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYPx}) stored on the BYPx hold capacitor (C_{BYPx}). A dual rate charge pump drives C_{BYPx} with currents that depend on the instantaneous differential voltage at the amplifier gain, while decay currents increase V_{BYPx} which increase the amplifier gain. When the signal at QUIP/QUIN is greater than 100% of the programmed AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high/low yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 μA acts to increase the amplifier gain when the signal at QUIP/QUIN is less than the programmed AGC level. The large ratio (0.18 mA : 4 μA) of the nominal attack and nominal decay currents allow the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is

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AGC CIRCUIT (continued)

provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 21.

In read mode, the reference voltage for the AGC charge pump is a nominal 1V. If required, the reference voltage for the AGC charge pump is set by a 4-bit DAC (DACAMO/DACAEM) controlled by the AGC level register. The DAC output voltage is offset so that "1111" results in a 0.76V output, and "0000" results in a 1V output:

$$V_{AGC} = 1.00 - (DACA\ X \times 0.016)\ Vp\text{-}p$$

where DACAX is the decimal value of the AGC Level register (DACAMO/DACAEM).

When the chip is in power down mode, the AGC dual rate charge pump is disabled.

Upon power up, the $\overline{LOW\_Z}$ pin should be brought low then high to execute fast decay. The part will recover from any transients or drift which may have occurred on the BYPx hold capacitors.

BYPMO AND BYPE CONTROL VOLTAGE

The BYPx capacitor voltage will be held constant (subject to leakage currents) during sleep mode, Low_Z mode, or when the HOLD signal is high. Upon the transition of PWRON from low to high, there is a 1 µs delay inserted before the AGC loop is allowed to drive the BYPx capacitor selected by the MOEG pin (see AGC mode control). When MOEG is low, the BYPMO capacitor will be active and the BYPE capacitor voltage will be held constant (subject to leakage currents). When MOEG is high, the BYPE capacitor will be active and the BYPMO capacitor voltage will be held constant (subject to leakage currents). The high gain start mode (CAR bit1=high) enables a constant decay current of 4 µA to increase V_{BYPMO} voltage during emboss mode. The AGC acts from high gain at the transition to MO mode.

AGC MODE CONTROL

When the $\overline{LOW\_Z}$ pin is driven low, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant, and the AGC input signal to be muted. When the $\overline{LOW\_Z}$ pin goes high, the fast decay mode is internally set at a nominal 1 µs. Fast decay mode is also triggered by a transition of the MO/emboss gate (MOEG) pin in either direction. When the pulse detector is powered down, V_{BYPx} will be held constant subject to leakage currents only.

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, V_{BYPx} will be held constant subject to leakage currents only.

RDI INPUT PIN

Dual TTL compatible read data inputs (RDI/RDI2) are provided as read data inputs to the synchronizer from an external qualification circuit. RDI/RDI2 are available when CAR bit 2 (RDI register bit) goes high.

PULSE QUALIFICATION FOR PPM

The SSI 33P3701 provides an optimized pulse qualification circuit for Pit Position Modulation (PPM). A differential comparator with programmable hysteresis threshold allows differentiated signal qualification for noise rejection. The programmable hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by the LEVEL voltage and referenced to VRC. The hysteresis threshold may be set from 10 to 80% with a resolution of 1%. A slice comparator also allows normal signal qualification for noise rejection. The slice level is set to AC ground when CBR bit 5 is low. When CBR bit 5 goes high, the slice level is added as an offset referenced to AC ground. This offset is related to the hysteresis threshold by a specific equation (see Electrical Specifications, Slice comparator). The internal current sink LEVEL DAC (DACL) and external capacitor CT set the hysteresis threshold time constant. DACL is switched between two 4-bit registers by MO/emboss gate (MOEG) to determine the sink current magnitude in MO data mode and emboss mode. In MO data mode, the four LSBs of the Hysteresis Decay Register (HDCR) determine the value of the pull-down current. In emboss mode, the four MSBs are selected. The LSB value of DACL is 3.125 µA. DACL is offset by 1 LSB such that "0000" corresponds to 3.125 µA, and "1111" results in 50 µA. The SSI 33P3701 also provides a LEVEL2 pin for detecting the input signal. The internal sink current is fixed at 50 µA.

The differentiated signal is connected to both the hysteresis and zero cross comparators. A positive peak that clears the established threshold level will set the hysteresis comparator. A peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator. This output signal is gated by

the slice comparator output when CAR bit 3 is low. When CAR bit 3 goes high, the gate output is independent of the hysteresis comparator output. A positive edge of this gate output sets the D-Flip-flop Q high. This in turn feeds into the D-input of the second Flip-flop which is triggered by the negative edge of the zero cross comparator output. Timing for the pulse qualification is shown in Figure 2.

PULSE QUALIFICATION FOR PWM

The SSI 33P3701 provides an optimized pulse qualification circuit for Pit Width Modulation (PWM). PWM mode is set by CCR bit 7. A slice comparator with asymmetry compensation circuits allows normal signal qualification. The slice level is normally set to AC ground (CBR bit 4 is low). The asymmetry compensation circuits are enabled when RG goes high, compensating the signal base-line fluctuation caused by the asymmetry during one sector. The components of the base-line fluctuation are abstracted through the zero cross comparator, second order LPF and the gain stage, and subtracted from the original signal. The cutoff frequency of the second order LPF is determined by internal resistors and external capacitors. The gain of the gain stage is set by the external resistor, and also interlocks to the LEVEL pin voltage to avoid being influenced by the AGC gain variation when CAR bit 1 is high. Timing for the pulse qualification is shown in Figure 3. The PWM qualification output is enabled by CBR bit 1 and used as the normal slice output for the PPM qualification.

When CBR bit 4 goes high, the slice level adds an offset referenced to AC ground for the slice level margin test. This offset value is equivalent to the absolute hysteresis threshold value of the differentiated signal. The offset polarity is controlled by CBR bit 3.

The SSI 33P3701 also provides a test write output pin (TWO) to monitor the write power conditions. When CBR bit 6 and 7 are high in MO mode (MOEG=low), the zero cross comparator is bypassed, the internal resistance of the second order LPF switches to low impedance, and the LPF output is connected to the TWO pin through the internal 10x buffer. This output makes it possible to monitor the differences of the center level between 2 types of continuous pattern signals (ex. 2T/8T).

PPOL OUTPUT PIN

A pulse polarity signal output (a pseudo CMOS output: PPOL) is provided for sector mark detection. This signal is a comparator output and can be selected by CBR bit 2 to be the output of the normal or differentiated signal. When CBR bit 2 goes low, the normal signal is selected. The normal signal polarity can be selected from either the PPM or PWM qualification circuit by CBR bit 1. When CBR bit 0 goes high, PPOL will be held High-Z. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative.

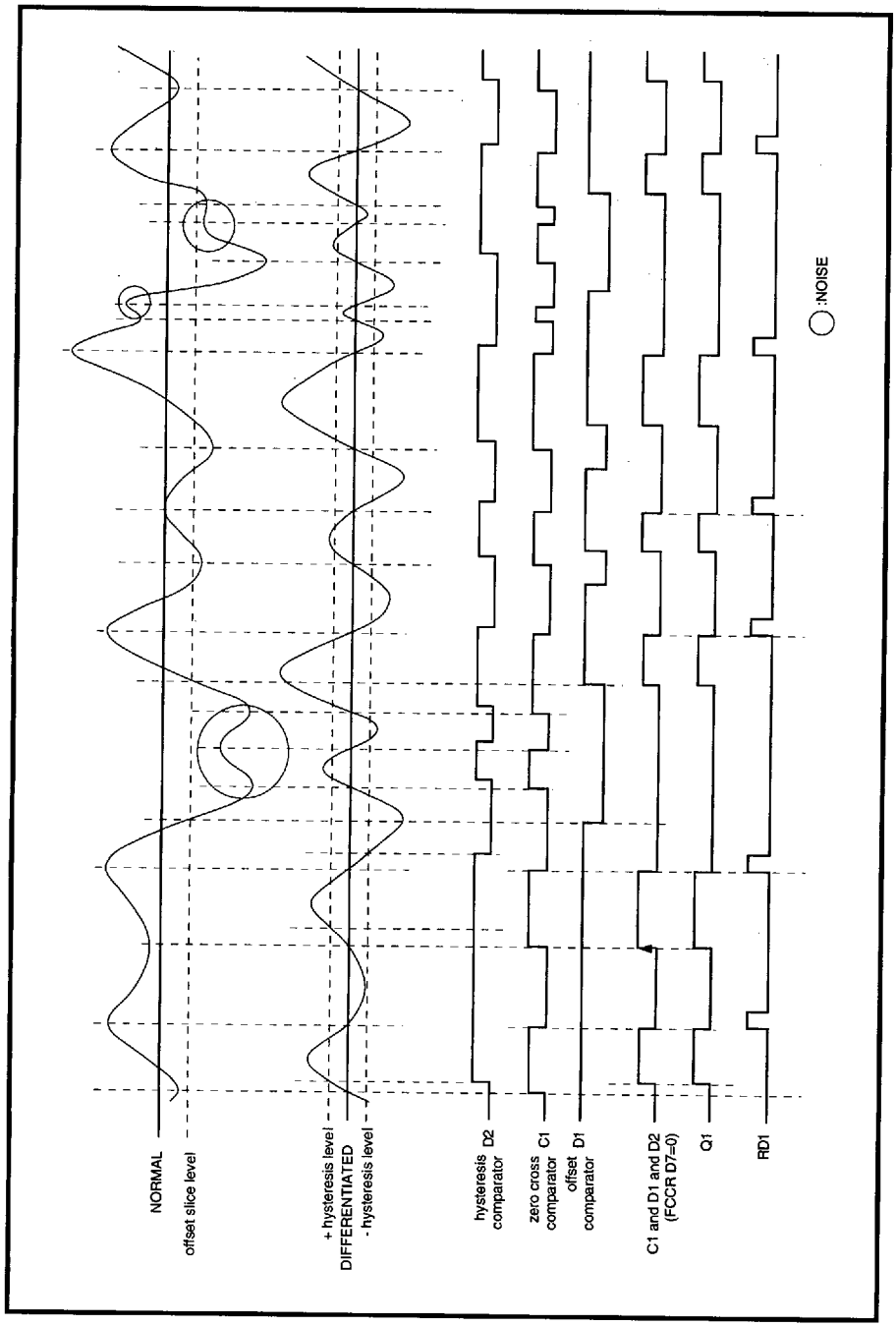

FIGURE 2 : Pulse Qualification Timing Diagram for PPM signal

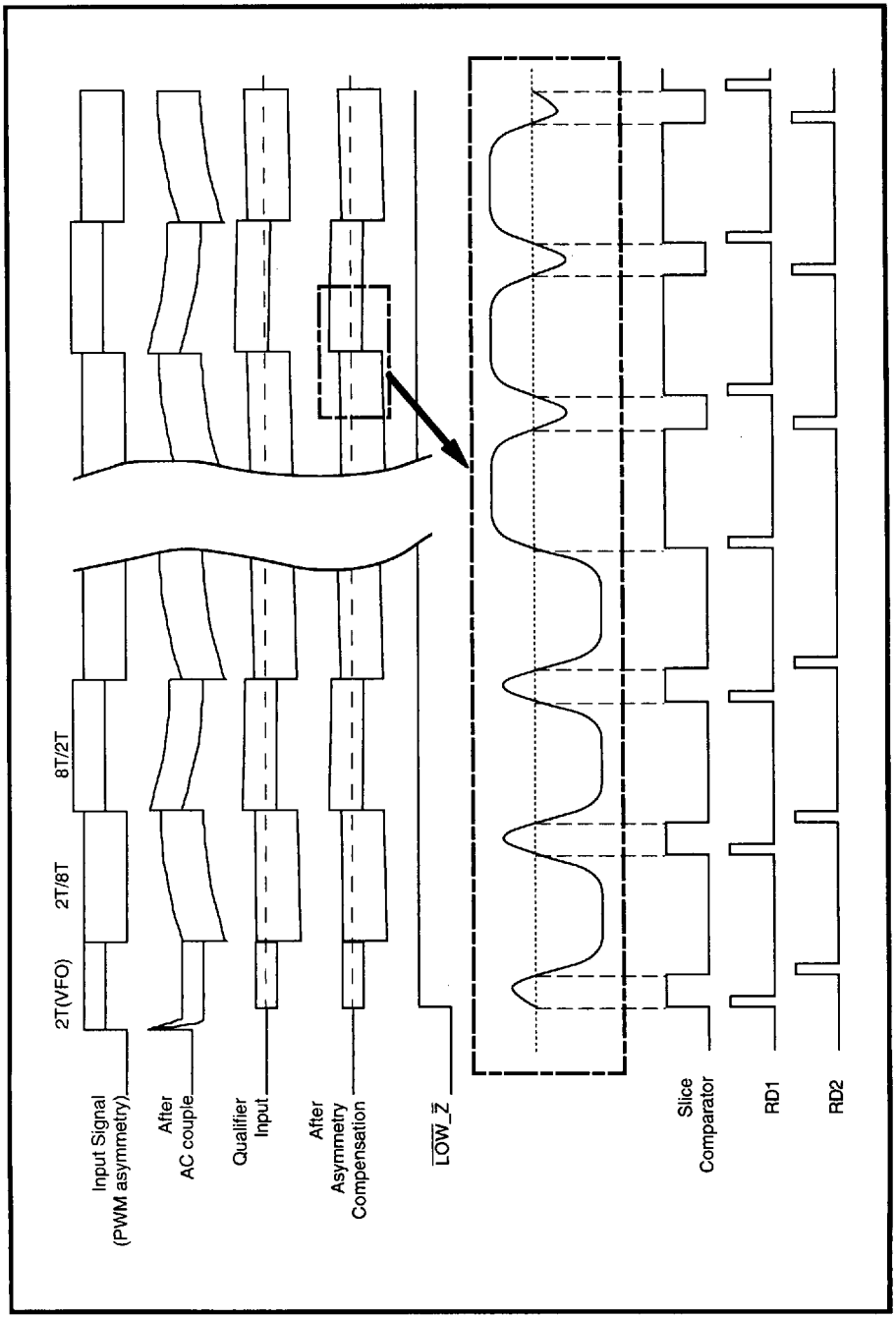

FIGURE 3 : Pulse Qualification Timing Diagram for PWM signal

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FUNCTIONAL DESCRIPTION (continued)

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 33P3701 programmable filter consists of an electronically controlled low-pass filter with separate normal and differentiated low-pass outputs. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., Wc = 2 πfc = 1) are:

Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] x A_N

and

Vdiff/Vi = (Vnorm/Vi) x (s/0.86133) x A_D

Where D (s)=

$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)(S^2 + 1.14558s + 5.37034)(s + 0.86133)$

A_N is adjusted for a gain of 10 at fs = (2/3) fc. A_D is adjusted for a gain of 10 at fs = fc in PPM mode and a gain of 15 at fs = fc in PWM mode.

FILTER OPERATION

The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc (MHz) = (0.194 x FCDAC) - 0.638

where FCDAC = FCCR register value.

In the read mode, the Filter Cutoff control Register (FCCR) is used to determine the filter's 3 dB cutoff frequency. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3 dB frequency.

TABLE 1: 3 dB cutoff frequency versus boost magnitude.

BOOST (dB)	fc (3 dB)	BOOST (dB)	fc (3 dB)
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32		

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost (dB) = 20 log [(0.02559 x FBDAC) +(3.8 x 10^{-5} x FBDAC x FCDAC) + (-1.6 x 10^{-5} x $FBDAC^2$) + 1]

where FBDAC = FBCR register value.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

The time base generator is programmed to provide a stable reference frequency for the data synchronizer and FOUT pin. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1)) FREF

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the data recovery control register (DRCR). This DAC also sets the 1/2 channel code bit delay, VCO center frequency and phase detector gain for the data synchronizer circuitry. A phase detector gain of 3 times KD is controlled by CCR bit 0. When changing frequencies, the M and N registers must be loaded first, followed by the DRCR register. A frequency change is initiated only when the DRCR register has been changed.

$$Fvco = [12.5/(RR + 0.4)] \times [(0.622 \times DACI) + 4.27] \text{ MHz}$$

For Fvco < 24 MHz,

$$Fvco = [12.5/(RR + 0.4)] \times [(0.7 \times DACI) + 1.4] \text{ MHz}$$

DACI is the value in the DRCR, and RR is the value (kΩ) of the external RR resistor, typically 12.1 kΩ.

In PWM read mode, the time base generator acts as a second data synchronizer for the trailing edge data of the PWM signal. The charge pump 2 and external passive loop filter 2 for the second data synchronizer are provided. During idle mode these interlock to the charge pump 1 and loop filter 1 of the data synchronizer to start from the same condition at the transition to read mode. When the internal read gate (see PREAMBLE SEARCH) is enabled, VCO2 is reset and prepared to be synchronized to MO/emboss data by changing the connection from the charge pump and loop filter. Following that, it operates the same as the data synchronizer. As for charge pump 3 and loop filter 3 for the time base generator, it acts in a manner that the loop filter voltage is the same as the loop filter 2 voltage in the emboss read mode. In the MO read mode, it is not active and the loop filter voltage is held constant subject to leakage current only. This operation is shown in Figure 4.

The SSI 32D4680 also can be used as an external time base genarator (CCR bit 4 = high). In this mode the internal time base generator always acts as the second data synchronizer. The reference clock from the external time base genarator is input to FREF2 and $\overline{\text{FREF2}}$ pins.

FOUT OUTPUT PIN

FOUT is a PSEUDO CMOS output that provides the time base generator output. The signal from this pin is actually the VCO2 output, so FOUT is not the time base clock during PWM read mode. When CCR bit 5 goes high, FOUT will be held High-Z.

DATA SYNCHRONIZER CIRCUIT DESCRIPTION

In the read mode, the data synchronizer performs data synchronization. Data rate is established by the time base generator and the internal reference DACI controlled by the DRCR. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/2 channel code bit delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the idle mode. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{\text{DRD}}$ pulse. In the idle mode the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is also fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL. The damping factor of the loop filter is enabled to change between PPM and PWM mode by switching the connection of the $\overline{\text{DFLTA}}$ pin.

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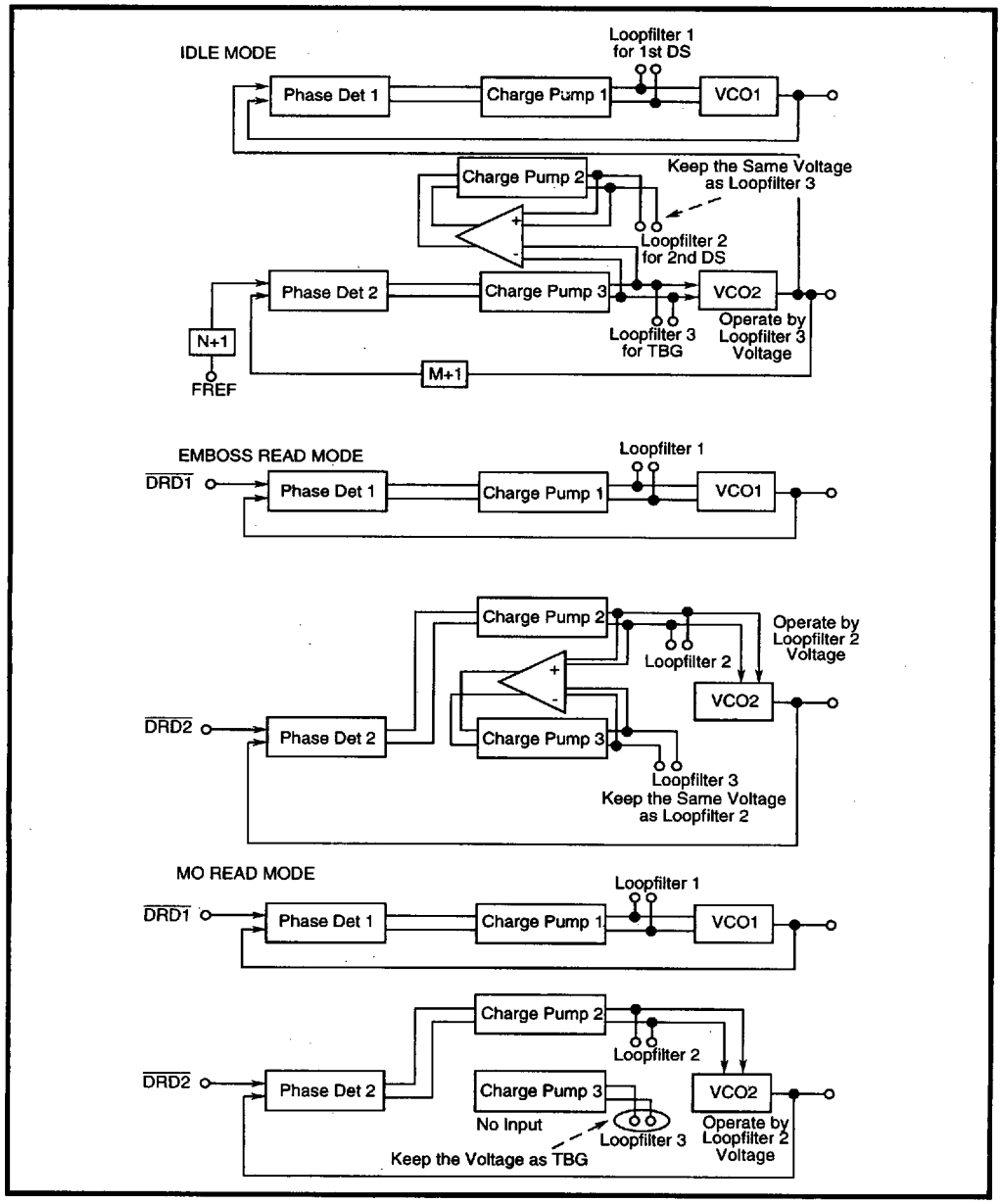

FIGURE 4 : Back-end Conceptual Operation in PWM Mode

FUNCTIONAL DESCRIPTION (continued)

MODE CONTROL

The read gate (RG) input controls the device operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode, the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/2 code bit wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock.

PREAMBLE SEARCH

When RG is asserted, an internal counter is triggered to count negative transitions of the internal time base, FOUT. Once the counter reaches a count of 2, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time the VCO stops, and after 2 cycle count of $\overline{DRD}$ an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to MO/emboss data.

VCO LOCK

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, bit 0 in the Control D register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 16 RD1 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and dampening factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the MO data which follows. This (a total of 19 RD1 pulses from assertion of RG) asserts an internal VCO lock signal.

When the VCO lock signal is asserted, the RRC output is enabled as the VCO clock signal that is phase locked to $\overline{DRD}$. In the idle mode, the RRC output is disabled and set to low.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 16 RD1 transitions.

WINDOW SHIFT

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR/WSCR2). The WSCR2 is active in PWM mode. Further description of WSCR/WSCR2 is provided in the window shift control section.

NON-READ MODE

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual MO data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

OPERATING MODES AND CONTROL

The SSI 33P3701 has several operating modes that support read (MO/emboss), and power management functions. Mode selection is accomplished by controlling the read gate (RG), MO/emboss gate (MOEG), $\overline{LOW\_Z}$, HOLD and PWRON pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), the Control B register (CBR), the Control C register (CCR) and the Control D register (CDR) via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), MO/emboss gate (MOEG), $\overline{LOW\_Z}$, HOLD and PWRON pins with TTL compatible signals. For normal operation the PWRON pin is driven high. During normal operation the SSI 33P3701 is controlled by the read gate (RG) and MO/emboss gate (MOEG) pins. When RG is high, the device is in read mode. If the RG is low, the device will be in idle mode.

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FUNCTIONAL DESCRIPTION (continued)

During read mode, the MOEG pin can be activated to enable the emboss read mode of operation and with the HOLD pin hold the AGC gain. During idle mode, the $\overline{LOW\_Z}$ pin enables low input impedance at the input interfaces.

POWER DOWN CONTROL

For power management, the PWRON pin can be used in conjunction with the Power Down Control register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the PWRON pin is brought low ("0") the device is placed into sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the PWRON pin is driven high ("1"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the sleep mode, the $\overline{LOW\_Z}$ pin should be asserted following power down to initiate the sag canceller recovery sequence.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bidirectional port for reading and writing programming data from/to the internal registers of the SSI 33P3701. The serial port data transfer format is shown in Figure 5. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In serial port read mode (R/W=1) the SSI 33P3701 will output the register contents of the selected address. In serial port write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 6.

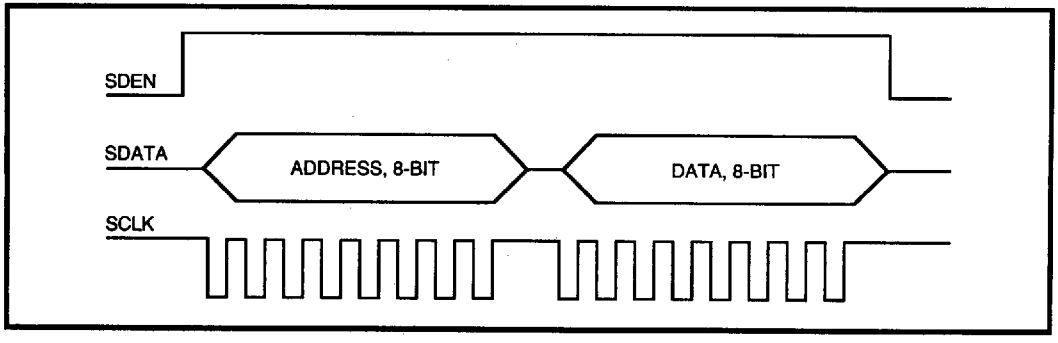

FIGURE 5: Serial Port Data Transfer Format

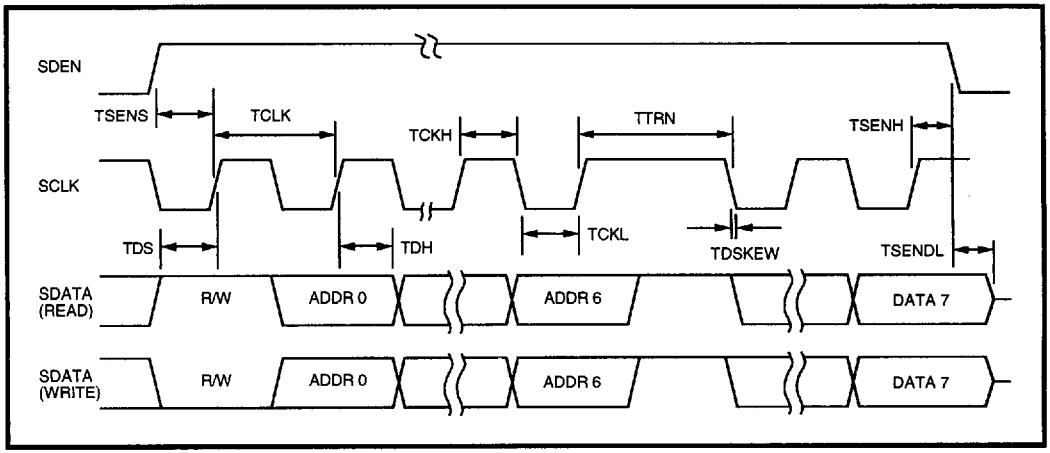

FIGURE 6 : Serial Port Timing Information

TABLE 2 : Mode Control

CONTROL LINE					DAC CONTROL			
PWRON	RG	MOEG	LOW_Z	DEVICE MODE	V_{TH}	AGC	ATT gain	HYSTERESIS
0	X	X	X	SLEEP MODE: All Functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
1	1	0	1	MO READ MODE: The pulse detector is active. The data synchronizer begins the preamble lock sequence.	MR	MR	MR	MR
1	1	1	1	EMBOSS READ MODE: The Pulse detector is active and the emboss control registers are selected for the V_{TH}, AGC Level, Hysteresis decay and Attentuator gain. The data syncronizer begins the preamble lock sequence.	ER	ER	ER	ER
1 (1	0 0	0 1	X X)	IDLE MODE: The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the MO data (Emboss) control registers are used for V_{TH} and FC.	MR (ER	MR ER	MR ER	MR ER)
-	-	-	-	All other states are illegal. If an illegal state is programmed, the chip function will be in an indertminable state, but no damage will occur.	MR	MR	MR	MR

DAC Control Key: MR = MO data register, ER = Emboss register, off = disabled

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TABLE 3 : Serial Port Register Mapping

REGISTER NAME	A6			ADDRESS			A0	R/W	D7			DATA BIT MAP				D0
POWER DOWN CONTROL (PDCR)	0	0	0	0	0	1	0	0	--	--	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	HEAD AMP 1=DISABLE 0=ENABLE	PD 1=DISABLE 0=ENABLE
MO DATA THRESHOLD (MDTR)	0	0	0	1	0	1	0	0	--	V_{TH} DAC BIT 6 MO	V_{TH} DAC BIT 5 MO	V_{TH} DAC BIT 4 MO	V_{TH} DAC BIT 3 MO	V_{TH} DAC BIT 2 MO	V_{TH} DAC BIT 1 MO	V_{TH} DAC BIT 0 MO
EMBOSS THRESHOLD (EMTR)	0	0	1	0	0	1	0	0	--	V_{TH} DAC BIT 6 EMBOSS	V_{TH} DAC BIT 5 EMBOSS	V_{TH} DAC BIT 4 EMBOSS	V_{TH} DAC BIT 3 EMBOSS	V_{TH} DAC BIT 2 EMBOSS	V_{TH} DAC BIT 1 EMBOSS	V_{TH} DAC BIT 0 EMBOSS
AGC LEVEL (ALCR)	0	1	0	0	0	1	0	0	DACAEM BIT 3	DACAEM BIT 2	DACAEM BIT 1	DACAEM BIT 0	DACAMO BIT 3	DACAMO BIT 2	DACAMO BIT 1	DACAMO BIT 0
HYSTERESIS DECAY (HDCR)	0	1	0	1	0	1	0	0	DACL BIT 3 EMBOSS	DACL BIT 2 EMBOSS	DACL BIT 1 EMBOSS	DACL BIT 0 EMBOSS	DACL BIT 3 MO	DACL BIT 2 MO	DACL BIT 1 MO	DACL BIT 0 MO
ATTENUATOR GAIN (ATGR)	0	1	1	0	0	1	0	0	ATTEM BIT 3	ATTEM BIT 2	ATTEM BIT 1	ATTEM BIT 0	ATTMO BIT 3	ATTMO BIT 2	ATTMO BIT 1	ATTMO BIT 0
FILTER CUTOFF (FCCR)	0	0	0	0	0	1	1	0	--	F_C DAC BIT 6	F_C DAC BIT 5	F_C DAC BIT 4	F_C DAC BIT 3	F_C DAC BIT 2	F_C DAC BIT 1	F_C DAC BIT 0
FILTER BOOST (FBCR)	0	0	0	1	0	1	1	0	--	F_B DAC BIT 6	F_B DAC BIT 5	F_B DAC BIT 4	F_B DAC BIT 3	F_B DAC BIT 2	F_B DAC BIT 1	F_B DAC BIT 0
DATA RECOVERY (DRCR)	0	0	0	0	1	0	0	0	--	DAC I BIT 6	DAC I BIT 5	DAC I BIT 4	DAC I BIT 3	DAC I BIT 2	DAC I BIT 1	DAC I BIT 0
CONTROL A (CAR)	0	0	0	1	1	0	0	0	TMS1	TMS0	Fast Decay test mode 0=ENABLE	HEAD AMP 1=BYPASS 0=NORMAL	HYS COMP OUTPUT 1=UNUSED 0=NORMAL	RDI/RDI2 1 = INPUT 0 = DISABLE	AGC HIGH GAIN START 1=ENABLE	GAIN STAGE INTERLOCK 1=ON 0=OFF
CONTROL B (CBR)	0	0	1	0	1	0	0	0	TW1	TW0	SLICE OFFSET PPM 1=ENABLE 0=DISABLE	SLICE OFFSET PWM 1=ENABLE 0=DISABLE	SLICE OFFSET PWM POLARITY 1=POSITIVE 0=NEGATIVE	PPOL SEL 1=DIFF 0=NORMAL	PPOL NORMAL SELECT 1=PWM 0=PPM	PPOL OUTPUT 1=HI-Z 0=ENABLE
CONTROL C (CCR)	0	0	1	1	1	0	0	0	PPM/PWM 1=PPM 0=PWM	TBG 1=BYPASS 0=NORMAL	FOUT 1=HI-Z 0=ENABLE	EXT TBG 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	TBG KD 1=3 x KD 0=1 x KD
CONTROL D (CDR)	0	1	0	0	1	0	0	0	TPS2	TPS1	TPS0	MTPE 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	GAIN SHFT 1 = ON 0 = OFF
N COUNTER (NCR)	0	0	0	0	1	0	1	0	--	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER (MCR)	0	0	0	1	1	0	1	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
WINDOW SHIFT (WSCR)	0	0	1	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
WINDOW SHIFT 2 (WSCR 2)	0	0	1	1	1	0	1	0	MOEQ POLARITY 1=NEGATIVE 0=POSITIVE	RG POLARITY 1=NEGATIVE 0=POSITIVE	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$

REGISTER DESCRIPTION

Control registers CAR, CBR, CCR and CDR allow the user to configure the SSI 33P3701 test points for evaluation of different internal signals and also control other device functions. CAR and CBR control functions of the front-end section. CCR controls functions of the time base generator. CDR controls test points and functions of the data separator. The bits of the CA, CB, CC and CD registers are defined as follows:

CONTROL REGISTER CA

BIT	NAME	DESCRIPTION
0	GSI	Enable PWM qualifier Gain Stage Interlock to LEVEL pin voltage
1	AHGS	Enable AGC High Gain Start at the transition from emboss to MO mode
2	RDI	RDI pin input control
3	HCO	Hysteresis Comparator Output control
4	BYPHA	Bypass Head Amp function
5	FDTM	Constant fast decay current test mode
6	TMS0	Control bit for Test Mode Selection (see Table 4)
7	TMS1	Control bit for Test Mode Selection (see Table 4)

CONTROL REGISTER CB

0	PO	PPOL Outout control
1	PNS	PPOL Normal Selection (PPM / PWM)
2	PS	PPOL Selection (Normal / Differentiated)
3	SOPP	Slice Offset Polarity control PWM comparator
4	ESOW	Enable Slice Offset of PWM comparator
5	ESOP	Enable Slice Offset of PPM comparator for normal signal
6	TW0	Control bit for selecting Test Write outputs (TWOP/TWON) source (see Table 5)
7	TW1	Control bit for selecting Test Write outputs (TWOP/TWON) source (see Table 5)

CONTROL REGISTER CC

0	TKD	Time Base Generator phase detector gain (KD) control
1	EPDT	Enable Phase Detector (Time Base Generator)
2	UT	Pump Up (TFLT sources current, $\overline{\text{TFLT}}$ sinks Current)
3	DT	Pump Down (TFLT sinks current, $\overline{\text{TFLT}}$ sources Current)
4	EET	Enable External Time Base Generator
5	FOC	FOUT pin control
6	BYPT	Bypass Time Base Generator Circuit Function
7	PPWM	Select the function for PPM signal or PWM signal

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REGISTER DESCRIPTION (continued)

CONTROL REGISTER CD

BIT	NAME	DESCRIPTION
0	GS	Enable phase detector Gain Switching
1	EPDD	Enable Phase Detector (Data Synchronizer)
2	UT	Pump Up (DFLT sources current, $\overline{\text{DFLT}}$ sinks current)
3	DT	Pump Down (DFLT sinks current, $\overline{\text{DFLT}}$ sources current)
4	MTPE	Monitor Test Point Enable
5	TPS0	Control bit for selecting Test Point Source (see Table 6)
6	TPS1	Control bit for selecting Test Point Source (see Table 6)
7	TPS2	Control bit for selecting Test Point Source (see Table 6)

TABLE 4: Multiplexed Test Mode Selection
MIP/MIN are used as inputs, FNP/FNN are used as outputs.

TMS1	TMS0	MODE
0	0	Normal Operation
0	1	Bypass ATT and Sag Canceller for AGC loop testing
1	0	Bypass ATT, Sag Canceller and AGC for Filter testing
1	1	Bypass ATT, Sag Canceller and Filter for AGC testing

TABLE 5: Multiplexed Test Write Output (TWO) Signal Selection
This output enabled when SHG=low.

TW1	TW0	MODE
0	0	Monitor the asymmetry compensation input
0	1	Monitor the asymmetry compensation output
1	0	Monitor the gain stage output of the asymmetry compensation
1	1	Enable Test Write mode and monitor Test Write signal (MOEG=low)

TABLE 6: Multiplexed Test Point Signal Selection

MTPE	TPS2	TPS1	TPS0	MTP1	MTP2
0	X	X	X	OFF	OFF
1	0	0	0	SET	RESET
1	0	0	1	RD1	RD2
1	0	1	0	COUT	COUT2
1	0	1	1	NCTR	—
1	1	0	0	VCOREF	$\overline{\text{DRD}}$
1	1	0	1	DSREF	$\overline{\text{DRD2}}$

SET	Output of the positive threshold comparator
RESET	Output of the negative threshold comparator
RD1 / RD2	Output of the pulse qualifier
COUT	Output of the PPM pulse qualifier clock circuit
COUT2	Output of the PWM slice comparator circuit
VCOREF	Output of the data synchronizer PLL
DSREF	Output of the time base generator
$\overline{DRD}$	Delayed $\overline{RD}$ (when RG is high) (Note: output is DSREF when RG is low)
$\overline{DRD2}$	Delayed $\overline{RD2}$ (when RG is high and PWM mode)
NCTR	N counter output of the time base generator, frequency is FREF/(N+1)

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift Control Register (WSCR/WSCR2). WSCR2 is for the second data synchronizer in PWM read mode. The WS register bits are as follows: (Note: WSCR2 Bit 6, 7 don't relate to window shift control)

WSCR

BIT	NAME	FUNCTION
0	$\overline{WS0}$	Bit for window shift magnitude (see Table 7)
1	$\overline{WS1}$	Bit for window shift magnitude (see Table 7)
2	$\overline{WS2}$	Bit for window shift magnitude (see Table 7)
3	$\overline{WS3}$	Bit for window shift magnitude (see Table 7)
4	WSD	Window shift direction. 0 = early, 1 = late
5	WSE	Window shift enable
6	TDAC0	Control bit for DACOUT signal selection (see Table 8)
7	TDAC1	Control bit for DACOUT signal selection (see Table 8)

WSCR2

0	$\overline{WS0}$	Bit for window shift magnitude (see Table 7)
1	$\overline{WS1}$	Bit for window shift magnitude (see Table 7)
2	$\overline{WS2}$	Bit for window shift magnitude (see Table 7)
3	$\overline{WS3}$	Bit for window shift magnitude (see Table 7)
4	WSD	Window shift direction. 0 = early, 1 = late
5	WSE	Window shift enable

REGISTER DESCRIPTION (continued)

*The window shift magnitude is set as a percentage of the full decode window, in 2% steps. This results in a window shift capability of ±30% of the full decode window. The tolerance of the window shift magnitude is TWS ± 20% ± 1ns, where TWS is the ideal shift magnitude value(ns). Window shift should be set during idle mode.

TABLE 7: Window Shift Magnitude Selection

WS3*	WS2*	WS1*	WS0*	SHIFT MAGNITUDE
1	1	1	1	No shift
1	1	1	0	2% (minimum shift)
1	1	0	1	4%
1	1	0	0	6%
1	0	1	1	8%
1	0	1	0	10%
1	0	0	1	12%
1	0	0	0	14%
0	1	1	1	16%
0	1	1	0	18%
0	1	0	1	20%
0	1	0	0	22%
0	0	1	1	24%
0	0	1	0	26%
0	0	0	1	28%
0	0	0	0	30% (maximum shift)

TABLE 8: DACOUT Test Point Signal Selection

TDAC1	TDAC0	DAC MONITORED
0	0	Filter fc DAC
0	1	Qualifier threshold DAC (VTH)
1	0	Window shift DAC
1	1	Window shift 2 DAC

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data synchronizer PLL analog power supply pin
VPB	-	Time base generator PLL analog power supply pin
VPC	-	Internal ECL, CMOS logic power supply pin
VPD, VPD2	-	CMOS and Pseudo CMOS buffer I/O digital power supply pin
VPG	-	Head amp, attenuator, pulse detector, filter, analog power supply pin
VNA	-	Data Synchronizer PLL analog ground pin
VNB	-	Time base generator PLL analog ground pin
VNC	-	Internal ECL, CMOS logic ground pin
VND, VND2	-	CMOS and pseudo CMOS buffer I/O digital ground pin
VNG	-	Head amp, attenuator, pulse detector, filter, analog ground pin

INPUT PINS

MIP, MIN	I	MO SIGNAL INPUTS: Differential MO signal attenuator input pins.
EIP, EIN	I	EMBOSS SIGNAL INPUTS: Differential emboss signal attenuator input pins when PDCR bit 1 is high. Also sum and differential head amplifier input pins when PDCR bit 1 is low.
SLP, SLN	I	ANALOG INPUTS FOR QUALIFIER: Differential analog inputs to the slice comparator.
QUIP, QUIN	I	ANALOG INPUTS FOR QUALIFIER: Differential analog inputs to the hysteresis and zero cross comparator and full wave rectifier.
$\overline{\text{LOW\_Z}}$	I	LOW IMPEDANCE ENABLE: TTL compatible input pin that activates the Low-Z switches. A low level activates the switches, and the falling edge of the internal LOW_Z triggers the fast decay circuit. The signal following an input stage is muted during Low-Z mode (low).
PWRON	I	POWER ENABLE: TTL compatible power control input. A high level TTL input enables power to circuitry according to the contents of the PDCR. A low level TTL input shuts down all circuitry.
HOLD	I	HOLD CONTROL: TTL compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. FREF pin has an internal pull-down resistor.
FREF2, $\overline{\text{FREF2}}$	I	REFERENCE FREQUENCY INPUTS: Pseudo ECL. A differential reference frequency of the external time base generator must be decoupled into these pins.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RDI, RDI2	I	READ DATA INPUT: TTL compatible inputs. RDI is provided as read data input to the data synchronizer from an external qualification circuit. RDI is available when CAR bit 2 goes high. RDI2 is for the second data synchronizer.
RG	I	READ GATE: TTL compatible read gate input. When WSCR2 bit 6 is low, a high level selects the RD input and enables the read mode and activates SDO output. The polarity is reversed when WSCR2 bit 6 goes high.
MOEG	I	MO/EMBOSS GATE: TTL compatible MO/emboss gate inputs. When WSCR2 bit 7 is low, a high level activates the emboss mode by selecting emboss control registers and the BYPE capacitor. The polarity is reversed when WSCR2 bit 7 goes high.
SHG	I	SAMPLE HOLD GATE: TTL compatible Sample/Hold gate input. A low level TTL input enables TWO output. A high level disables TWO output and holds the output level when a capacitor is connected between TWO and VPG.

OUTPUT PINS

MTP1, 2	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CDR bit 4-7. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO, SDO2	O	SYNCHRONIZED READ DATA: Pseudo CMOS output pins. Read MO/ emboss data output when RG is high. SDO2 is enabled in PWM mode only.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals.
RRC, RRC2	O	READ REFERENCE CLOCK: Read clock pseudo CMOS outputs. When RG goes low, RRC/RRC2 are disabled. After RG goes high, RRC/RRC2 are enabled as a clock synchronized to the read data when the internal VCO lock signal is asserted. RRC2 is enabled in PWM mode only.
AMOP, AMON	O	ATTENUATOR MO OUTPUTS: Differential attenuator output pins through the sag canceller for MO signal. These outputs are AC coupled into the sag canceller feedback pins (SMFP/SMFN).
AEOP, AEON	O	ATTENUATOR EMBOSS OUTPUTS: Differential attenuator output pins through the sag canceller for emboss signal. These outputs are AC coupled into the sag canceller feedback pins (SEFP/SEFN).
TWO	O	TEST WRITE OUTPUT: Test write signal output pin when CBR bit 6 and 7 are high. This pin also monitors three asymmetry compensation signals through other settings of CBR bit 6 and bit 7 (see Table 5).
FOUT	O	TIME BASE GENERATOR VCO OUTPUT: Pseudo CMOS output pin. This clock signal is the data synchronizer PLL reference.
PPOL	O	PULSE POLARITY: Pulse polarity pseudo CMOS output pin. The output is high when the input signal is over the threshold level. This output signal can select either input signal normal or differentiated by CBR bit 2. When the CBR bit 2 is low, the normal signal is selected. CBR bit 1 selects which qualifier, PPM or PWM, is used for the normal signal. When the CBR bit 0 goes high, PPOL will be held High-Z.

ANALOG PINS

NAME	TYPE	DESCRIPTION
CMP, CMN	-	MO AC POLE CAP: These pins are the connection points for the sag canceller AC pole capacitor. This holds the DC offset component of the sag canceller during MO mode.
CEP, CEN	-	EMBOSS AC POLE CAP: These pins are the connection points for the sag canceller AC pole capacitor. This holds the DC offset component of the sag canceller during emboss mode.
SMFP, SMFN	-	SAG CANCELLER FEEDBACK: Differential feedback pins of the sag canceller for MO signal. These pins are AC coupled from the attenuator outputs (AMOP/AMON).
SEFP, SEFN	-	SAG CANCELLER FEEDBACK: Differential feedback pins of the sag canceller for emboss signal. These pins are AC coupled from the attenuator outputs (AEOP/AEON).
BYPMO	-	The AGC read mode integration capacitor, CBYPMO, is connected between BYPMO and VPG.
BYPE	-	The AGC emboss read mode integration capacitor, CBYPE, is connected between BYPE and VPG.
CS1P, CS1N	-	LPF CAP: These pins are the connection points for the second order LPF capacitor of the PWM qualifier. The cut off frequency is determined by this capacitor with an internal resistor.
CS2P, CS2N	-	LPF CAP: These pins are the other connection points for the second order LPF capacitor of the PWM qualifier. The cut off frequency is determined by this capacitor with an internal resistor.
RSP, RSN	-	GAIN RESISTOR: These pins are the connection points for the external resistor which determines the gain of the PWM qualifier gain stage.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the output of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register (see Table 8).
TFLT, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DFLT, $\overline{\text{DFLT}}$, $\overline{\text{DFLTA}}$	-	PLL LOOP FILTER: These pins are the connection points for the data synchronizer loop filter. When CCR bit 7 is low (PWM mode), $\overline{\text{DFLTA}}$ is connected internally to $\overline{\text{DFLT}}$. When CCR bit 7 is high (PPM mode), $\overline{\text{DFLTA}}$ is disconnected internally to $\overline{\text{DFLT}}$.
DFLT2, $\overline{\text{DFLT2}}$	-	PLL LOOP FILTER: These pins are the connection points for the second data synchronizer in PWM mode.

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
LEVEL, LEVEL 2	-	NPN emitter outputs that provide a full wave rectified signal from QUIP/QUIN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with the internal current DAC, (DACL). The internal sink current of LEVEL 2 is fixed.
VRC	-	REFERENCE VOLTAGE OUTPUT: This pin provides the internal DC bias reference voltage.
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data synchronizer and time base generator.
RX	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

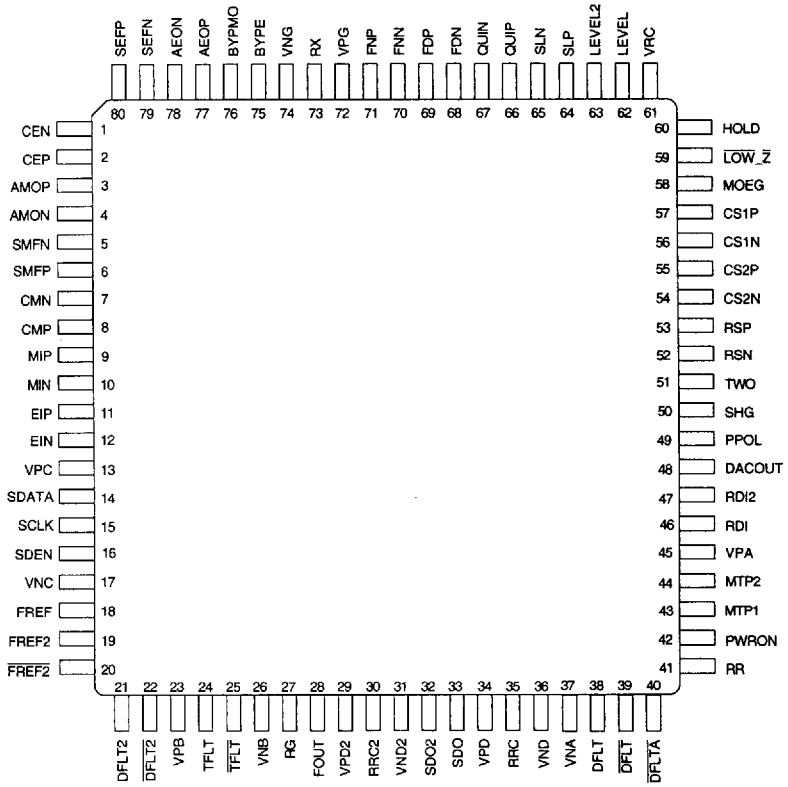
SDEN	I	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDATA	I/O	SERIAL DATA: Serial data bidirectional CMOS compatible pin. NRZ programming data for the internal registers is applied to this input when the first bit is 0. When the first bit is 1, the address register data will be clocked out on the rising edge of SCLK.
SCLK	I	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

PACKAGE PIN DESIGNATIONS

(Top view)

THERMAL CHARACTERISTICS: θjA

80-lead TQFP	° C/W



80-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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