P54/74FCT191T/AT/CT
UP-DOWN BINARY COUNTERS

FEATURES

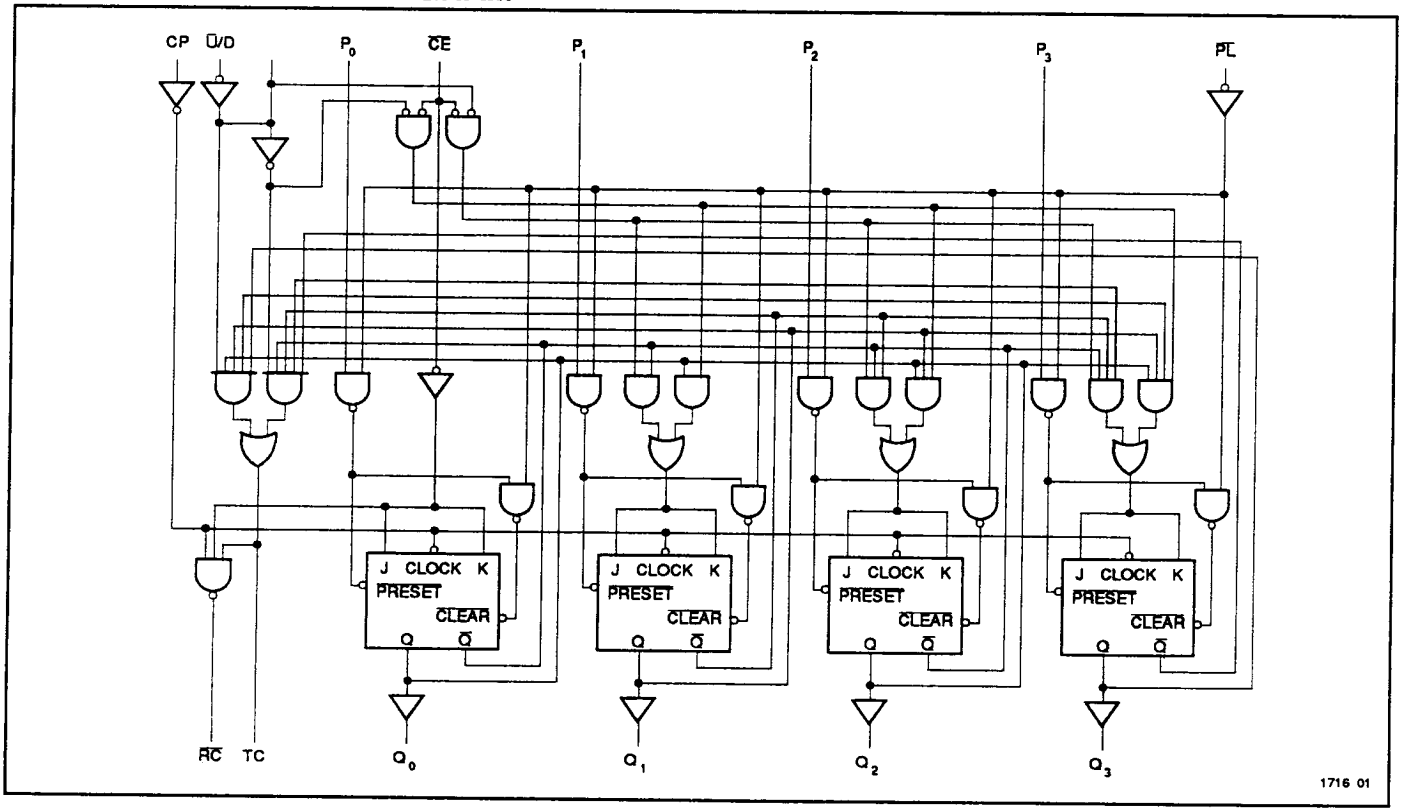
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 6.2ns max. (Com'l) FCT-A speed at 7.8ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **3-State Outputs**
- **Manufactured in 0.7 micron PACE Technology™**

DESCRIPTION

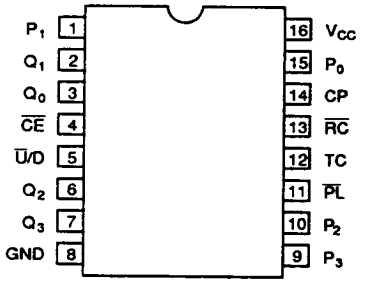
The 'FCT191T are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting. The preset allows the 'FCT191T to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

The 'FCT191T are manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

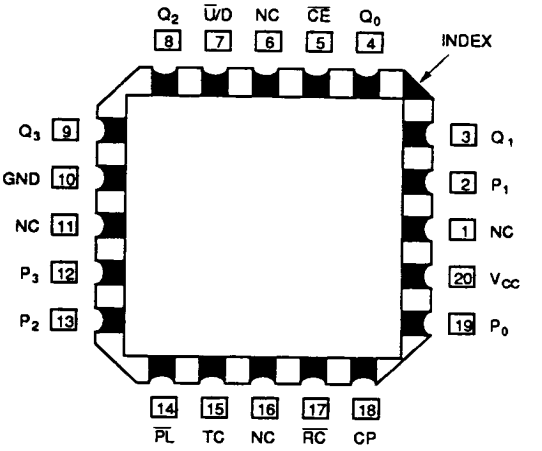
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P10, D10)
SOIC (S10)



LCC (L2)

1716 02

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

1716 Tbl 01

$\overline{RC}$ FUNCTION TABLE[2]

Inputs		Outputs	
$\overline{CE}$	CP	TC[1]	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

1716 Tbl 02

MODE SELECT FUNCTION TABLE[2]

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

1716 Tbl 03

Notes:
1. TC is generated internally.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care, ⌐ = LOW-to-HIGH clock transition.

2/13/92 - 8

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1716 Tbl 04

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1716 Tbl 05

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1716 Tbl 06

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1716 Tbl 07

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$

1716 Tbl 08

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions[6]
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, Preset Mode, 50% Duty Cycle, Outputs Open, $\overline{MR}$ = V_{CC} = $\overline{SR}$, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.0	2.8	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = V_{CC}, V_{IN} = GND
		1.2	3.8	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = 3.4V, V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = V_{CC}, V_{IN} = GND,
		4.2	10.5[4]	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = 3.4V or V_{IN} =GND

1716 Tbl 09

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

2/13/92 - 8

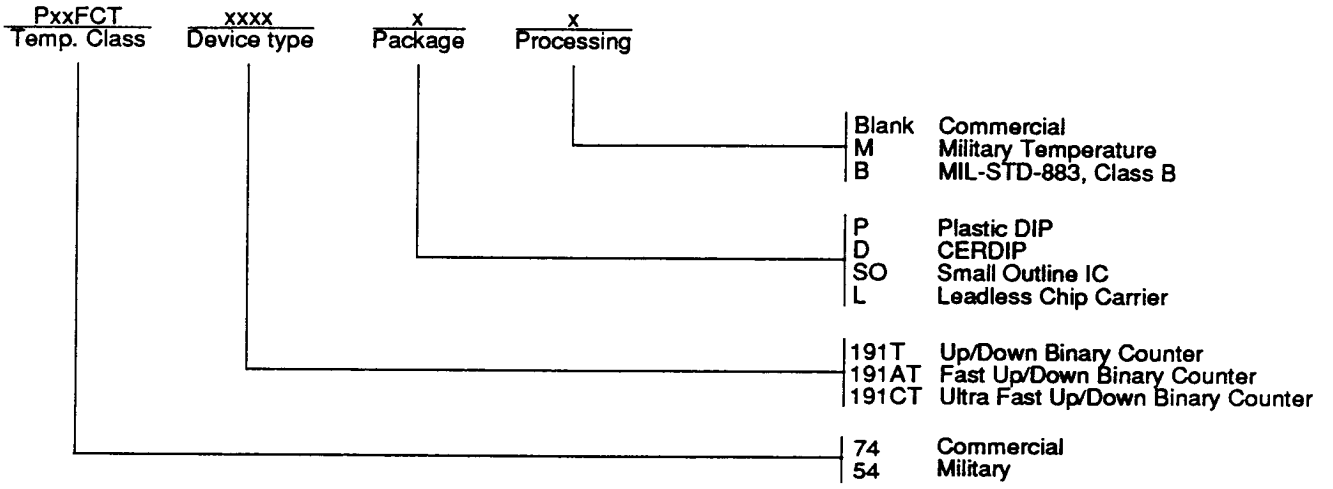
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Sym.	Parameter	Test Condition[1]	'FCT191T				'FCT191AT				'FCT191CT				Units
			MIL		COM'L		MIL		COM'L		MIL		COM'L		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	1.5	16.0	2.5	12.0	1.5	10.5	2.5	7.8	1.5	8.4	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		2.0	16.0	3.0	14.0	2.0	12.2	3.0	11.8	1.5	9.8	1.5	9.4	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		1.5	12.5	2.5	8.5	1.5	10.0	2.5	8.5	1.5	7.9	1.5	6.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.5	2.0	8.0	2.0	8.0	2.0	7.2	1.5	6.4	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		4.0	22.5	4.0	20.0	4.0	14.7	4.0	13.0	2.5	11.7	2.5	11.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC		3.0	13.0	3.0	11.0	3.0	8.5	3.0	7.2	1.5	6.8	1.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		1.5	16.0	2.0	14.0	1.5	10.4	2.0	9.1	1.5	8.3	1.5	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		3.0	14.0	3.0	13.0	3.0	9.1	3.0	8.5	2.0	7.3	2.0	7.2	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		6.0		5.0		5.0		4.0		4.0		3.5		
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5		1.5		1.5		1.5		1.5		1.0		ns
t_{SU}	Set-up Time LOW $\overline{CE}$ to CP		10.5		10.0		9.5		9.0		7.6		7.2		ns
t_H	Hold Time LOW $\overline{CE}$ to CP		0		0		0		0		0		0		ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{U}$/D to CP		12.0		12.0		10.0		10.0		8.5		8.0		ns
t_H	Hold Time, HIGH or LOW $\overline{U}$/D to CP		0		0		0		0		0		0		ns
t_W	$\overline{PL}$ Pulse Width LOW		8.5		6.0		8.0		5.5		6.0		5.0		ns
t_W	Clock Pulse Width HIGH or LOW		7.0		5.0		6.0		4.0[3]		5.0		4.0[3]		ns
t_{REM}	Recovery Time $\overline{PL}$ to CP		7.5		6.0		6.5		5.0		5.0		4.5		ns

1716 Tbl 10

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

ORDERING INFORMATION



1716 03