

**Dual P-Channel High Density Trench MOSFET**
**◆ DESCRIPTION**

The MT4953 uses advanced technology to provide excellent  $R_{DS(ON)}$ , low switching loss and reasonable price.

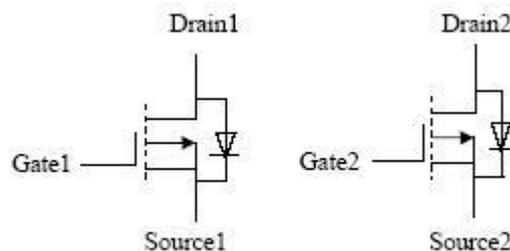
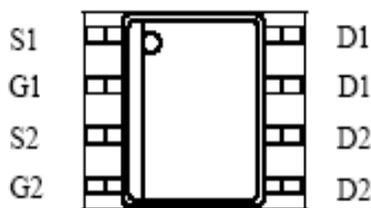
This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**◆ FEATURES**

- -30V/-4.9A,  $R_{DS(ON)} = 65m\Omega @ V_{GS} = -10V$
- -30V/-3.6A,  $R_{DS(ON)} = 105m\Omega @ V_{GS} = -4.5V$
- Super high dense cell trench design for low  $R_{DS(ON)}$
- Rugged and reliable
- SOP-8 package design

**◆ APPLICATIONS**

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- LCD Display

**◆ PIN CONFIGURATION**


**Dual P-Channel High Density Trench MOSFET**
**◆ ABSOLUTE MAXIMUM RATINGS**

(T<sub>A</sub>=25 °C Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V <sub>DS</sub>	-30	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	V
Drain Current	Continuous <sup>(1)</sup>	I <sub>D</sub>	-4.9	A
	Pulse <sup>(2)</sup>	I <sub>DM</sub>	-20	
Drain-Source Diode Forward Current <sup>(1)</sup>		I <sub>S</sub>	-1.7	A
Maximum Power Dissipation <sup>(1)</sup>		P <sub>D</sub>	2.0	W
Operating junction temperature range		T <sub>J</sub>	150	°C
Storage temperature range		T <sub>STG</sub>	- 55 to 150	°C

**◆ THERMAL RESISTANCE RATINGS**

Thermal Resistance	Symbol	Maximum	Unit
Junction-to-Ambient	R <sub>θJA</sub>	78	°C/W

Note :

1. Surface Mounted on FR4 Board , t ≤ 10sec
2. Pulse Test : Pulse width ≤ 300us , Duty Cycle ≤ 2%

**Dual P-Channel High Density Trench MOSFET**
**◆ ELECTRICAL CHARACTERISTICS**

 (T<sub>A</sub>=25 °C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0 V	-	-	-1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ± 20V,	-	-	±100	nA
<b>On Characteristics <sup>(1)</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA	-1.2	-1.8	-2.4	V
Drain-Source On State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -4.9A	-	42	65	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3.6A	-	67	105	
<b>Drain-Source Diode Characteristics <sup>(1)</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = -1.0A, V <sub>GS</sub> = 0V	-	-	-1.0	V
<b>Dynamic Parameters <sup>(2)</sup></b>						
Input Cap.	C <sub>iss</sub>	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V f = 1MHz	-	970	-	pF
Output Cap.	C <sub>oss</sub>		-	170	-	
Reverse Transfer Cap.	C <sub>rss</sub>		-	120	-	
<b>Switching Parameters <sup>(2)</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A	-	18.20	-	nC
		V <sub>DS</sub> = -15V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1A	-	9.20	-	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A	-	2.64	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	3.52	-	
Turn-On Time	T <sub>D(on)</sub>	V <sub>DS</sub> = -15V, R <sub>L</sub> = 15Ω I <sub>D</sub> = -1A, V <sub>GEN</sub> = -10V, R <sub>G</sub> = 10Ω	-	5.36	-	nS
	T <sub>r</sub>		-	7.76	-	
Turn-Off Time	T <sub>D(off)</sub>		-	15.84	-	
	T <sub>f</sub>		-	9.84	-	

Note :

1. Pulse Test : Pulse width ≤ 300us , Duty Cycle ≤ 2%
2. Guaranteed by design, not subject to production testing

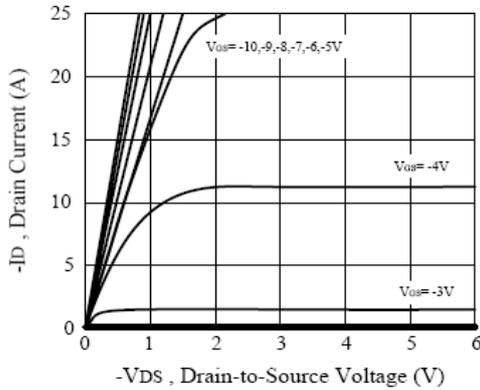
**Dual P-Channel High Density Trench MOSFET**
**◆ TYPICAL CHARACTERISTICS**


Figure 1. Output Characteristics

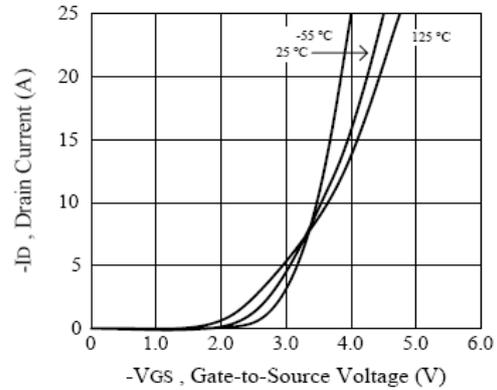


Figure 2. Transfer Characteristics

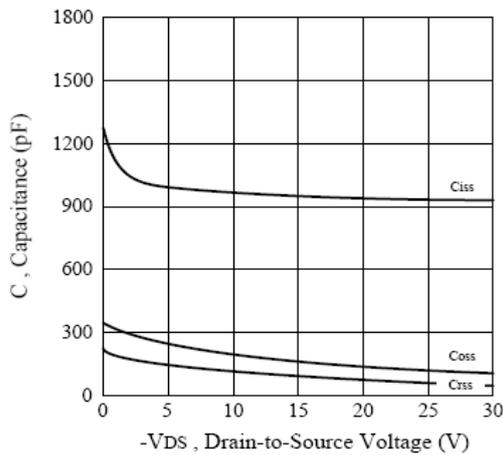


Figure 3. Capacitance

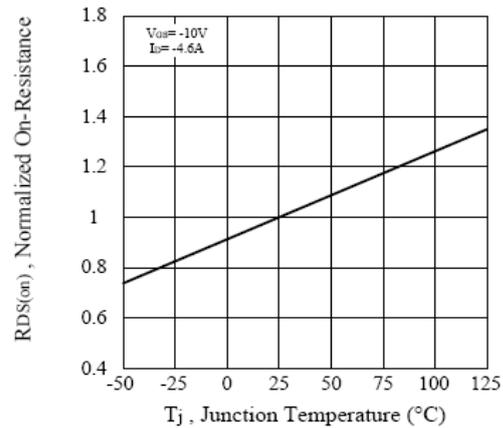


Figure 4. On-Resistance Variation with Temperature

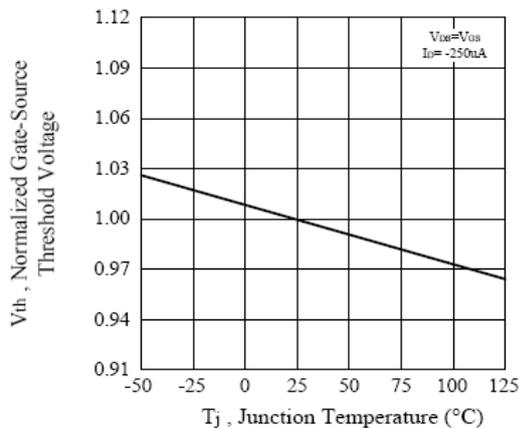


Figure 5. Gate Threshold Variation with Temperature

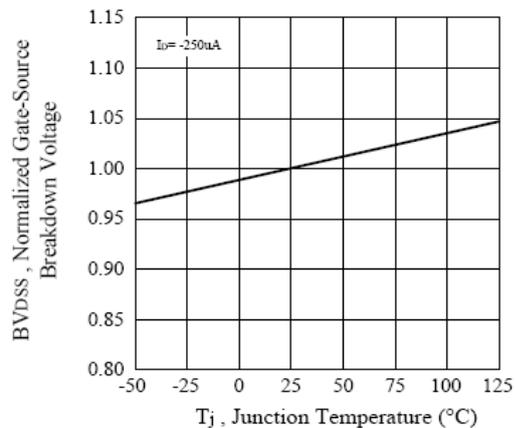


Figure 6. Breakdown Voltage Variation with Temperature

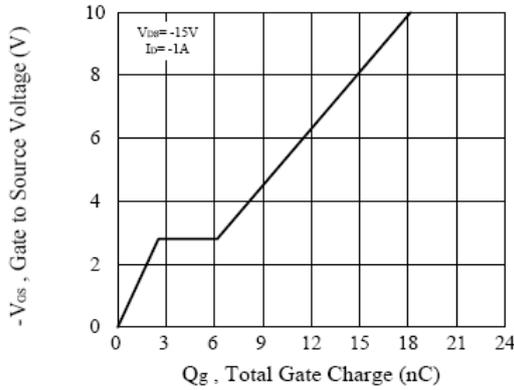
**◆ TYPICAL CHARACTERISTICS**


Figure 7. Gate Charge

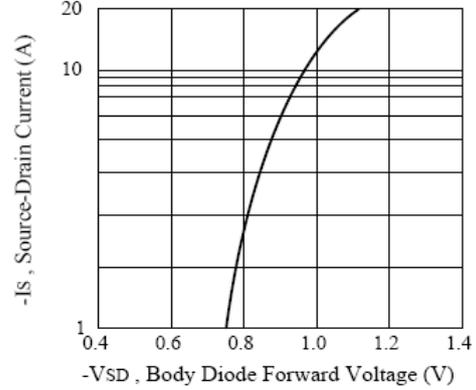


Figure 8. Body Diode Forward Voltage Variation with Source Current

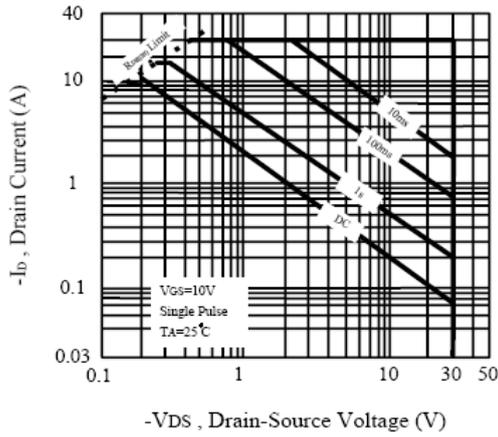


Figure 9. Maximum Safe Operating Area

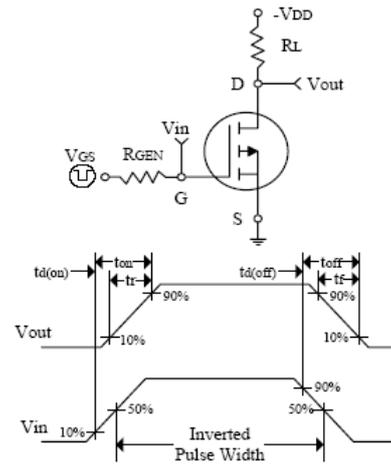


Figure 10. Switching Test Circuit and Switching Waveforms

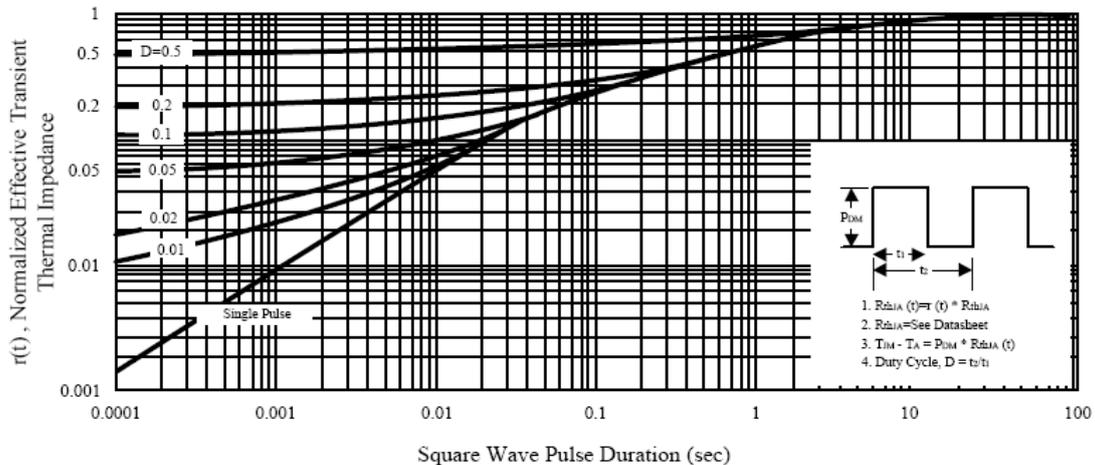


Figure 11. Normalized Thermal Transient Impedance Curve

**Dual P-Channel High Density Trench MOSFET**
**◆ PHYSICAL DIMENSIONS**
**8-Pin Plastic S.O.I.C.**
