International Rectifier

SERIES IRK.135, .136, .141, .142, .161, .162

SCR / SCR and SCR / DIODE

NEW INT-A-pak™ Power Modules

INTERNATIONAL RECTIFIER

135A
140A
160A

Features

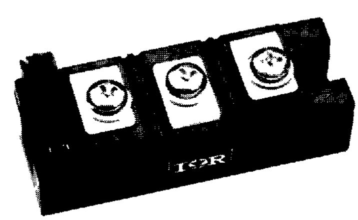
- High voltage
- Electrically isolated base plate
- 3000 V_{RMS} isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- Beryllium oxide substrate
- Also available with aluminum nitrade substrate

Description

This new IRK series of INT-A-paks modules uses high voltage power thyristors/ diodes in seven basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel.
These modules are intended for general purpose applications such as battery chargers, welders and plating equipment and where high voltage and high

Major Ratings and Characteristics

Parameters		IRK.135... IRK.136...	IRK.141... IRK.142...	IRK.161... IRK.162...	Units
$I_{T(AV)}$ @ 85°C		135	140	160	A
$I_{T(RMS)}$		300	310	355	A
I_{TSM}	@ 50Hz	3200	4750	5100	A
	@ 60Hz	3360	5000	5350	A
I^2t	@ 50Hz	51.5	113.0	131.0	kA^2s
	@ 60Hz	47.0	103.3	119.3	kA^2s
$I^2\sqrt{t}$		515.5	1130	1310	$kA^2\sqrt{s}$
V_{DRM} - V_{RRM}		Up to 1600	Up to 2000	Up to 1600	V
T_J		-40 to 130	-40 to 125		°C



ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{RRM} V_{DRM} maximum repetitive peak reverse and off-state blocking voltage V	V_{RSM}, maximum non-repetitive peak reverse voltage V	I_{RRM} I_{DRM} max @ 125°C mA
IRK.135- / IRK.136- IRK.141- / IRK.142- IRK.161- / IRK.162-	04	400	500	50
	06	600	700	50
	08	800	900	50
	10	1000	1100	50
	12	1200	1300	50
	14	1400	1500	50
	16	1600	1700	50
IRK.141- / IRK.142-	18	1800	1900	50
	20	2000	2100	50

On-state Conduction

	Parameters	IRK.135	IRK.141	IRK.161	Units	Conditions		
$I_{T(AV)}$	Maximum average on-state current	135	140	160	A	180° conduction, half sine wave		
	@ Case temperature	85	85	85	°C			
$I_{T(RMS)}$	Maximum RMS on-state current	300	310	355	A	as AC switch		
I_{TSM}	Maximum peak, one-cycle on-state, non-repetitive surge current	3200	4750	5100	A	t=10ms	No voltage	Sinusoidal half wave, initial $T_J = T_J$ max
		3360	5000	5350	A	t=8.3ms	reapplied	
		2700	4000	4300	A	t=10ms	100% V_{RRM}	
		2800	4200	4500	A	t=8.3ms	reapplied	
I^2t	Maximum I^2t for fusing	51.5	113.0	131.0	kA^2s	t=10ms	No voltage	Sinusoidal half wave, Initial $T_J = T_J$ max
		47.0	103.3	119.3	kA^2s	t=8.3ms	reapplied	
		36.5	80.0	92.5	kA^2s	t=10ms	100% V_{RRM}	
		33.3	73.0	84.4	kA^2s	t=8.3ms	reapplied	
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	515.5	1130	1310	$kA^2\sqrt{s}$	t=0.1 to 10ms, no voltage reapplied		
$V_{T(TO)1}$	Low level value of threshold voltage	0.98	1.14	0.88	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
$V_{T(TO)2}$	High level value of threshold voltage	1.01	1.19	1.12	V	$(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
r_{t1}	Low level on-state slope resistance	1.62	1.29	1.20	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
r_{t2}	High level on-state slope resistance	1.56	1.20	0.86	mΩ	$(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
V_{TM}	Maximum on-state voltage drop	1.66	1.70	1.50	V	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = T_J$ max., 180° conduction Av. power $= V_{T(TO)} \times I_{T(AV)} + r_f \times (I_{T(RMS)})^2$		
I_H	Maximum holding current	500	500	500	mA	Anode supply=12V, initial I_T=30A, T_J=25°C		
I_L	Maximum latching current	300	300	300	mA	Anode supply=12V, resistive load=1Ω gate pulse: 10V, 100µs, T_J=25°C		

Switching

		IRK.135	IRK.141	IRK.161	Units	Conditions	
t_d	Typical delay time	2.0	1.0	1.0	µs	T_J= 25°C	Gate Current=1A $dIg/_{dt}$=1A/µs
t_r	Typical rise time	3.0	2.0	2.0	µs	T_J= 25°C	Vd=0,67% V_{DRM}
t_q	Typical turn-off time	50 - 150			µs	I_{TM}=300 A ; -dI/dt=15 A/µs ; $T_J = T_J$ max ; Vr=50 V ; dV/dt = 20 V/µs ; Gate 0 V, 100 ohm	

Blocking

I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current	50	mA	$T_J = T_J$ max.
V_{INS}	RMS isolation voltage	3000	V	50Hz, circuit to base, all terminals shorted, t=1s
$dv/_{dt}$	Critical rate of rise of off-state voltage	500	V/µs	$T_J = T_J$ max, linear to 80% rated V_{DRM}
		1000	V/µs	$T_J = T_J$ max, linear to 67% rated V_{DRM}

Triggering

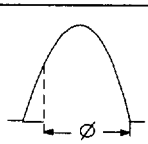
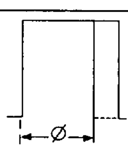
	Parameters	IRK.135	IRK.141	IRK.161	Units	Conditions	
P_{GM}	Maximum peak gate power	5.0	10.0	10.0	W	tp ≤ 5ms,	T_J = T_J max.
$P_{G(AV)}$	Maximum average gate power	1.0	2.0	2.0	W	f=50Hz,	T_J = T_J max.
$+I_{GM}$	Maximum peak gate current	2.0	3.0	3.0	A	tp ≤ 5ms,	T_J = T_J max.
$-V_{GT}$	Max. peak negative gate voltage	5.0	5.0	5.0	V	tp ≤ 5ms,	T_J = T_J max.
V_{GT}	Maximum required DC gate voltage to trigger	4.0 3.0 2.0	4.0 3.0 2.0	4.0 3.0 2.0	V V V	T_J=-40°C T_J= 25°C T_J= T_J max.	Anode supply = 12V, resistive load ; Ra = 1Ω
I_{GT}	Maximum required DC gate current to trigger	350 200 100	350 200 100	350 200 100	mA mA mA	T_J=-40°C T_J= 25°C T_J= T_J max.	Anode supply = 12V, resistive load ; Ra = 1Ω
V_{GD}	Maximum gate voltage that will not trigger	0.25	0.30	0.30	V	@ T_J= T_J max., rated V_{DRM} applied	
I_{GD}	Maximum gate current that will not trigger	10.0	10.0	10.0	mA	@ T_J= T_J max., rated V_{DRM} applied	
$di/_{dt}$	Max rate of rise of turned-on current	300	500	500	A/μs	@ T_J = T_J max., I_{TM} = 400 A rated V_{DRM} applied	

Thermal and Mechanical Specifications

		IRK.135	IRK.141	IRK.161	Units	Conditions
T_J	Junction operating temperature	-40 to 130	-40 to 125		°C	
T_{stg}	Storage temperature range	-40 to 150			°C	
R_{thJC}	Maximum thermal resistance junction to case	0.20	0.17	0.17	K/W	Per junction, DC operation
R_{thC-S}	Thermal resistance, case to heatsink	0.05	0.05	0.05	K/W	Mounting surface flat, smooth and greased (per module)
T Mounting tourque ±10%	INT-A-pak to heatsink	4 to 6			Nm	A mounting compound is recommended and the tourque should be rechecked after a period of about 3 hours to allow for the spread of the compound
	Busbar to INT-A-pak	4 to 6			Nm	
wt	Approximate weight	500 17.8			g oz	
	Case style	INT-A-pak				

ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

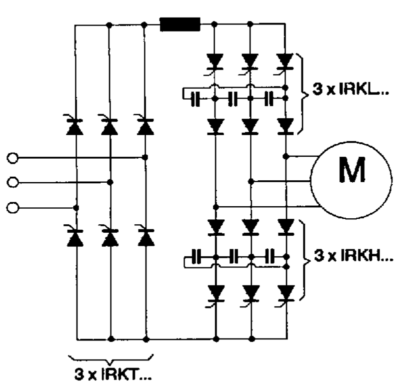
Conduction angle		IRK.135 IRK.136	IRK.141 IRK.142	IRK.161 IRK.162	Units	Conditions
	180°	0.016	0.016	0.015	K/W	T_J = T_J max.
	120°	0.019	0.019	0.019	K/W	
	90°	0.024	0.025	0.024	K/W	
	60°	0.035	0.036	0.036	K/W	
	30°	0.060	0.060	0.060	K/W	
	180°	0.011	0.012	0.012	K/W	T_J = T_J max.
	120°	0.019	0.020	0.020	K/W	
	90°	0.026	0.027	0.027	K/W	
	60°	0.037	0.037	0.037	K/W	
	30°	0.060	0.060	0.060	K/W	

INT-A-paks Suitable for Current Source Inverters

Thyristor		Diode	$I_{T(AV)}$ / $I_{F(AV)}$ @ T_C		
V_{DRM} V_{RRM}	V_{RSM}	V_{RRM} V_{RSM}	135A @ 85°C	140A @ 85°C	160A @ 85°C
1400	1500	2000	IRKH135-14D20	IRKH141-14D20	IRKH161-14D20
			IRKH136-14D20	IRKH142-14D20	IRKH162-14D20
1400	1500	2000	IRKL135-14D20	IRKL141-14D20	IRKL161-14D20
			IRKL136-14D20	IRKL142-14D20	IRKL162-14D20
1600	1700	2500	IRKH135-16D25	IRKH141-16D25	IRKH161-16D25
			IRKH136-16D25	IRKH142-16D25	IRKH162-16D25
1600	1700	2500	IRKL135-16D25	IRKL141-16D25	IRKL161-16D25
			IRKL136-16D25	IRKL142-16D25	IRKL162-16D25
1800	1900	2800	Not Available	IRKH141-18D28	Not Available
			Not Available	IRKH142-18D28	Not Available
1800	1900	2800	Not Available	IRKL141-18D28	Not Available
			Not Available	IRKL142-18D28	Not Available
2000	2100	3200	Not Available	IRKH141-20D32	Not Available
			Not Available	IRKH142-20D32	Not Available
2000	2100	3200	Not Available	IRKL141-20D32	Not Available
			Not Available	IRKL142-20D32	Not Available

For all other parameters and characteristics refer to standard IRKH... and IRKL... modules.

Application Notes



Current Source Inverter using 9 INT-A-paks

Current Source Inverters

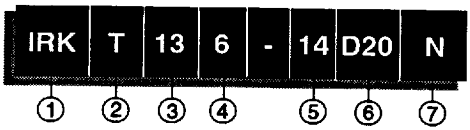
Current-Source Inverters (also known as Sequentially Commutated Inverters) use Phase Control (as opposed to Fast) Thyristors and Diodes.

The advantages of Current Source Inverters lie in their ease control, absence of large commutation inductances and limited fault currents.
Their simple construction, illustrated by the circuit on the left, is further enhanced by the use of INT-A-paks which allow the power circuit of an Inverter to be realised with 6 capacitors and 9 INT-A-paks all mounted on just one heatsink.

The optimal design of Current Source Inverters requires the use of Diodes with blocking voltages greater than those of the thyristors .
This departure from conventional half-bridge modules is catered for by INT-A-pak range with Thyristors up to 2000V and Diodes up to 3200V.

Ordering Information Table

Device Code

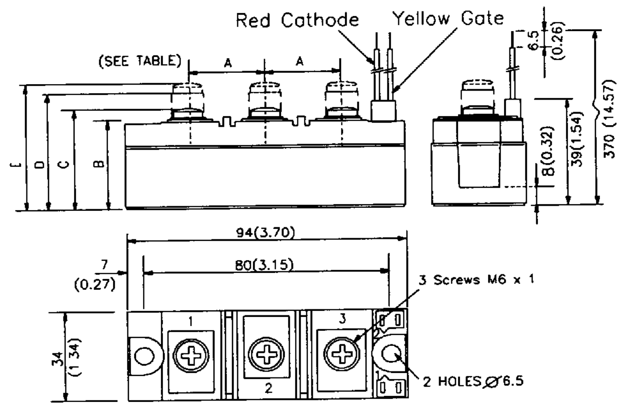


- **1** - Module type
- **2** - Circuit configuration (See Outline Table)
- **3** - Current rating: IT(AV) x 10 rounded
- **4** *-For IRK.13. only*:
  - 5 = option with spacers and longer terminal screws
  - 6 = option with standard terminal screws

  For IRK.14. and IRK.16. only:
  - 1 = option with spacers and longer terminal screws
  - 2 = option with standard terminal screws
- **5** - Voltage code: Code x 100 = V_{RRM} (See Voltage Ratings Table)
- **6** - Current Source Inverters types
- **7** - None= standard devices (beryllium oxide)

  N = aluminum nitrade substrate (contact factory)

Outline Table

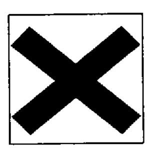


For all types	A	B	C	D	E
IRK...5	25(0.98)	----	----	41(1.61)	47(1.85)
IRK 6	23(0.91)	30(1.18)	36(1.42)	----	----

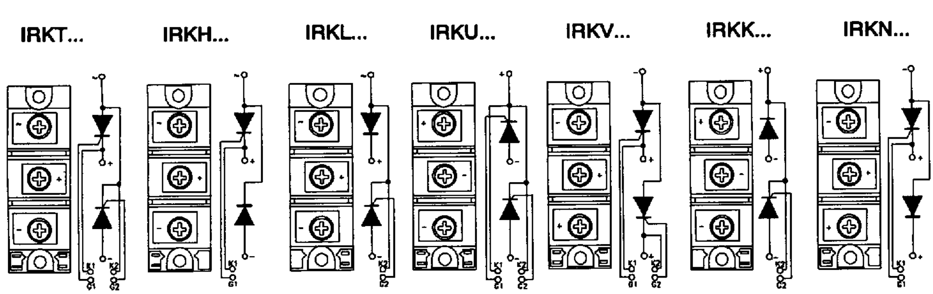
For all types	A	B	C	D	E
IRK .1	25(0.98)	----	----	41(1 61)	47(1.85)
IRK 2	23(0.91)	30(1.18)	36(1.42)	----	----

CONTAINS BERYLLIUM OXIDE CERAMIC

- May contain Beryllium Oxide Ceramic, and under normal circumstances is non hazardous.
- Do not open, cut or grind.
- Unserviceable parts must be disposed of as harmful waste.


HARMFUL

- **All dimensions in millimetres (inches)**
- **Dimensions are nominal**
- **Full engineering drawings are available on request**
- **UL identification number for gate and cathode wire: UL 1385**
- **UL identification number for package: UL 94V0**



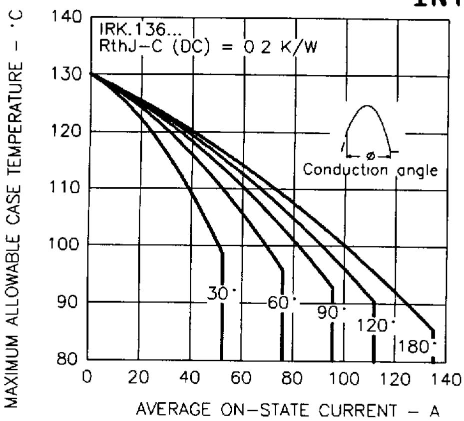


Fig. 1 - Current Ratings Characteristics

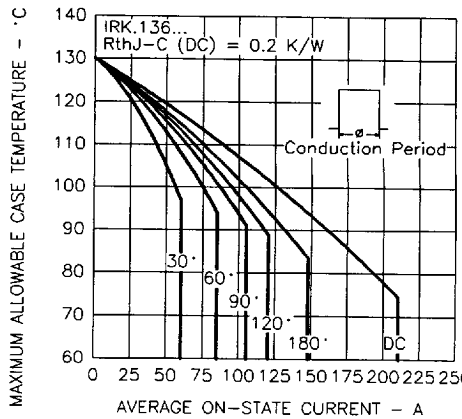


Fig. 2 - Current Ratings Characteristics

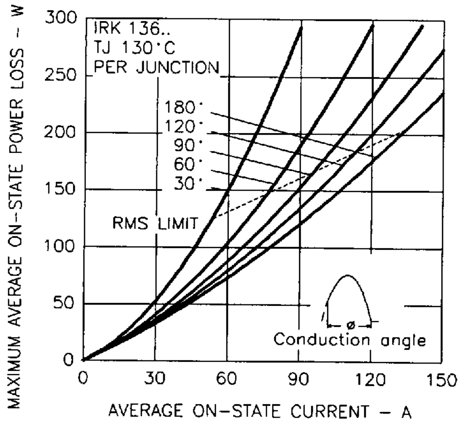


Fig. 3 - On-state Power Loss Characteristics

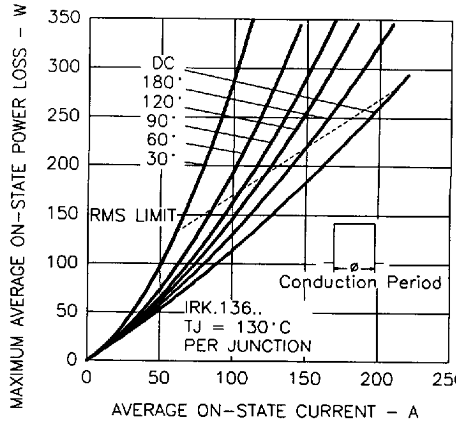


Fig. 4 - On-state Power Loss Characteristics

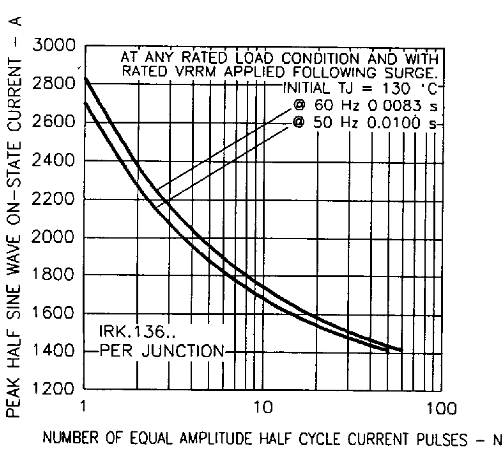


Fig. 5 - Maximum Non-Repetitive Surge Current

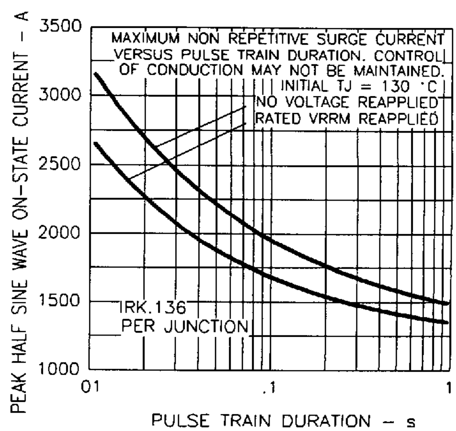


Fig. 6 - Maximum Non-Repetitive Surge Current

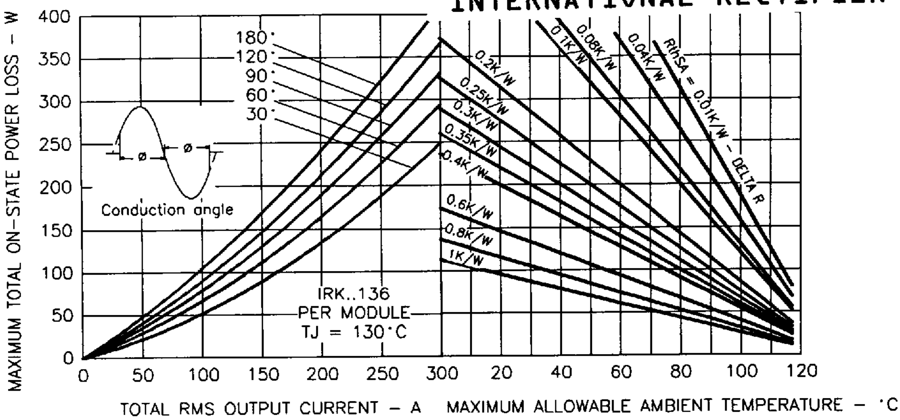


Fig. 7 - On-state Power Loss Characteristics

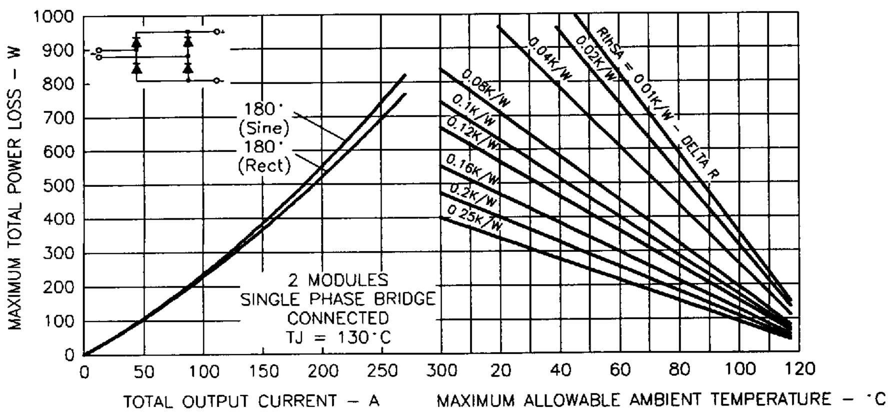


Fig. 8 - On-state Power Loss Characteristics

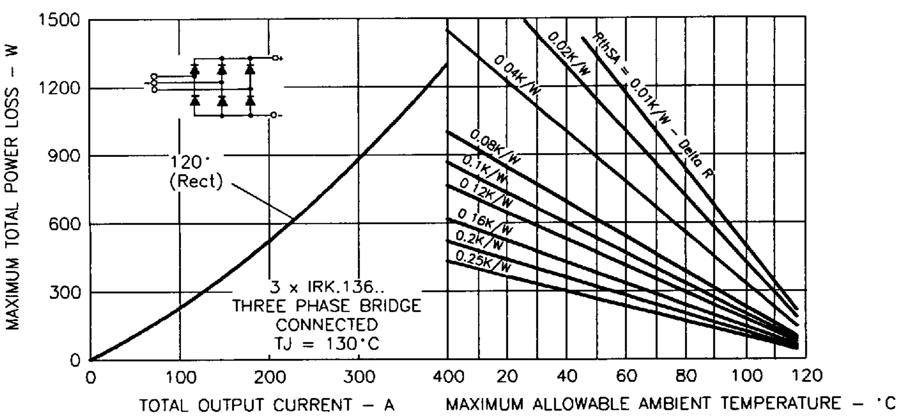


Fig. 9 - On-state Power Loss Characteristics

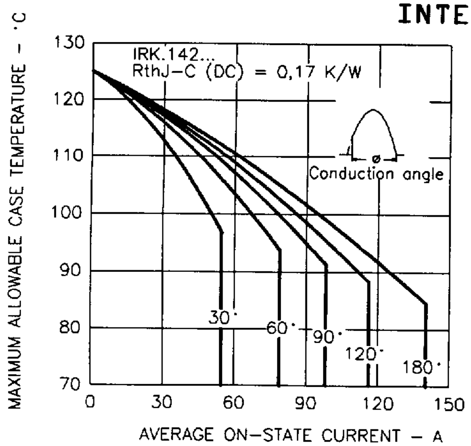


Fig. 10 - Current Ratings Characteristics

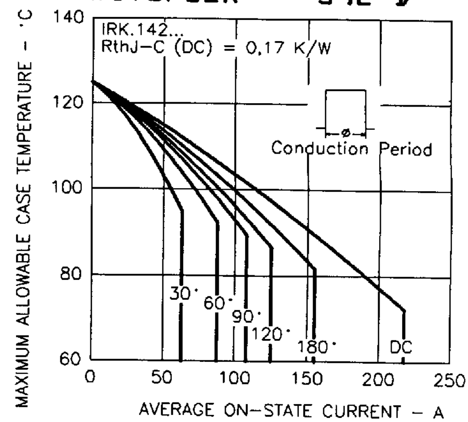


Fig. 11 - Current Ratings Characteristics

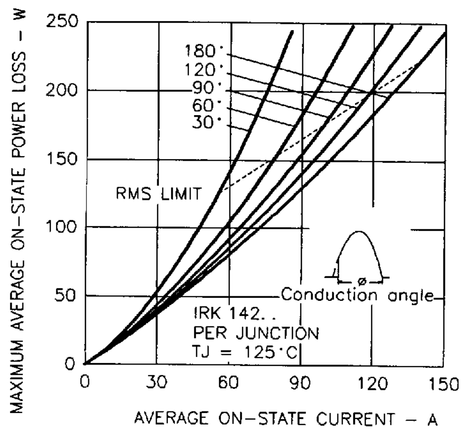


Fig. 12 - On-state Power Loss Characteristics

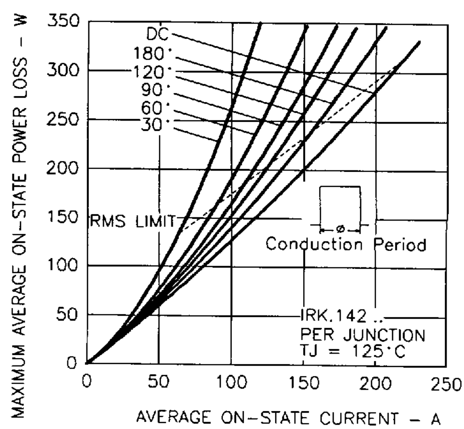


Fig. 13 - On-state Power Loss Characteristics

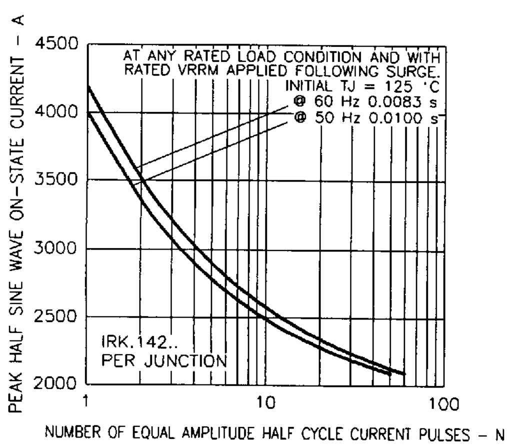


Fig. 14 - Maximum Non-Repetitive Surge Current

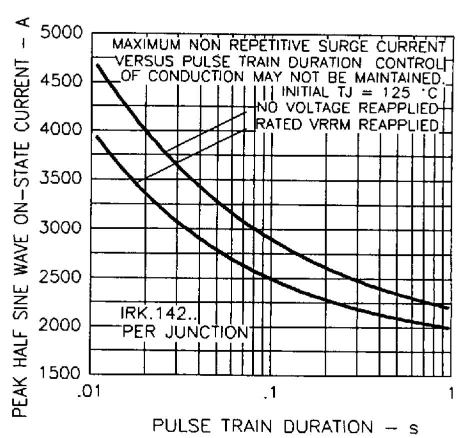


Fig. 15 - Maximum Non-Repetitive Surge Current

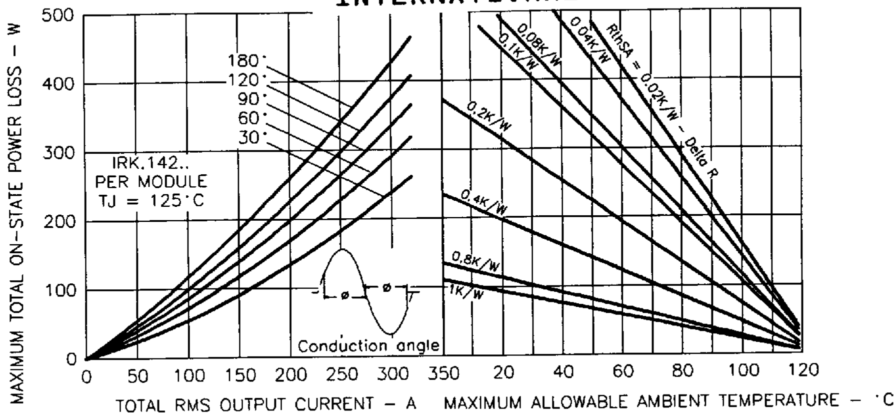


Fig. 16 - On-state Power Loss Characteristics

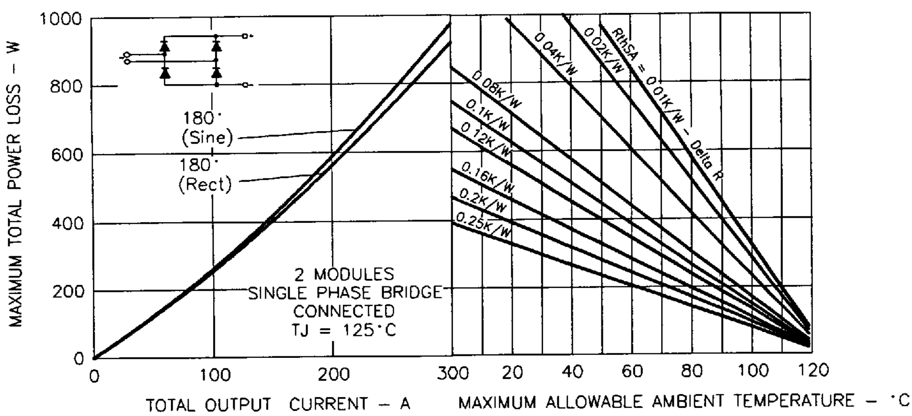


Fig. 17 - On-state Power Loss Characteristics

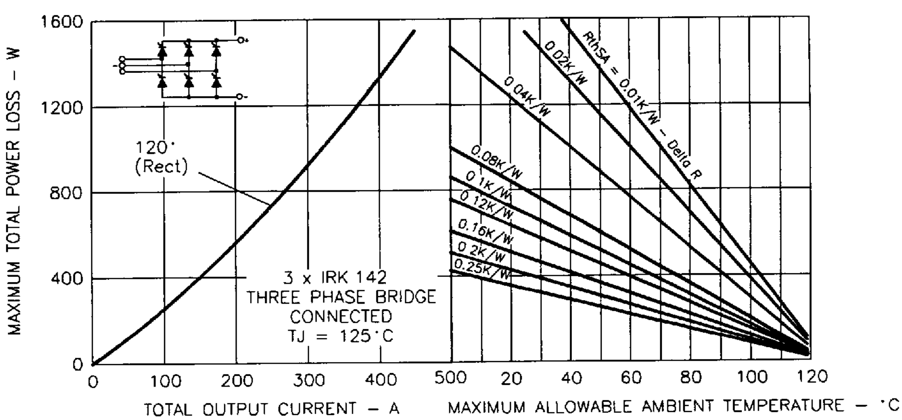


Fig. 18 - On-state Power Loss Characteristics

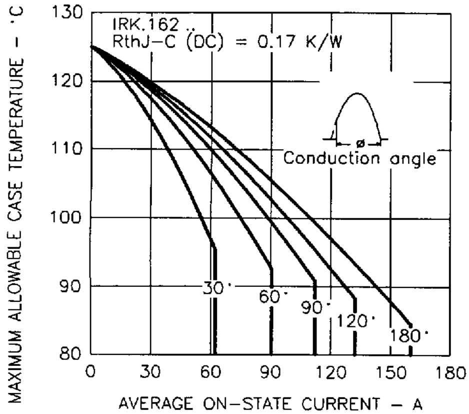


Fig. 19 - Current Ratings Characteristics

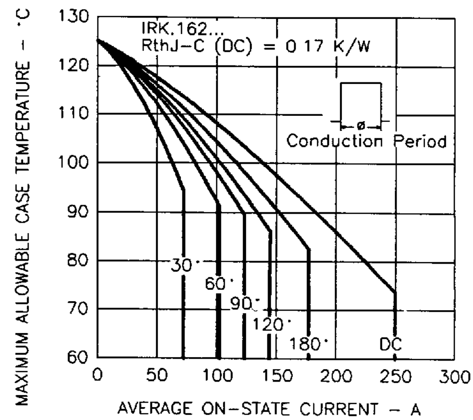


Fig. 20 - Current Ratings Characteristics

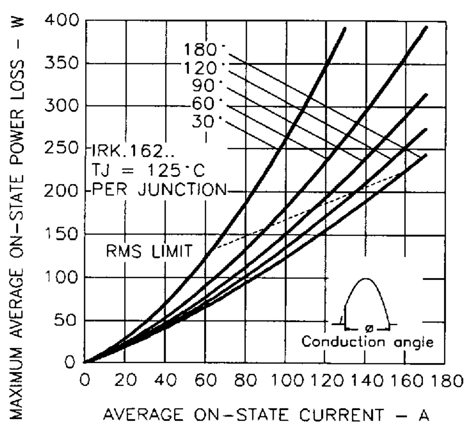


Fig. 21 - On-state Power Loss Characteristics

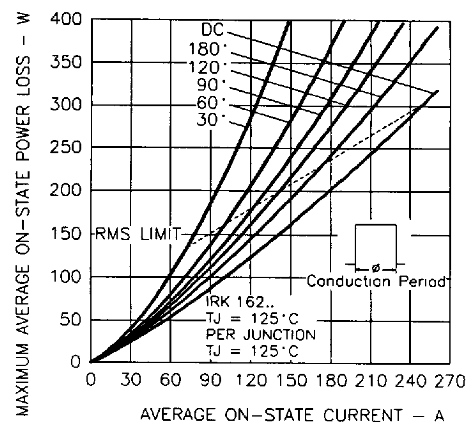


Fig. 22 - On-state Power Loss Characteristics

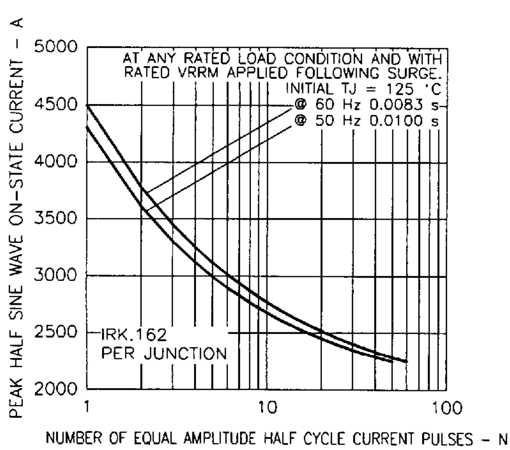


Fig. 23 - Maximum Non-Repetitive Surge Current

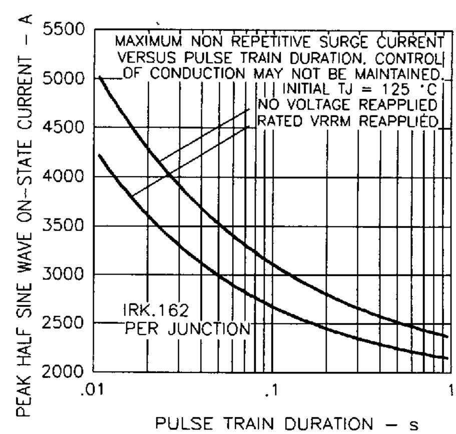


Fig. 24 - Maximum Non-Repetitive Surge Current

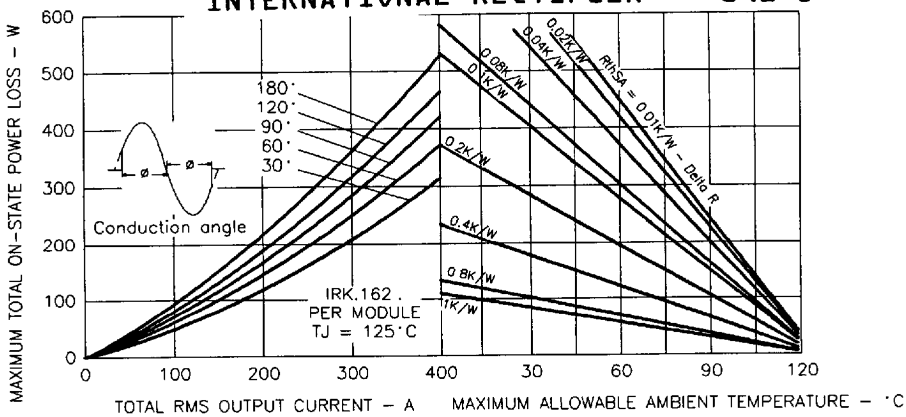


Fig. 25 - On-state Power Loss Characteristics

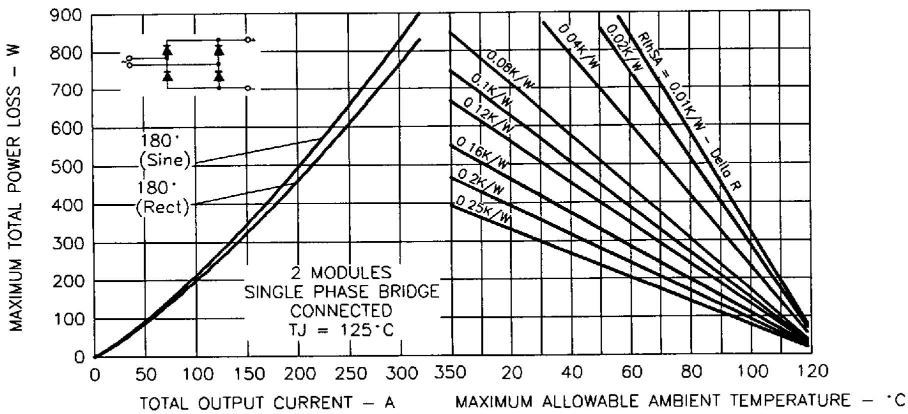


Fig. 26 - On-state Power Loss Characteristics

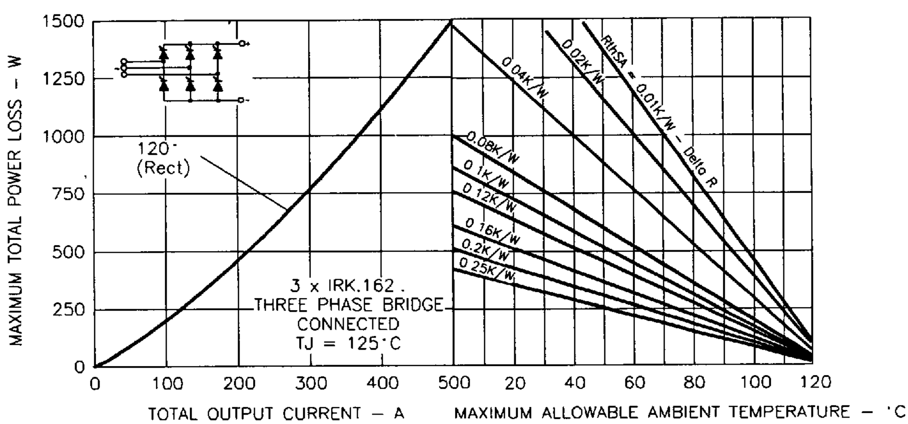


Fig. 27 - On-state Power Loss Characteristics

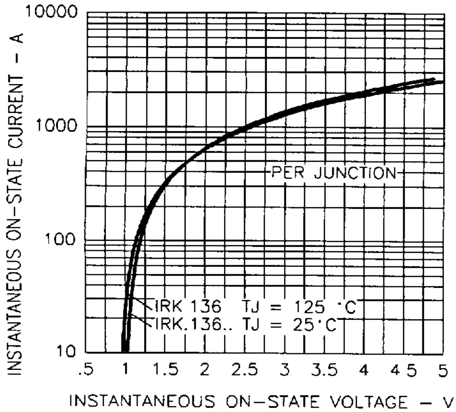


Fig. 28 - On-state Voltage Drop Characteristics

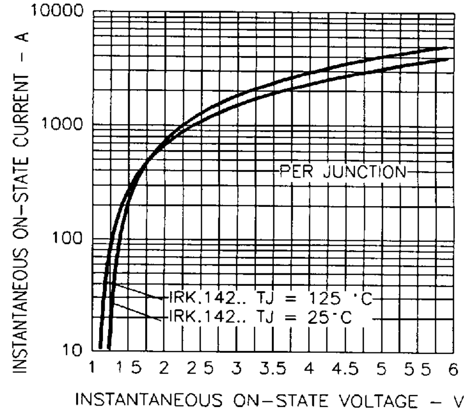


Fig. 29 - On-state Voltage Drop Characteristics

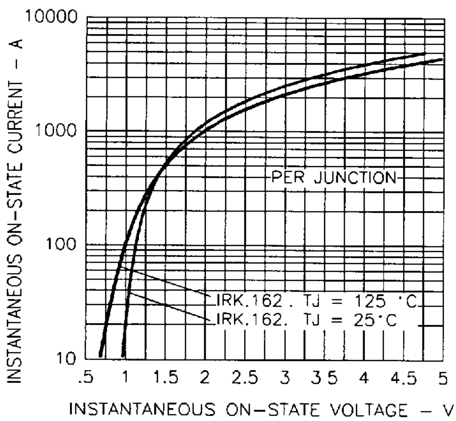


Fig. 30 - On-state Voltage Drop Characteristics

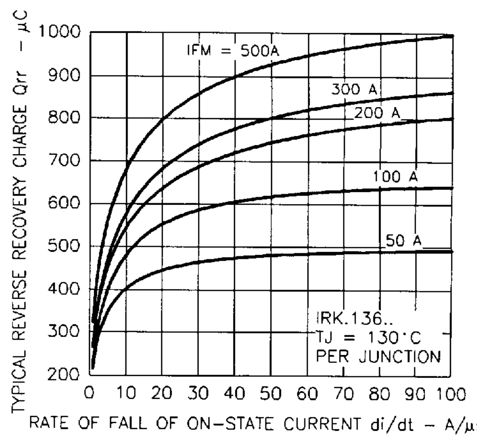


Fig. 31 - Reverse Recovery Charge Characteristics

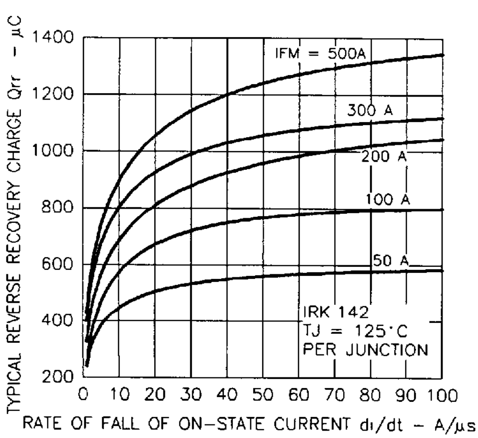


Fig. 32 - Reverse Recovery Charge Characteristics

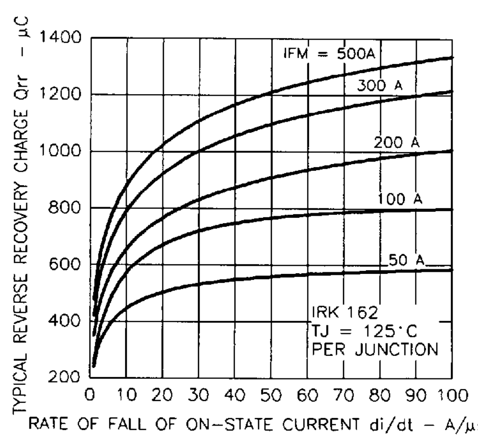


Fig. 33 - Reverse Recovery Charge Characteristics

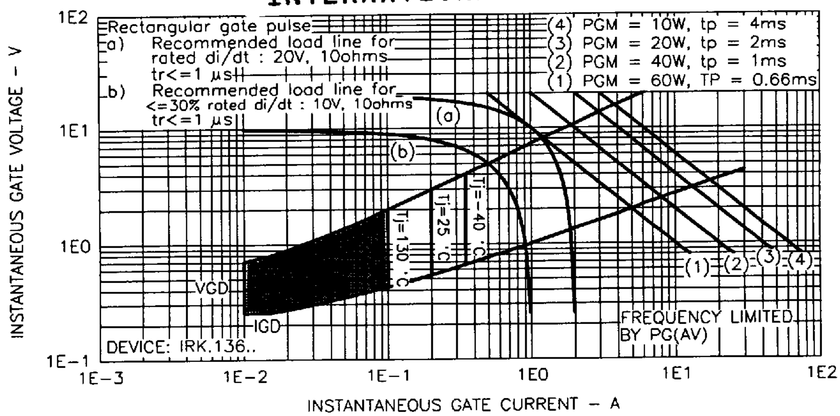


Fig. 34 - Gate Characteristics

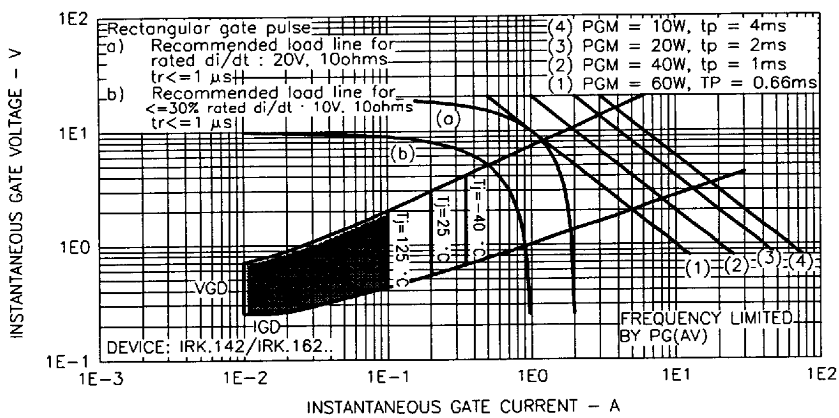


Fig. 35 - Gate Characteristics

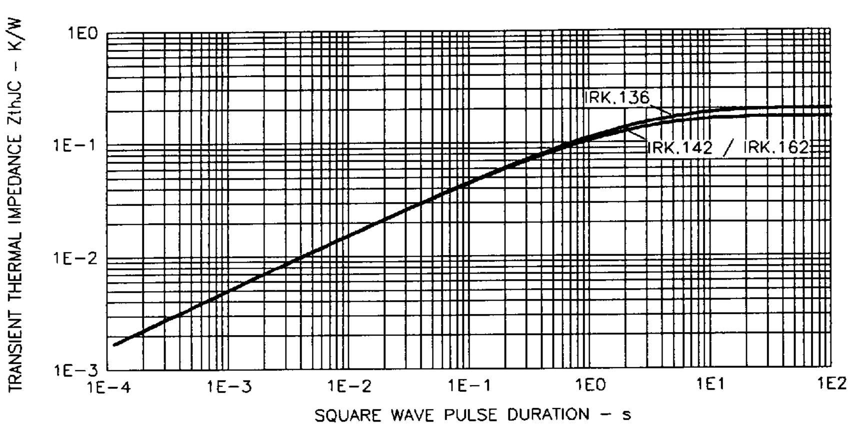


Fig. 36 - Thermal Impedance ZthJC Characteristics