| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |

| REV STATUS OF SHEETS | REV | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

| | | |
|---|---|---|
| PMIC N/A | PREPARED BY<br>Joseph A. Kerby | **DEFENSE SUPPLY CENTER COLUMBUS**<br>**COLUMBUS, OHIO 43216** |
| **STANDARD MICROCIRCUIT DRAWING**<br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br>AMSC N/A | CHECKED BY<br>Charles F. Saffle, Jr | |
| | APPROVED BY<br>Monica L. Poelking | MICROCIRCUIT, DIGITAL, CMOS, 10-BIT ADDRESSABLE SCAN PORTS, MULTIDROP-ADDRESSABLE IEEE STD 1149.1 (JTAG) TAP TRANSCEIVERS, MONOLITHIC SILICON |
| | DRAWING APPROVAL DATE<br>97-10-20 | |
| | REVISION LEVEL | SIZE: **A** / CAGE CODE: **67268** / **5962-96812** |
| | | SHEET 1 OF 47 |

DSCC FORM 2233
APR 97

5962-E032-98

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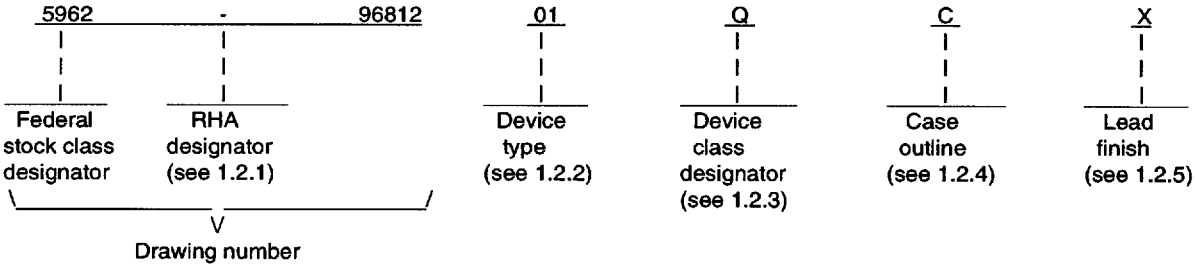
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54ABT8996 | 10-BIT Addressable Scan Ports Multidrop-Addressable IEEE STD 1149.1 (JTAG) TAP Transceivers |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| L | GDIP3-T24 or CDIP4-T24 | 24 | Dual-in-line |
| K | GDFP2-F24 or CDFP3-F24 | 24 | Flat pack |
| 3 | CQCC1-N28 | 28 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.



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1.3 Absolute maximum ratings. 1/ 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +7.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.5 V dc to +7.0 V dc 4/ |
| DC output voltage range ($V_{OUT}$) (high state or power-off state) | -0.5 V dc to +5.5 V dc |
| DC input clamp current ($I_{IK}$) ($V_{IN}$ < 0.0 V) | -18 mA |
| DC output clamp current ($I_{OK}$) ($V_{OUT}$ < 0.0 V) | -50 mA |
| Current into any output in the low state ($I_{OUT}$) | +96 mA |
| Maximum power dissipation at $T_A$ = +55°C (in still air) | 0.5 W 6/ |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +150°C |

1.4 Recommended operating conditions. 2/ 3/ 7/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Minimum high level input voltage ($V_{IH}$) | +2.0 V |
| Maximum low level input voltage ($V_{IL}$) | +0.8 V |
| Input voltage range ($V_{IN}$) | 0.0 V to Vcc |
| Maximum high level output current ($I_{OH}$) | -24 mA |
| Maximum low level output current ($I_{OL}$) | +48 mA |
| Maximum input transition rise and fall rate ($\Delta t/\Delta V$) | 10 ns/V |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1.5 Digital logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) | XX percent 8/ |

---

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55°C to +125°C.
4/ The input and output negative voltage ratings may be exceeded provided that the input and output clamp current ratings are observed.
5/ The value of $V_{CC}$ is provided in the recommended operating conditions table.
6 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
7/ Unused inputs must be held high or low to prevent them from floating.
8/ Values will be added when they become available.



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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuit.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the document which are DOD adopted are those listed in the issue of DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)
IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.



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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional table. The functional table shall be as specified on figure 2.

3.2.4 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.5 Bit-pair timing. The bit-pair timing shall be as specified on figure 4.

3.2.6 Complete shadow protocol. The complete shadow protocol shall be as specified on figure 5.

3.2.7 Shadow protocol errors. The shadow protocol errors shall be as specified on figure 6.

3.2.8 TAP monitor state diagram. The TAP monitor state diagram shall be as specified on figure 7.

3.2.9 Address map. The address map shall be as specified on figure 8.

3.2.10 Shadow-protocol timing, protocol result = MATCH, prior connect status = ON. The Shadow-protocol timing, protocol result = MATCH, prior connect status = ON shall be as specified on figure 9.

3.2.11 Shadow-protocol timing, protocol result = NO MATCH, prior connect status = ON. The Shadow-protocol timing, protocol result = NO MATCH, prior connect status = ON shall be as specified on figure 10.

3.2.12 Shadow-protocol timing, protocol result = NO MATCH, prior connect status = OFF. The Shadow-protocol timing, protocol result = NO MATCH, prior connect status = OFF shall be as specified on figure 11.

3.2.13 Shadow-protocol timing, protocol result = DISCONNECT, prior connect status = ON. The Shadow-protocol timing, protocol result = DISCONNECT, prior connect status = ON shall be as specified on figure 12.

3.2.14 Shadow-protocol timing, protocol result = DISCONNECT, prior connect status = OFF. The Shadow-protocol timing, protocol result = DISCONNECT, prior connect status = OFF shall be as specified on figure 13.

3.2.15 Shadow-protocol timing, protocol result = RESET, prior connect status = ON. The Shadow-protocol timing, protocol result = RESET, prior connect status = ON shall be as specified on figure 14.

3.2.16 Shadow-protocol timing, protocol result = RESET, prior connect status = OFF. The Shadow-protocol timing, protocol result = RESET, prior connect status = OFF shall be as specified on figure 15.

3.2.17 Protocol result = TEST SYNCHRONIZATION, prior connect status = ON. The Protocol result = TEST SYNCHRONIZATION, prior connect status = ON shall be as specified on figure 16.

3.2.18 Protocol result = TEST SYNCHRONIZATION, prior connect status = OFF. The Protocol result = TEST SYNCHRONIZATION, prior connect status = OFF shall be as specified on figure 17.

3.2.19 Protocol result = HARD ERROR (PTMS change during select protocol), prior connect status = ON. The Protocol result = HARD ERROR (PTMS change during select protocol), prior connect status = ON shall be as specified on figure 18.

3.2.20 Protocol result = HARD ERROR (PTMS change during acknowledge protocol), prior connect status = ON. The Protocol result = HARD ERROR (PTMS change during acknowledge protocol), prior connect status = ON shall be as specified on figure 19.



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3.2.21 Protocol result = SOFT ERROR, prior connect status = ON. The Protocol result = SOFT ERROR, prior connect status = ON shall be as specified on figure 20.

3.2.22 Protocol-bypass timing, prior connect status = ON. The Protocol-bypass timing, prior connect status = ON shall be as specified on figure 21.

3.2.23 Protocol-bypass timing, prior connect status = OFF. The Protocol-bypass timing, prior connect status = OFF shall be as specified on figure 22.

3.2.24 Asynchronous reset timing, prior connect status = ON. Asynchronous reset timing, prior connect status = ON shall be as specified on figure 23.

3.2.25 Asynchronous reset timing, prior connect status = OFF. Asynchronous reset timing, prior connect status = OFF shall be as specified on figure 24.

3.2.26 Asynchronous reset timing, $\overline{BYP}$ = L. Asynchronous reset timing, $\overline{BYP}$ = L shall be as specified on figure 25.

3.2.27 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 128 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1 - 1990.



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TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Negative input clamp voltage 3022 | $V_{IC-}$ | For input under test, $I_{IN} = -18mA$ | | 4.5 V | 1, 2, 3 | | -1.2 | V |
| High level output voltage 3006 | $V_{OH}$ | For all inputs affecting output under test $V_{IN} = V_{IH}$ or $V_{IL}$ For all other inputs $V_{IN} = V_{CC}$ or GND | $I_{OH} = -3$ mA | 4.5 V | 1, 2, 3 | 2.5 | | V |
| | | | | 5.0 V | 1, 2, 3 | 3.0 | | |
| | | | $I_{OH} = -24$ mA | 4.5 V | 1, 2, 3 | 2.0 | | |
| Low level output voltage 3007 | $V_{OL}$ | For all inputs affecting output under test $V_{IN} = V_{IH}$ or $V_{IL}$ For all other inputs $V_{IN} = V_{CC}$ or GND | $I_{OL} = +48mA$ | 4.5 V | 1, 2, 3 | | 0.55 | V |
| Input current high 3010 | $I_{IH1}$ | For all inputs affecting output under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND | PTCK | 0.0 V and 5.5 V | 1, 2, 3 | | +1.0 | µA |
| Input current low 3009 | $I_{IL1}$ | For all inputs affecting output under test $V_{IN}$ = GND For all other inputs $V_{IN} = V_{CC}$ or GND | | 0.0 V and 5.5 V | 1, 2, 3 | | -1.0 | µA |
| Input current high 3010 | $I_{IH2}$ | For all inputs affecting output under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND | PTDI, PTMS, PTRST | 5.5 V | 1, 2, 3 | | +10.0 | µA |
| Input current low 3009 | $I_{IL2}$ | For all inputs affecting output under test $V_{IN}$ = GND For all other inputs $V_{IN} = V_{CC}$ or GND | PTDI, PTMS, PTRST | 5.5 V | 1, 2, 3 | -18 | -50.0 | µA |
| Input current high 3010 | $I_{IH3}$ | For all inputs affecting output under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND | A9-A0, $\overline{BYP}$, STDI | 5.5 V | 1, 2, 3 | | +10.0 | µA |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ -55°C ≤ $T_C$ ≤ +125°C +4.5 V ≤ $V_{CC}$ ≤ +5.5 V unless otherwise specified | | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Input current low 3009 | $I_{IL3}$ | For all inputs affecting output under test $V_{IN}$ = GND For all other inputs $V_{IN}$ = $V_{CC}$ or GND | A9-A0, $\overline{BYP}$, STDI | 5.5 V | 1, 2, 3 | -60 | -150 | µA |
| Offstate leakage current high 3021 | $I_{OZH}$ | For control inputs affecting output under test, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{OUT}$ = 2.7V | PTDO, STDO | 5.5 V | 1, 2, 3 | | +10.0 | µA |
| Offstate leakage current low 3020 | $I_{OZL}$ | For control inputs affecting output under test, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{OUT}$ = 0.5V | PTDO, STDO | 5.5 V | 1, 2, 3 | | -10.0 | µA |
| Three-state output leakage current 3009 | $I_{OFF}$ | For input/output under test, $V_{IN}$ or $V_{OUT}$ ≤ 4.5V For all other inputs, $V_{IN}$ = $V_{CC}$ or GND | | 0.0 V | 1 | | ±100 | µA |
| Offstate leakage current low 3020 | $I_{CEX}$ | $V_{OUT}$ = 5.5V | Outputs in the high state | 5.5 V | 1, 2, 3 | | 50.0 | µA |
| Output current 3011 | $I_{OUT}$ 4/ | $V_{OUT}$ = 2.5V | | 5.5 V | 1, 2, 3 | -50.0 | -200.0 | mA |
| Quiescent supply current 3005 | $I_{CC1}$ | $I_{OUT}$ = 0.0A For all inputs, $V_{IN}$ = $V_{CC}$ or GND | Off, STCK = H, STMS = H | 5.5 V | 1, 2, 3 | | 1.5 | mA |
| | $I_{CC2}$ | | On, PTDO = L, STCK = L, STDO = L, STMS = L | 5.5 V | 1, 2, 3 | | 18.0 | |
| | $I_{CC3}$ | | On, PTDO = H, STCK = H, STDO = H, STMS = H | 5.5 V | 1, 2, 3 | | 5.0 | |
| | $I_{CC4}$ | | TRST, STCK = L | 5.5 V | 1, 2, 3 | | 8.0 | |
| Quiescent supply current delta TTL input levels 3005 | $\Delta I_{CC}$ 5/ | For input under test, $V_{IN}$ = 3.4 V Other inputs at $V_{CC}$ or GND | | 5.5 V | 1, 2, 3 | | 1.5 | mA |
| Input capacitance 3012 | $C_{IN}$ | $T_C$ = +25°C, See 4.4.1c | | 5.0 V | 4 | | 14.0 | pF |
| Output capacitance 3012 | $C_{OUT}$ | $T_C$ = +25°C See 4.4.1c | STDO, PTDO | 5.0 V | 4 | | 12.0 | pF |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Clock frequency, PTCK | $f_{clock}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 0 | 40 | MHz |
| Pulse duration, $\overline{BYP}$ low | $t_{w1}$ 6/ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 4.9 | | ns |
| Pulse duration, PTCK high | $t_{w2}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5V | 9, 10,11 | 12.0 | | ns |
| Pulse duration, PTCK low | $t_{w3}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5V | 9, 10,11 | 6.5 | | ns |
| Pulse duration, PTRST low | $t_{w4}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5V | 9, 10,11 | 2.6 | | ns |
| Setup time, An before PTCK↓ | $t_{su1}$ 7/ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 6.6 | | ns |
| Setup time, PTDI before PTCK↑ | $t_{su2}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 4.9 | | ns |
| Setup time, PTMS before BYP↑ | $t_{su3}$ 6/ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 0.8 | | ns |
| Setup time, PTMS before PTCK↑ | $t_{su4}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 9.0 | | ns |
| Hold time, An before PTCK↓ | $t_{h1}$ 7/ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 0.3 | | ns |
| Hold time, PTDI after PTCK↑ | $t_{h2}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 0.7 | | ns |
| Hold time, PTMS after BYP↑ | $t_{h3}$ 6/ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 2.4 | | ns |
| Hold time, PTMS after PTCK↑ | $t_{h4}$ | $C_L$ 50 pF minimum<br>$R_L$ = 500 Ω<br>See figure 5 | 4.5 V and 5.5 V | 9, 10,11 | 1.3 | | ns |

See footnotes at end of table.




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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Functional test 3014 | 8/ | $V_{IN} = V_{IH}$ or $V_{IL}$ Verify output $V_O$ See 4.4.1b | 4.5 V<br>5.0 V<br>5.5 V | 7, 8 | L | H | |
| Maximum operating frequency, PTCK | $f_{max}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 40 | | MHz |
| | | | 4.5 V and 5.5 V | 10,11 | 40 | | |
| Propagation delay time, BYP↑ to CON 3003 | $t_{PLH1}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.0 | 4.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.3 | |
| Propagation delay time, BYP↓ to CON 3003 | $t_{PHL1}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.0 | 5.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 6.3 | |
| Propagation delay time, BYP↓ to STMS 3003 | $t_{PLH2}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 2.5 | 10.0 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 2.5 | 12.9 | |
| Propagation delay time, BYP↓ to STMS 3003 | $t_{PHL2}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 2.5 | 7.0 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 2.5 | 8.9 | |
| Propagation delay time, PTCK to STCK 3003 | $t_{PLH3}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.0 | 3.1 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 3.7 | |
| Propagation delay time, PTCK to STCK 3003 | $t_{PHL3}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.0 | 3.9 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 4.6 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay time, PTCK↓ to CON 3003 | $t_{PLH4}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 3.5 | 8.9 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.5 | 11.2 | |
| Propagation delay time, PTCK↓ to CON 3003 | $t_{PHL4}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 3.5 | 9.3 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.5 | 11.6 | |
| Propagation delay time, PTCK↓ to PTDO (Shadow protocol acknowledge) 3003 | $t_{PLH5}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 3.0 | 9.9 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.0 | 12.6 | |
| Propagation delay time, PTCK↓ to PTDO (Shadow protocol acknowledge) 3003 | $t_{PHL5}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 3.0 | 9.4 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.0 | 10.9 | |
| Propagation delay time, PTCK↓ to STMS (connect) 3003 | $t_{PLH6}$ 9/ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 5.5 | 15.4 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 5.5 | 19.9 | |
| Propagation delay time, PTCK↓ to STMS (connect) 3003 | $t_{PHL6}$ 9/ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 5.5 | 12.5 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 5.5 | 15.8 | |
| Propagation delay time, PTDI to STDO 3003 | $t_{PLH7}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.4 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.4 | |

See footnotes at end of table.




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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay time, PTDI to STDO<br>3003 | $t_{PHL7}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.5 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.6 | |
| Propagation delay time, PTMS to STMS<br>3003 | $t_{PLH8}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.4 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.5 | |
| Propagation delay time, PTMS to STMS<br>3003 | $t_{PHL8}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.7 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.7 | |
| Propagation delay time, PTRST to STRST<br>3003 | $t_{PLH9}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.8 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.8 | |
| Propagation delay time, PTRST to STRST<br>3003 | $t_{PHL9}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.7 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.7 | |
| Propagation delay time, PTRST↓ to CON<br>3003 | $t_{PLH10}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$, | 5.0 V | 9 | 3.5 | 9.5 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.5 | 12.1 | |
| Propagation delay time, PTRST↓ to STMS<br>3003 | $t_{PLH11}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$, | 5.0 V | 9 | 2.5 | 7.7 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 2.5 | 9.6 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay time, STDI to PTDO 3003 | $t_{PLH12}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.0 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 4.9 | |
| Propagation delay time, STDI to PTDO 3003 | $t_{PHL10}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 1.0 | 4.6 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 5.7 | |
| Propagation delay time, BYP↓ to PTDO 3003 | $t_{PZH1}$ 10/ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 1.5 | 5.5 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.5 | 6.9 | |
| Propagation delay time, BYP↓ to PTDO 3003 | $t_{PZL1}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 1.5 | 6.1 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.5 | 7.5 | |
| Propagation delay time, BYP↓ to STDO 3003 | $t_{PZH2}$ 11/ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 1.5 | 5.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.5 | 6.2 | |
| Propagation delay time, BYP↓ to STDO 3003 | $t_{PZL2}$ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 1.5 | 5.8 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.5 | 6.9 | |
| Propagation delay time, PTCK↓ to PTDO 3003 | $t_{PZH3}$ 10/ | $C_L = 50$ pF minimum, $R_L = 500\ \Omega$, | 5.0 V | 9 | 4.0 | 9.5 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 4.0 | 12.1 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay time, PTCK↓ to STDO 3003 | $t_{PZH4}$ 11/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 4.0 | 10.0 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 4.0 | 12.5 | |
| Propagation delay time, PTCK↓ to STDO 3003 | $t_{PZL3}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 4.0 | 10.7 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 4.0 | 12.8 | |
| Propagation delay time, BYP↑ to PTDO 3003 | $t_{PHZ1}$ 10/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.5 | 4.8 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.5 | 5.5 | |
| Propagation delay time, BYP↑ to PTDO 3003 | $t_{PLZ1}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.3 | 4.9 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.3 | 5.8 | |
| Propagation delay time, BYP↑ to STDO 3003 | $t_{PHZ2}$ 11/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.5 | 4.8 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.5 | 5.5 | |
| Propagation delay time, BYP↑ to STDO 3003 | $t_{PLZ2}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.5 | 4.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.5 | 4.8 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay time, PTCK↓ to PTDO 3003 | $t_{PHZ3}$ 10/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 3.0 | 8.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.0 | 11.0 | |
| Propagation delay time, PTCK↓ to PTDO 3003 | $t_{PLZ3}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.0 | 9.5 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 13.1 | |
| Propagation delay time, PTCK↓ to STDO 3003 | $t_{PHZ4}$ 11/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 3.5 | 9.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.5 | 12.0 | |
| Propagation delay time, PTCK↓ to STDO 3003 | $t_{PLZ4}$ 12/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.0 | 8.7 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 10.4 | |
| Propagation delay time, PTRST↓ to PTDO 3003 | $t_{PHZ5}$ 10/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 3.5 | 9.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.5 | 11.0 | |
| Propagation delay time, PTRST↓ to PTDO 3003 | $t_{PLZ5}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, | 5.0 V | 9 | 1.0 | 10.2 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 1.0 | 13.4 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay time, PTRST↓ to STDO 3003 | $t_{PHZ6}$ 11/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, See Figure 5 | 5.0 V | 9 | 4.5 | 12.0 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 4.5 | 13.6 | |
| Propagation delay time, PTRST↓ to STDO 3003 | $t_{PLZ6}$ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, See Figure 5 | 5.0 V | 9 | 3.0 | 9.0 | ns |
| | | | 4.5 V and 5.5 V | 10,11 | 3.0 | 10.5 | |

1/ For tests not listed in the referenced MIL-STD-883 (e.g. $\Delta I_{CC}$), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all $I_{CC}$ and $\Delta I_{CC}$ tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, $V_{IN}$ = GND or $V_{IN} \le 5.5$ V.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

5/ This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously (alternate method) at $V_{IN}$ = 3.4V. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.5 mA; and the preferred method and limits are guaranteed.

6/ In normal application of the Addressable Scan Port, such timing requirements with respect to $\overline{BYP}$ are met implicitly and, therefore, need not be considered.



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TABLE I. Electrical performance characteristics - Continued

7/ These requirements apply only in the case where the address inputs are changed during a shadow protocol. For normal application of the ASP, it is recommended that the address inputs remain static throughout any shadow protocols. In such cases, the timing of address inputs relative to PTCK need not be considered.

8/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, $V_{IL}$ = 0.4 V and $V_{IH}$ = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

9/ The transitions at STMS are only possible when a shadow-protocol select is issued while STMS is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended since state synchronization of the primary TAP to secondary TAP cannot be ensured.

10/ In most applications, the node to which PTDO is connected has a pullup resistor. In such cases, this parameter is not significant.

11/ In most applications, the node to which STDO is connected has a pullup resistor. In such cases, this parameter is not significant.

12/ This parameter applies only in case of protocol hard error.



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| Device type | 01 | |
|---|---|---|
| Case outlines | L, K | 3 |
| Terminal number | Terminal symbol | |
| 1 | A4 | NC |
| 2 | A3 | A4 |
| 3 | A2 | A3 |
| 4 | A1 | A2 |
| 5 | A0 | A1 |
| 6 | BYP | A0 |
| 7 | GND | BYP |
| 8 | PTDO | NC |
| 9 | PTCK | GND |
| 10 | PTMS | PTDO |
| 11 | PTDI | PTCK |
| 12 | PTRST | PTMS |
| 13 | STRST | PTDI |
| 14 | STDO | PTRST |
| 15 | STMS | NC |
| 16 | STCK | STRST |
| 17 | STDI | STDO |
| 18 | CON | STMS |
| 19 | VCC | STCK |
| 20 | A9 | STDI |
| 21 | A8 | CON |
| 22 | A7 | NC |
| 23 | A6 | VCC |
| 24 | A5 | A9 |
| 25 | - | A8 |
| 26 | - | A7 |
| 27 | - | A6 |
| 28 | - | A5 |

NC = No Connection

FIGURE 1. Terminal connections.



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| TERMINAL NAME | TERMINAL DESCRIPTION |
|---|---|
| A9-A0 | ADDRESS INPUTS. The ASP compares addresses received via shadow protocol against the value at A9-A0 to determine address match. The bit order is from most significant to least significant. An internal pullup at each A9-A0 terminal forces the terminal to a high level if it has no external connection |
| $\overline{BYP}$ | BYPASS INPUT. A low input at $\overline{BYP}$ forces the ASP into BYP or BYP/TRST status, depending on $\overline{PTRST}$ being high or low respectively. While BYP is low, shadow protocols are ignored. Otherwise, while BYP is high, the ASP is free to respond to shadow protocols. An internal pullup forces BYP to a high level if it has no external connection. |
| $\overline{CON}$ | CONNECT INDICATOR (output). The ASP indicates secondary-scan-port activity (resulting from BYP, BYP/TRST, MULTICAST, or ON status) by forcing CON to be low. Inactivity (resulting from OFF, RESET, or TRST status) is indicated when CON is high. |
| GND | Ground |
| PTCK | PRIMARY TEST CLOCK. PTCK receives the TCK signal required by IEEE Standard 1149.1 - 1990. The ASP always buffers PTCK to STCK. Shadow protocols are received/acknowledged synchronously to PTCK and connect-status changes invoked by shadow protocol are made synchronously to PTCK. |
| PTDI | PRIMARY TEST DATA INPUT. PTDI receives the TDI signal required by IEEE Standard 1149.1 - 1990. During appropriate TAP states, the ASP monitors PTDI for shadow protocols, data at PTDI is captured on the rising edge of PTCK. When a valid shadow protocol is received in this fashion, the ASP compares the received address against the A9-A0 inputs. If the ASP detects a match, it outputs an acknowledgement and then connects it's primary TAP terminals. Under BYP, BYP.TRST, MULTICAST or ON status, the ASP buffers the PTDI signal to STDO. An internal pullup forces PTDI to high level if it has no external connection. |
| PTDO | PRIMARY TEST DATA OUTPUT, PTDO transmits the TDO signal required by IEEE Standard 1149.1 - 1990. During shadow protocols, the ASP transmits any required acknowledgement via the PTDO. The acknowledgement data output at PTDO changes on the falling edge of PTCK. Under BYP, BYP/TRST, or ON status, the ASP buffers the PTDO signal from STDI. Under OFF, MULTICAST, RESET, or TRST status, PTDO is at high impedance. |
| PTMS | PRIMARY TEST MODE SELECT. PTMS receives the TMS signal required by IEEE Standard 1149.1 - 1990. The ASP monitors the PTMS to determine the TAP-controller state. During stable TAP states other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test-Idle, Pause-DR, Pause-IR) the ASP can respond to shadow protocols. Under BYP, MULTICAST, or ON status, the ASP buffers the PTMS signal to STMS. An internal pullup forces PTMS to high level if it has no external connection. |
| $\overline{PTRST}$ | PRIMARY TEST RESET. $\overline{PTRST}$ receives the TRST signal allowed by IEEE Standard 1149.1 - 1990. The ASP always buffers PTRST to STRST. A low input at PTRST forces the ASP to assume TRST or BYP/TRST status, depending on BYP being high or low, respectively. Such operation also synchronously resets the internal ASP state to it's power-up condition. Otherwise, while PTRST is high, the ASP is free to respond to shadow protocols. An internal pullup forces PTRST to a high level if it has no external connection. |
| STCK | SECONDARY TEST CLOCK. STCK retransmits the TCK signal required by IEEE Standard 1149.1 - 1990. The ASP always buffers STCK from PTCK. |
| STDI | SECONDARY TEST DATA INPUT. STDI receives the TDI signal required by IEEE Standard 1149.1 - 1990. Under BYP, BYP/TRST, or on status, the ASP buffers STDI to PTDO. An internal pullup forces STDI to a high level if it has no external connection. |
| STDO | SECONDARY TEST DATA OUTPUT. STDO transmits the TDO signal required by IEEE Standard 1149.1 - 1990. Under BYP, BYP/TRST, MULTICAST, or ON status, the ASP buffers STDO from PTDI. Under OFF, RESET, or TRST status, the ASP buffers STMS from PTMS. When disconnected (as a result of OFF status, STDO is at high impedance. |
| STMS | SECONDARY TEST MODE SELECT. STMS retransmits the TMS signal required by IEEE Standard 1149.1 - 1990. Under BYP, MULTICAST, or ON status, the asp buffers STMS from PTMS. When disconnected (as a result of OFF status), STMS maintains it's last valid state until the ASP assumes BYP/TRST, RESET, or TRST status (upon which it is forced high) or the ASP again assumes BYP, MULTICAST, or ON status. |
| $\overline{STRST}$ | SECONDARY TEST RESET. $\overline{STRST}$ retransmits the $\overline{TRST}$ signal allowed by IEEE Standard 1149.1 - 1990. The ASP always buffers STRST from PTRST. |
| $V_{CC}$ | SUPPLY VOLTAGE |

FIGURE 1. Terminal connections - Continued.



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| Inputs | | Shadow-Protocol Result 1/ | Outputs | | | | | | Primary To Secondary Connect Status |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{BYP}$ | $\overline{PTRST}$ | | $\overline{STRST}$ | STCK | STMS | STDO | PTDO | $\overline{CON}$ | |
| L | L | - | L | PTCK | H 2/ | PTDI | STDI | L | BYP/TRST 2/ |
| L | H | - | H | PTCK | PTMS | PTDI | STDI | L | BYP |
| H | L | - | L | PTCK | H | Z | Z | H | TRST |
| H | H | Reset | H | PTCK | H | Z | Z | H | RESET |
| H | H | Match | H | PTCK | PTMS | PTDI | STDI | L | ON |
| H | H | No match | H | PTCK | $STMS_0$ 3/ | Z | Z | H | OFF |
| H | H | Hard error 4/ | H | PTCK | $STMS_0$ 3/ | Z | Z | H | OFF |
| H | H | Disconnect | H | PTCK | $STMS_0$ 3/ | Z | Z | H | OFF |
| H | H | Test synchronization | H | PTCK | PTMS | PTDI | Z | L | MULTICAST |

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high clock transition

1/ Shadow protocols are received serially via PTCK and PTDI and acknowledged serially via PTCK and PTDO under certain conditions in which PTMS is static low or static high (see shadow protocol). The result shown here follows any required acknowledgment.

2/ In normal operation of IEEE Std 1149.1-compliant architectures, it is recommended that TMS be high prior to release of TRST. The BYP/TRST connect status ensures that this condition is met at STMS regardless of the applied PTMS. Also, it is recommended that STMS be kept high for a minimum duration of 5 PTCK cycles following assertion of PTRST, either by maintaining PTRST low or by setting PTMS high. This ensures that ICs both with and without TRST inputs are moved to their Test-Logic-Reset TAP states. It is expected that in normal application, this condition will only occur when BYP is fixed at the low state. In such case, upon release of PTRST, the ASP immediately resumes the BYP connect status.

3/ STMS level before indicated steady-state conditions were established.

4/ The shadow protocol is well defined. Some variations in the protocol are tolerated (see protocol errors shown in figure 5). Those that are not tolerated are considered hard errors and cause disconnect as indicated.

FIGURE 2. Functional table.



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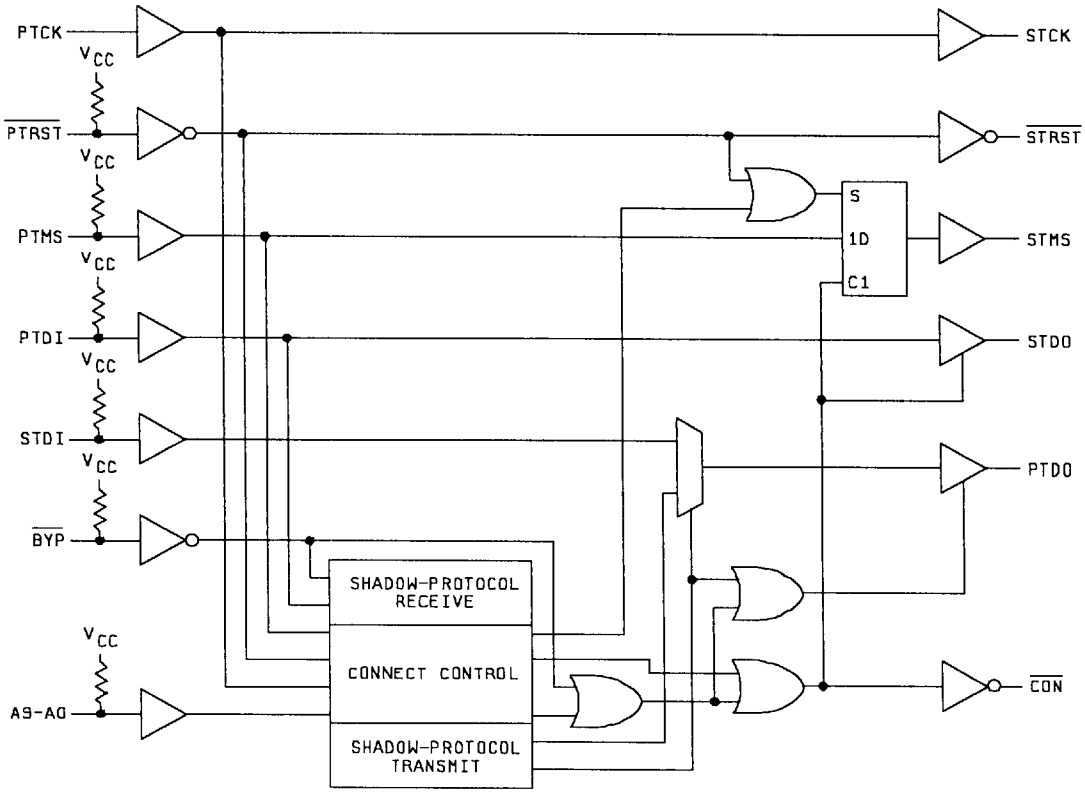


FIGURE 3. Functional block diagram.



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Addressing of an ASP in system is accomplished by shadow protocols, which are received at PTDI synchronously to PTCK. Shadow protocols can occur only in the following stable TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR. Shadow protocols never occur in Shift-DR or Shift-IR states in order to prevent contention on the signal bus to which PTDO is wired. Additionally, the ASP PTMS must be held at a constant low or high level throughout a shadow protocol. If TAP-state changes occur in the midst of a shadow protocol, the shadow protocol is aborted and the select-protocol state machine returns to its initial state.

The shadow protocol is based on a serial bit-pair signaling scheme in which two bit-pair combinations (data one, data zero) are used to represent address data and the other two bit-pair combinations (select, idle) are used for framing - that is, to indicate where address data begins and ends.

These bit pairs are received serially at PTDI (or transmitted serially at PTDO) synchronously to PTCK as follows:

The idle bit pair (I) is represented as two consecutive high signals.
The select bit pair (S) is represented as two consecutive low signals.
The data-one bit pair (D) is represented as a low signal followed by a high signal.

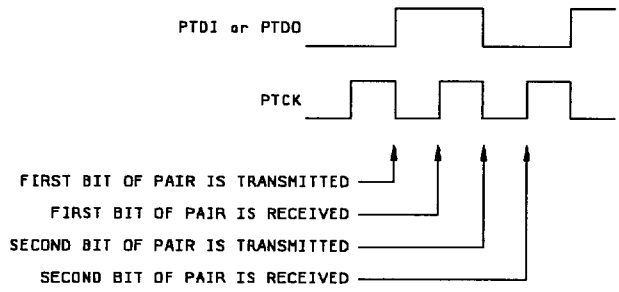


FIGURE 4. Bit-pair timing.

A complete shadow protocol is composed of the receipt of a protocol followed, if applicable, by the transmission of an acknowledged protocol (which is issued from PTDO only if the received address matches that at the A9 - A0 inputs). Both of these subprotocols are composed of ten data bit pairs framed at the beginning by idle and select bit pairs and at the end by select and idle bit pairs. This is represented in an abbreviated fashion as follows: ISDDDDDDDDDSI. Figure 4 shows a complete shadow protocol (the symbol T is used to represent a high-impedance condition on the associated signal line - since the high-impedance state at PTDI at logically high due to pullup, it maps onto the idle bit pair).

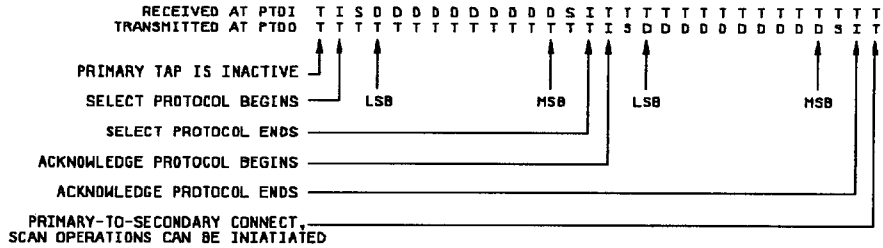


FIGURE 5. Complete shadow protocol.



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SELECT PROTOCOL

The select protocol is the ASP's means of receiving (at PTDI) address information from an IEEE Std 1149.1 bus master. It follows the ISDDDDDDDDDDSI sequence described previously. A 10-bit address value is decoded from the received data-one and/or data/zero bit pairs. These bit pairs are interpreted in least-significant-bit-first order (that is, the first data bit pair received is considered to correspond to A).

ACKNOWLEDGE PROTOCOL

Following the receipt of a complete select-protocol sequence, the protocol result provisionally is set to NO MATCH and the connect status set to OFF. The received address is then compared to that at the ASP address inputs (A9-A0). If these address values match, the ASP immediately (with no delay) responds with an acknowledge protocol transmitted from PTDO. This protocol follows the ISDDDDDDDDDDSI sequence described previously. The transmitted address represents the address of the selected ASP which, by definition, is the same address the ASP received in the select protocol. The 10-bit address value is encoded into data-one and/or data-zero bit pairs. The bit pairs are to be interpreted in least-significant-bit-first order (that is, the first data bit pair transmitted is to be considered to correspond to A0). If the received address does not match that at the A9-A0 inputs, no acknowledge protocol is transmitted and the shadow protocol is considered complete.

PROTOCOL ERRORS

Protocol errors occur when bit pairs are received out of sequence. Some of these sequencing errors can be tolerated and are termed soft errors. No specific action occurs as the result of a soft error. Other errors represent cases where the addressing information could be incorrectly received and are termed hard errors. Hard errors are characterized by sequences in which at least one bit of address data has been properly transmitted followed by a sequencing error. When a hard error occurs, any connection to an ASP is dissolved.

Figure 6 lists the bit-pair sequences that result in soft errors and hard errors. A hard error also results when the primary TAP state changes during select protocol following the proper transmission of at least one bit of address data. Figures 18 and 19 show shadow-protocol timing in case of protocol hard error while figure 20 shows shadow-protocol timing in case of protocol soft error.

| SOFT ERRORS | HARD ERRORS |
|---|---|
| I(D)I | |
| I(D)(D)I | |
| I(D)(S)(D)I | IS(D)I |
| I(S)I | IS(D)S(D)I |
| IS(S)(D)I | IS(D)S(S)I |
| IS(S)(D)(S)I | |

FIGURE 6. Shadow protocol errors.

LONG ADDRESS

Receipt of an address longer than ten bits is considered a hard error and the ASP assumes OFF status. The sole exceptions are when all data ones are received or all data zeros are received. In these special cases, the global addresses represented by these bit sequences are observed and appropriate action taken. That is, in the case that only data ones (ten or more) are received, the shadow-protocol result is TEST SYNCHRONIZATION (if primary TAP state is Pause-DR or Pause-IR), and in the case that only data zeros (ten or more) are received, the shadow-protocol result is RESET.

SHORT ADDRESS

In all cases, receipt of an address shorter than ten bits is considered a hard error and the ASP assumes OFF status.



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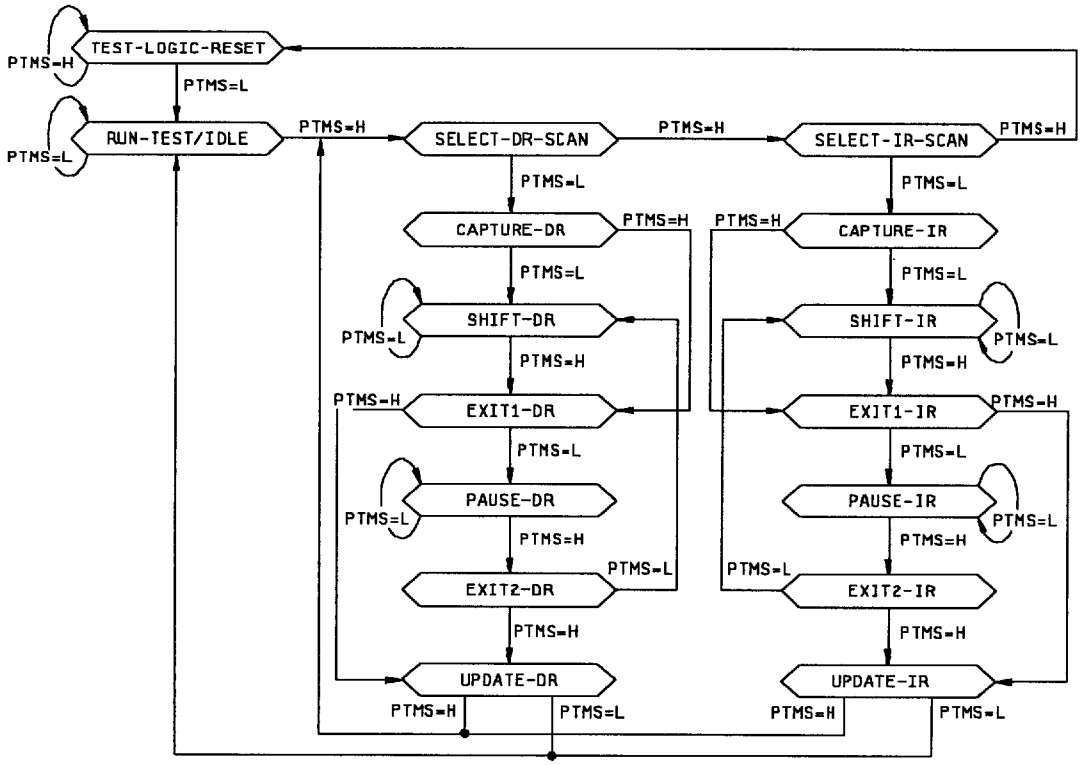


The TAP-state monitor is a synchronous finite-state machine that monitors the primary TAP state. The state diagram is shown here and mirrors that specified by IEEE Standard 1149.1-1990. The TAP-state monitor proceeds through its states based on the level of PTMS at the rising edge of PTCK. Each state is described both in terms of its significance for ASP devices and for connected IEEE Standard 1149.1-compliant devices (called targets). However, the monitor state (primary TAP) can be different from that of disconnected scan chains (secondary TAP).

FIGURE 7. TAP monitor state diagram.



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ADDRESS MATCHING

Connect status of the ASP is computed by a match of the address received in the last valid shadow protocol against that at the address inputs (A9-A0) as well as against the three dedicated addresses that are internal to the ASP (DSA, RSA, and TSA).

If the shadow-protocol address matches the address inputs (A9-A0), then the ASP responds by transmitting an acknowledge protocol. Following the complete transmission of the acknowledge protocol, the ASP assumes ON status (in which PTDI, PTDO, and PTMS are connected to STDO, STDI, and STMS, respectively). The ON status allows the scan chain associated with the ASP's secondary TAP to be controlled from the multidrop primary TAP as if I t were directly wired as such. Figure 9 shows the shadow-protocol timing for MATCH result when the prior ASP connect status is ON and OFF, respectively.

If the shadow-protocol address does not match the address inputs (A9-A0), then (unless the address is one of the three dedicated global address described below) the ASP responds immediately by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 10 and 11 show the shadow-protocol timing for NO MATCH result when the prior ASP connect status is ON and OFF, respectively.

| Address Name | Binary Code | Hex Code | Shadow-Protocol Result | Resultant Primary-To-Secondary Connect Status |
|---|---|---|---|---|
| Reset Address (RSA) | 0000000000 | 000 | RESET | RESET |
| Matching Address | A9–A0 | A9–A0 | MATCH | ON |
| Disconnect Address (DSA) | 1111111110 | 3FE | DISCONNECT | OFF |
| Test Synchronization Address (TSA) | 1111111111 | 3FF | TEST SYNCHRONIZATION | MULTICAST |
| All Other Addresses | All others | All others | NO MATCH | OFF |

FIGURE 8. Address map.

DISCONNECT ADDRESS

The disconnect address (DSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the DSA, it immediately responds by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 12 and 13 show the shadow-protocol timing for DISCONNECT result when the prior ASP connect status is ON and OFF, respectively.

The same result occurs when a non-matching address is received. No specific action to disconnect an ASP is required, as a given ASP is disconnected by the address that connects another. The dedicated DSA ensures that at least one address is available for the purpose of disconnecting all receiving ASPs. It is especially useful when the currently selected scan chain is in a different TAP state then that to be selected. In such a case, the DSA is used to leave the former scan chain in the proper state, after which the primary TAP state is moved to that needed to select the latter scan chain.

RESET ADDRESS

The reset address (RSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the RSA, it immediately responds by assuming the RESET status (in which PTDO and STDO are high impedance and STMS is forced to the high level). This has the effect of deselecting and resetting (to Test-Logic-Reset state) the scan chain associated with ASP secondary TAP. No acknowledge protocol is sent. Figures 14 and 15 show the shadow-protocol timing for RESET result when the prior ASP connect status is ON and OFF, respectively.



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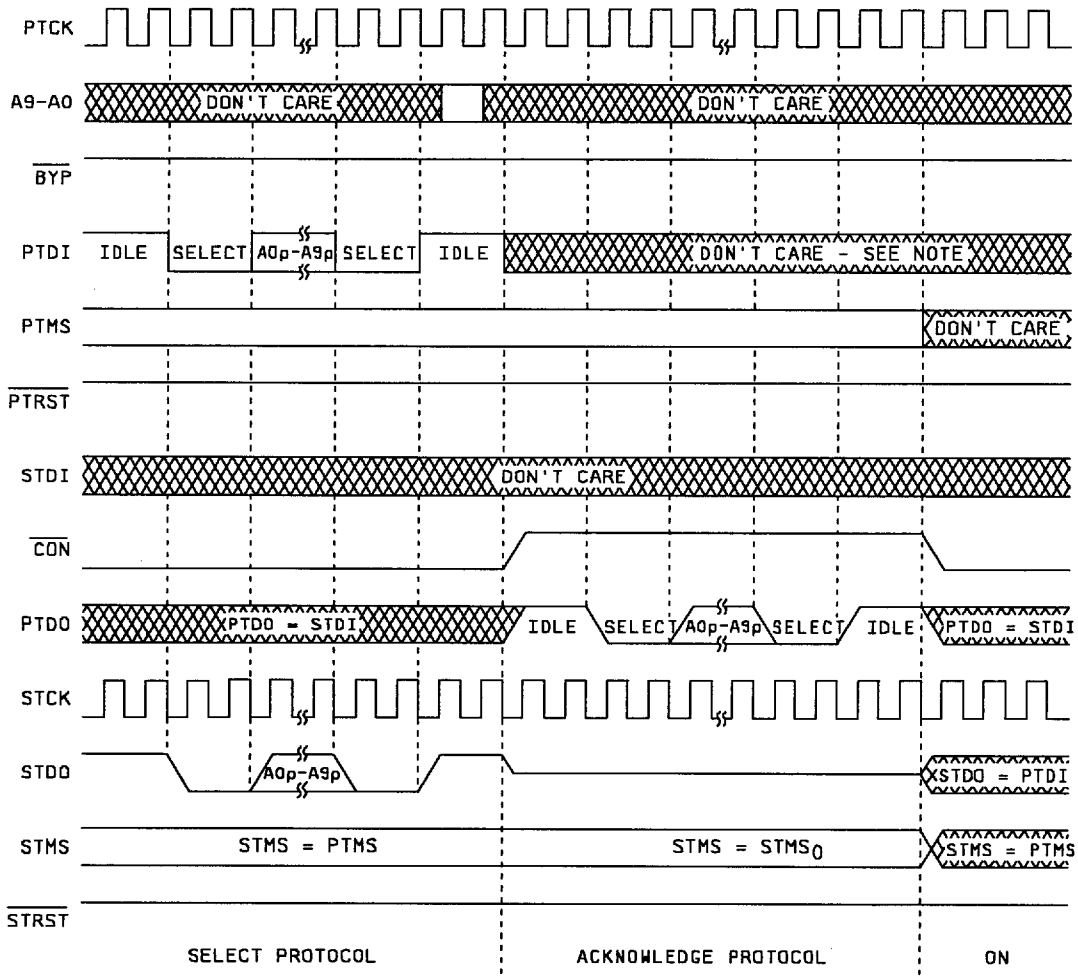


NOTE: The instantaneous value of PTDI during protocol acknowledge is "don't care" as long as the cumulative effect does not represent a protocol hard-error or another valid select protocol.

FIGURE 9. Shadow-protocol timing, protocol result = MATCH, prior connect status = ON.



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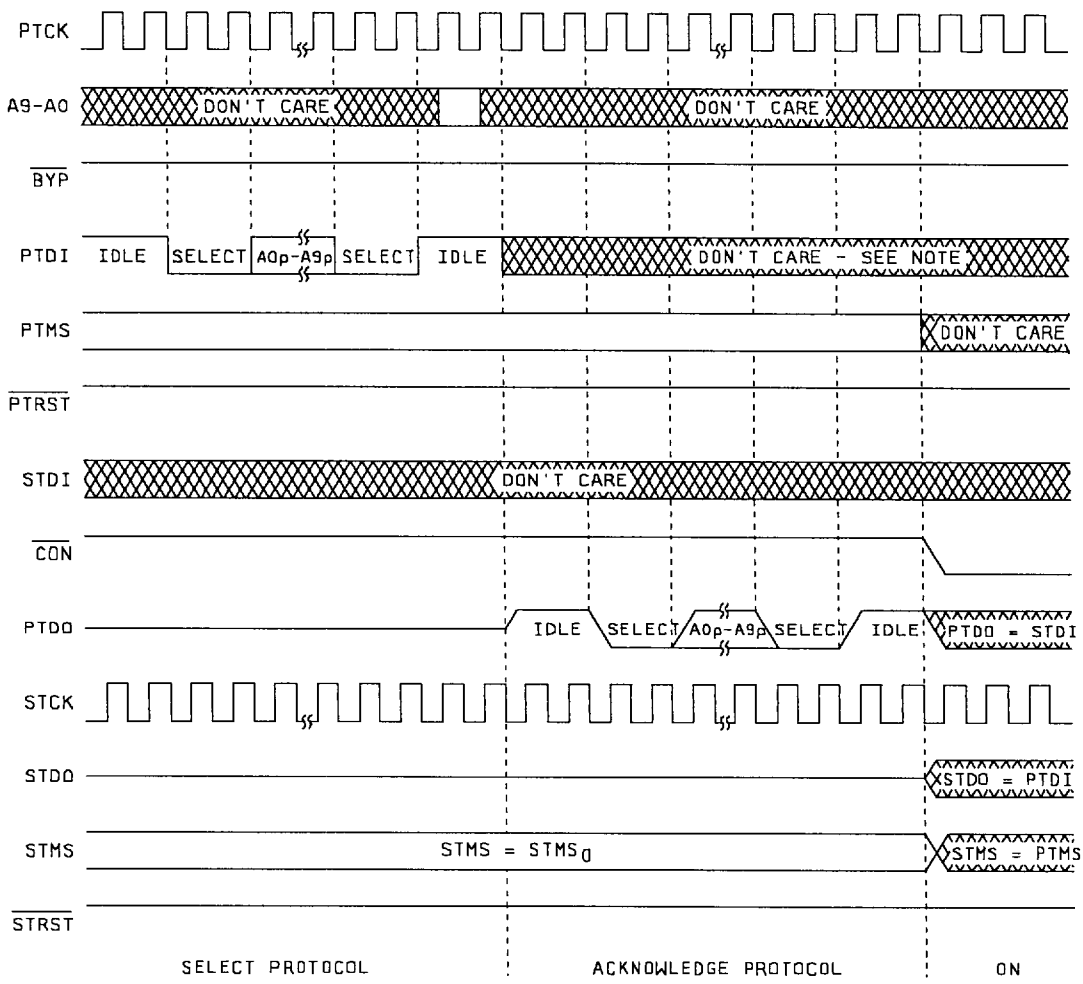


NOTE: Hard-error or another valid select protocol.

FIGURE 9. Shadow-protocol timing, protocol result = MATCH, prior connect status = ON - Continued.



9004708 0033573 615

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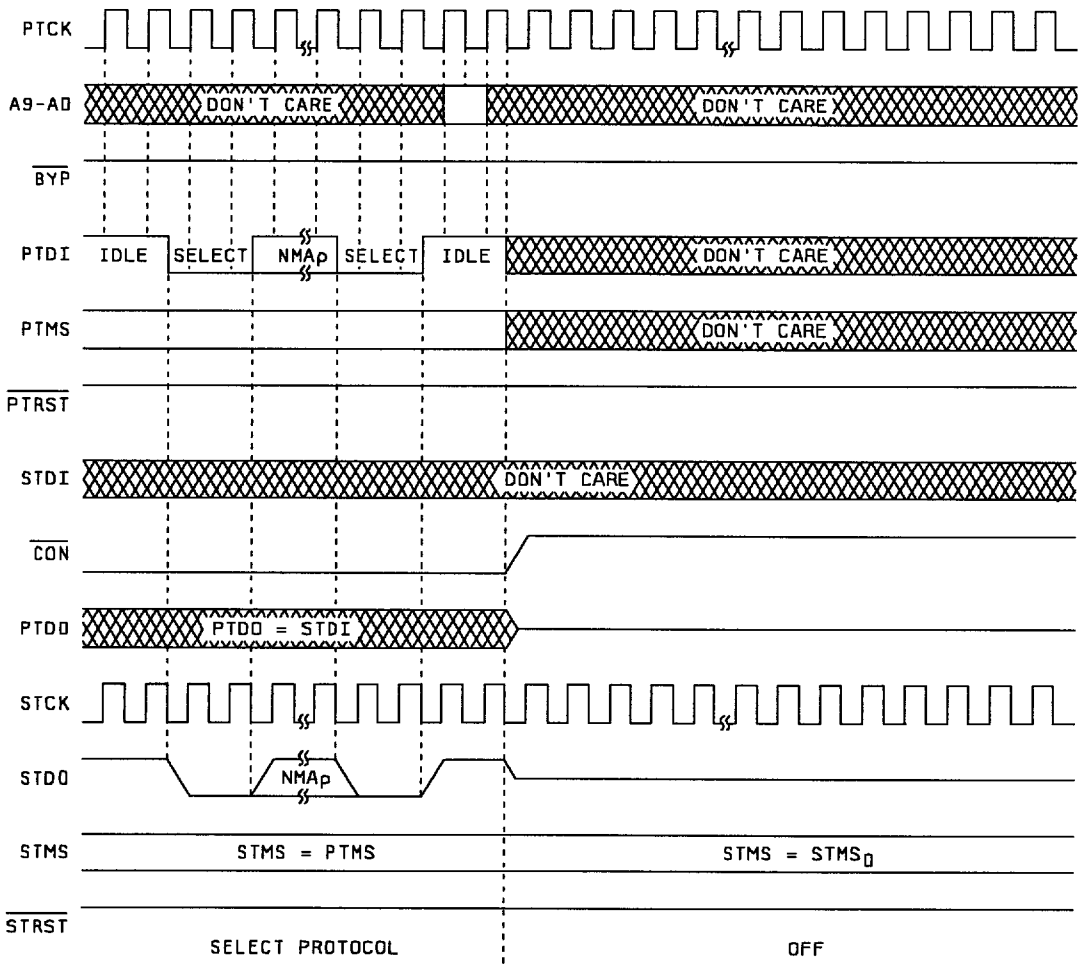


FIGURE 10. Shadow-protocol timing, protocol result = NO MATCH, prior connect status = ON.



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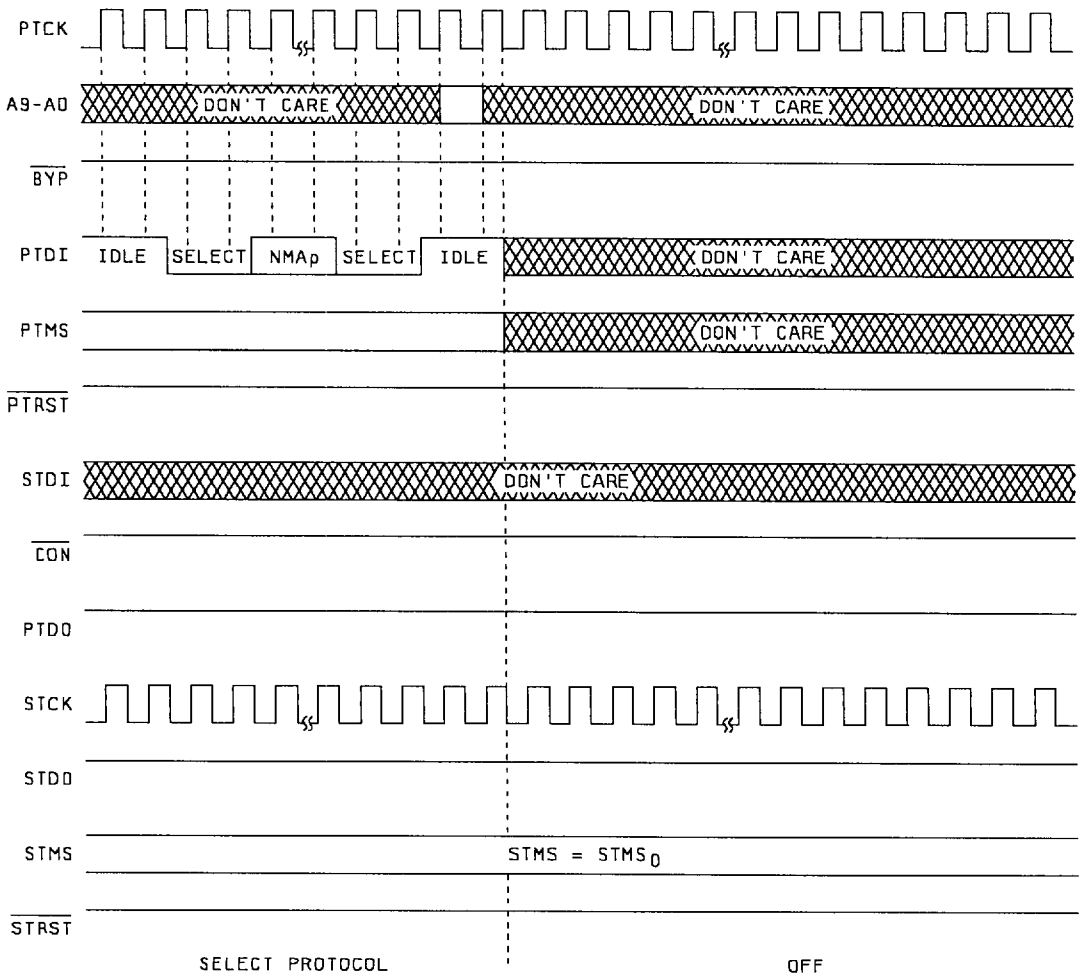


FIGURE 11. Shadow-protocol timing, protocol result = NO MATCH, prior connect status = OFF.



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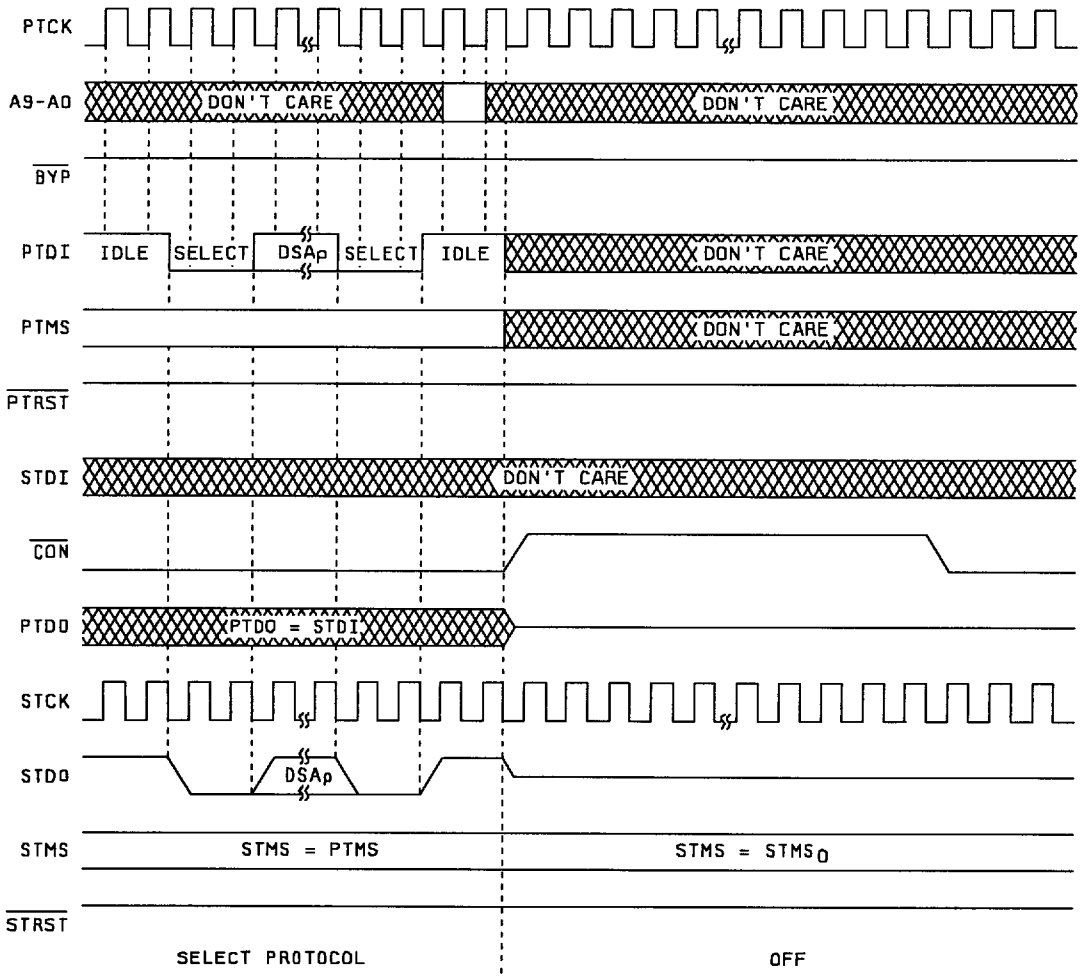


FIGURE 12. Shadow-protocol timing, protocol result = DISCONNECT, prior connect status = ON.



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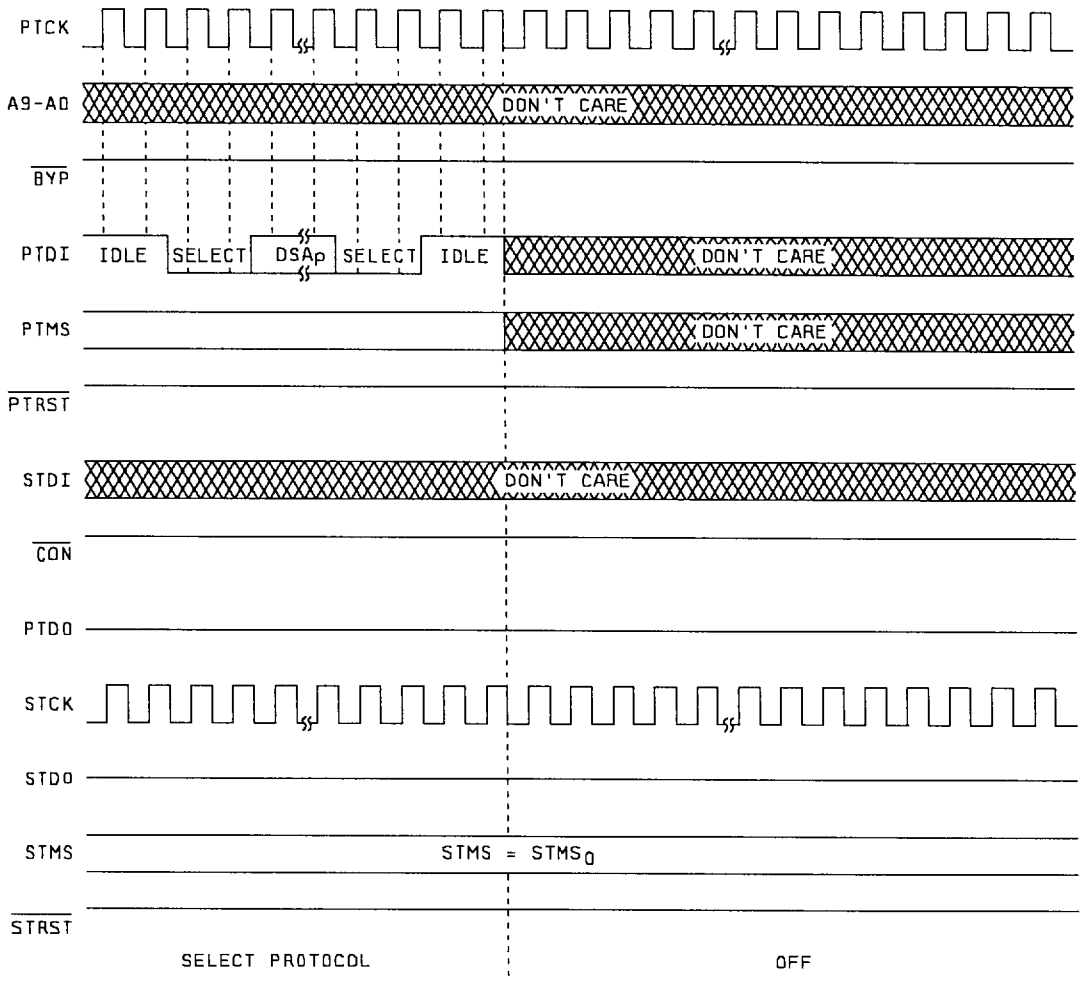


FIGURE 13. Shadow-protocol timing, protocol result = DISCONNECT, prior connect status = OFF.



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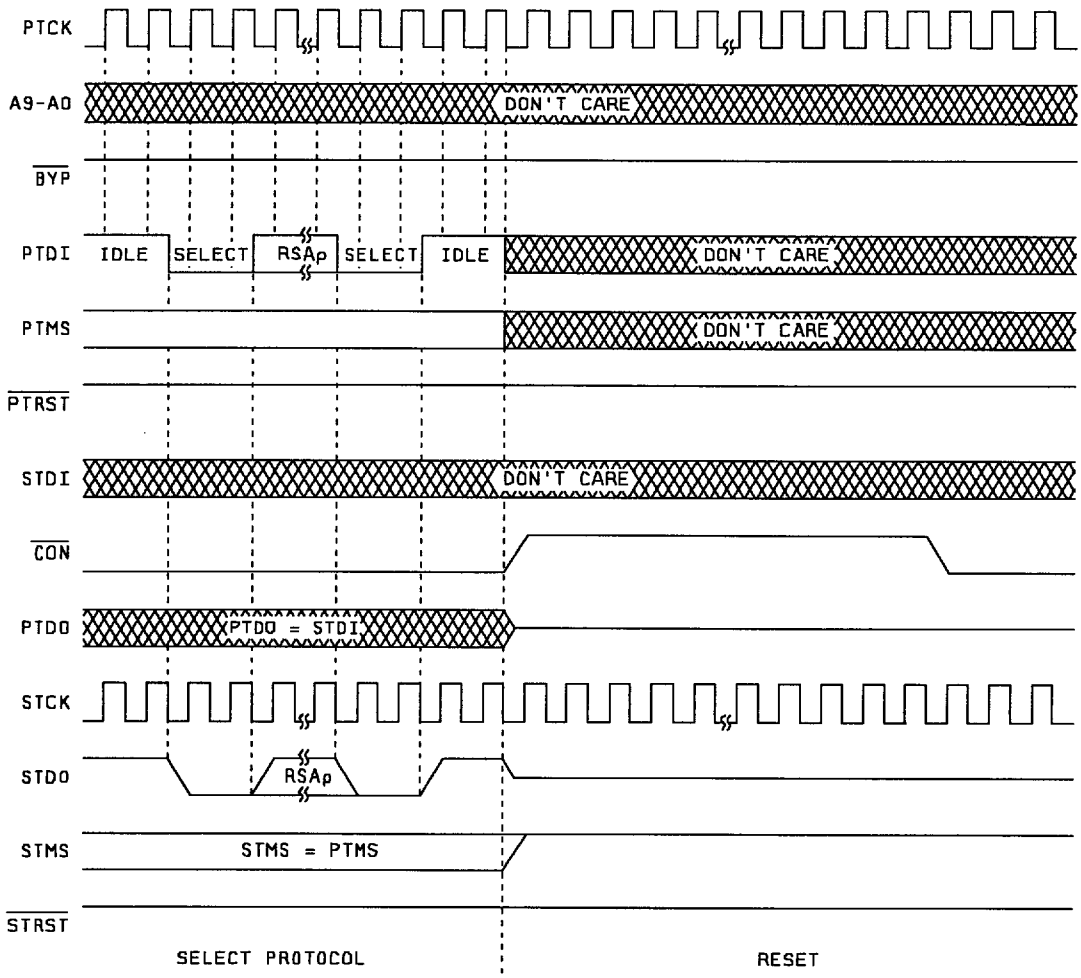


FIGURE 14. Shadow-protocol timing, protocol result = RESET, prior connect status = ON.



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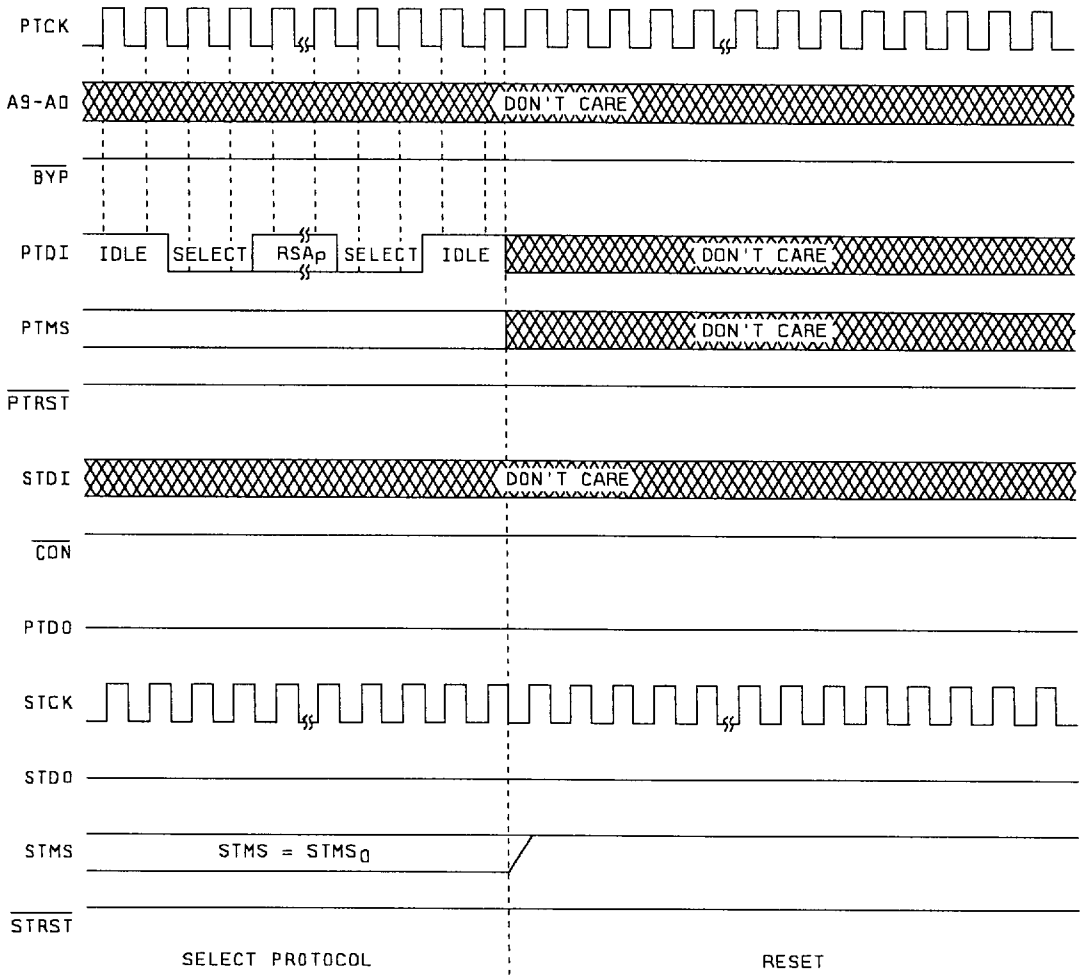


FIGURE 15. Shadow-protocol timing, protocol result = RESET, prior connect status = OFF.



9004708 0033579 033

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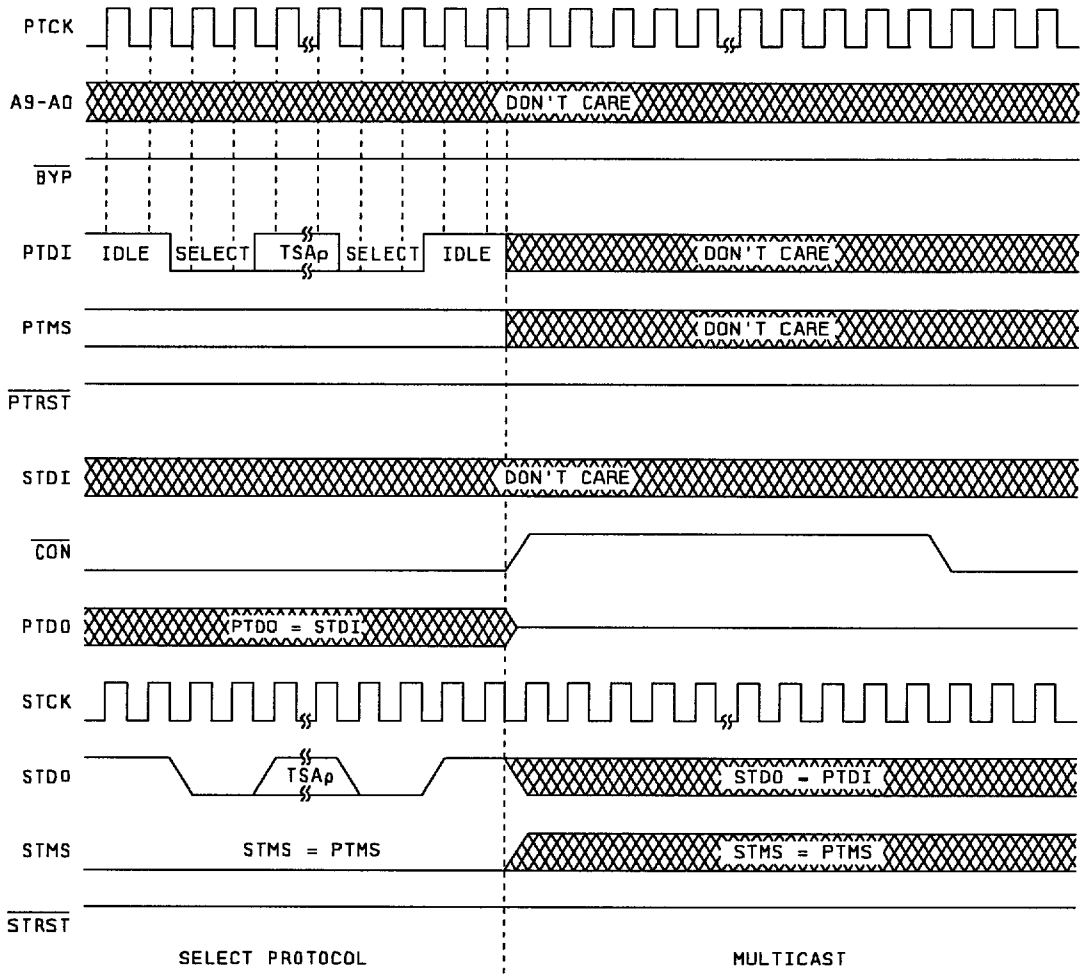


FIGURE 16. Protocol result = TEST SYNCHRONIZATION, prior connect status = ON.



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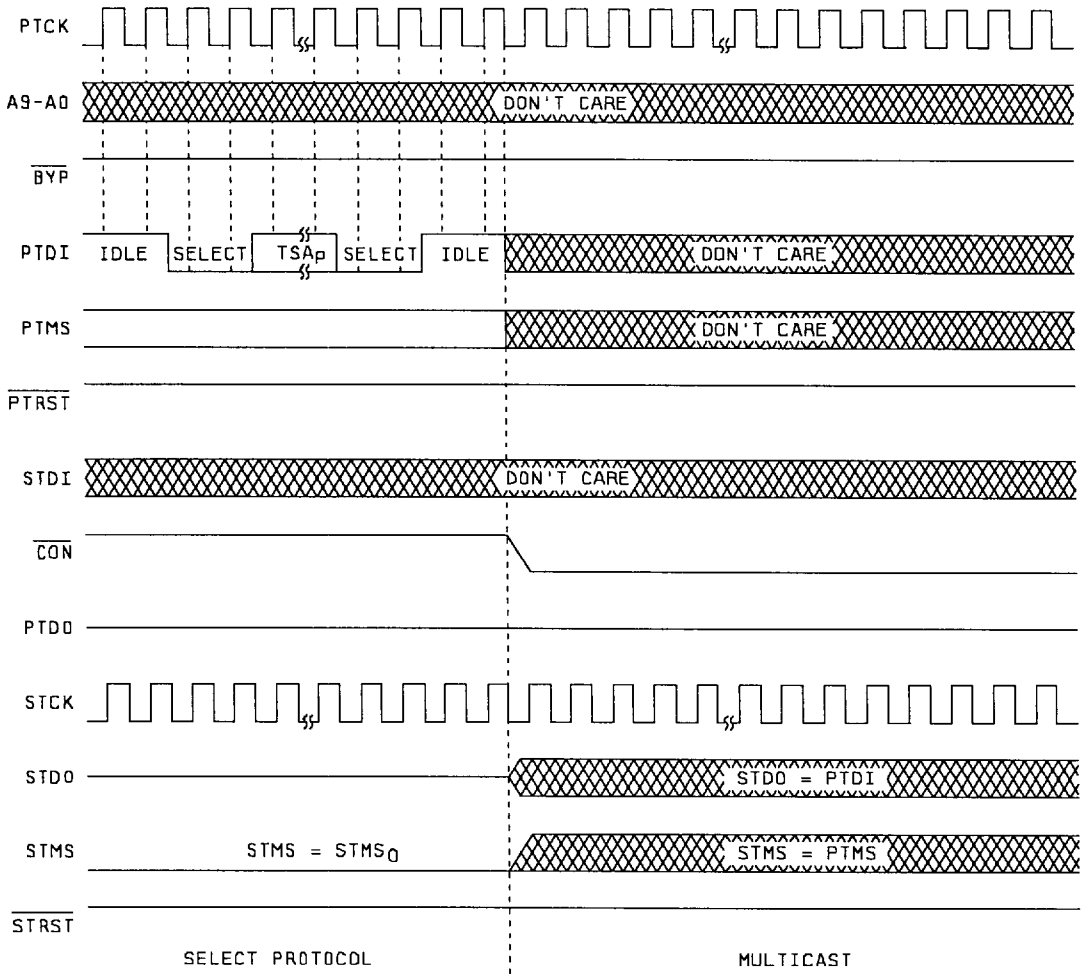


FIGURE 17. Protocol result = TEST SYNCHRONIZATION, prior connect status = OFF.



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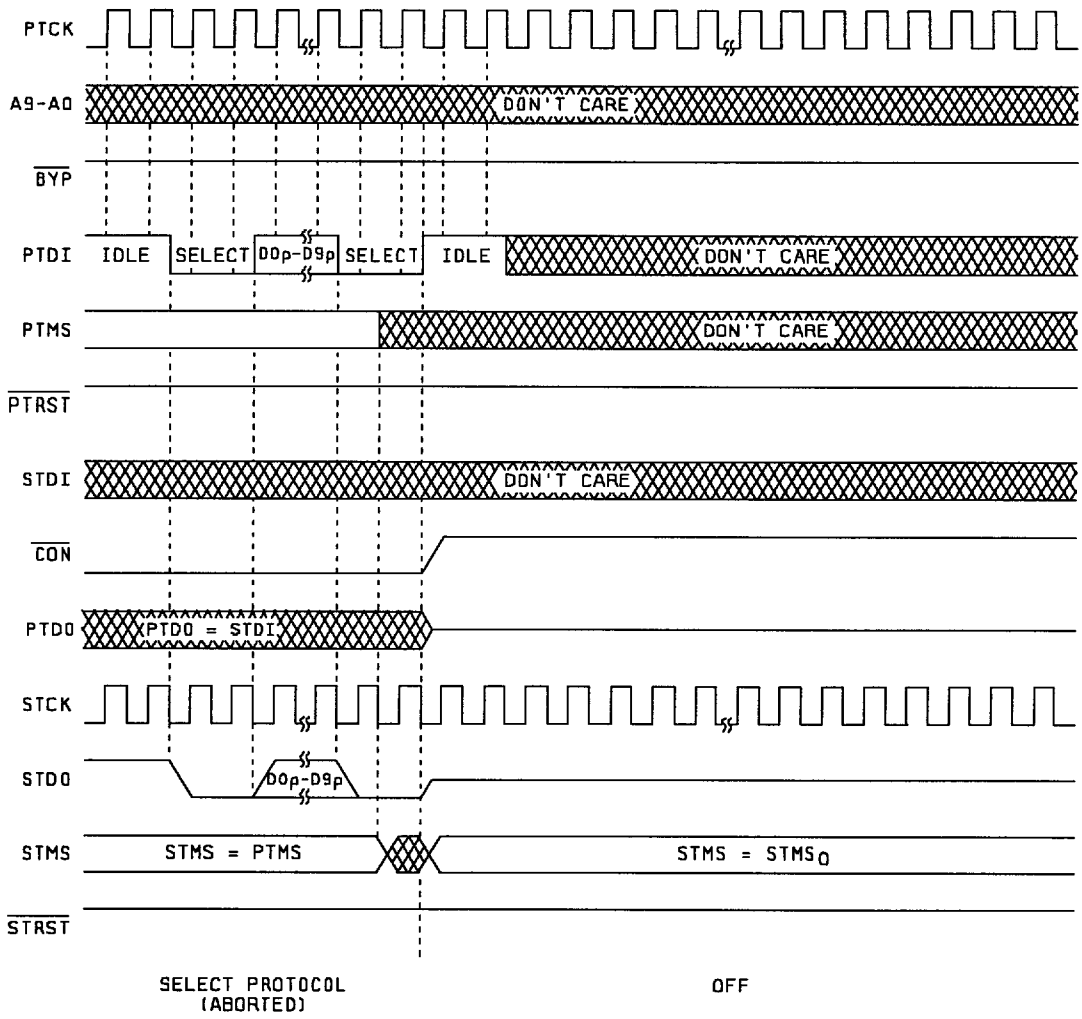


NOTE: The position of PTMS shown in this figure is only one of many that would produce protocol result hard error.

FIGURE 18. Protocol result = HARD ERROR (PTMS change during select protocol), prior connect status = ON.



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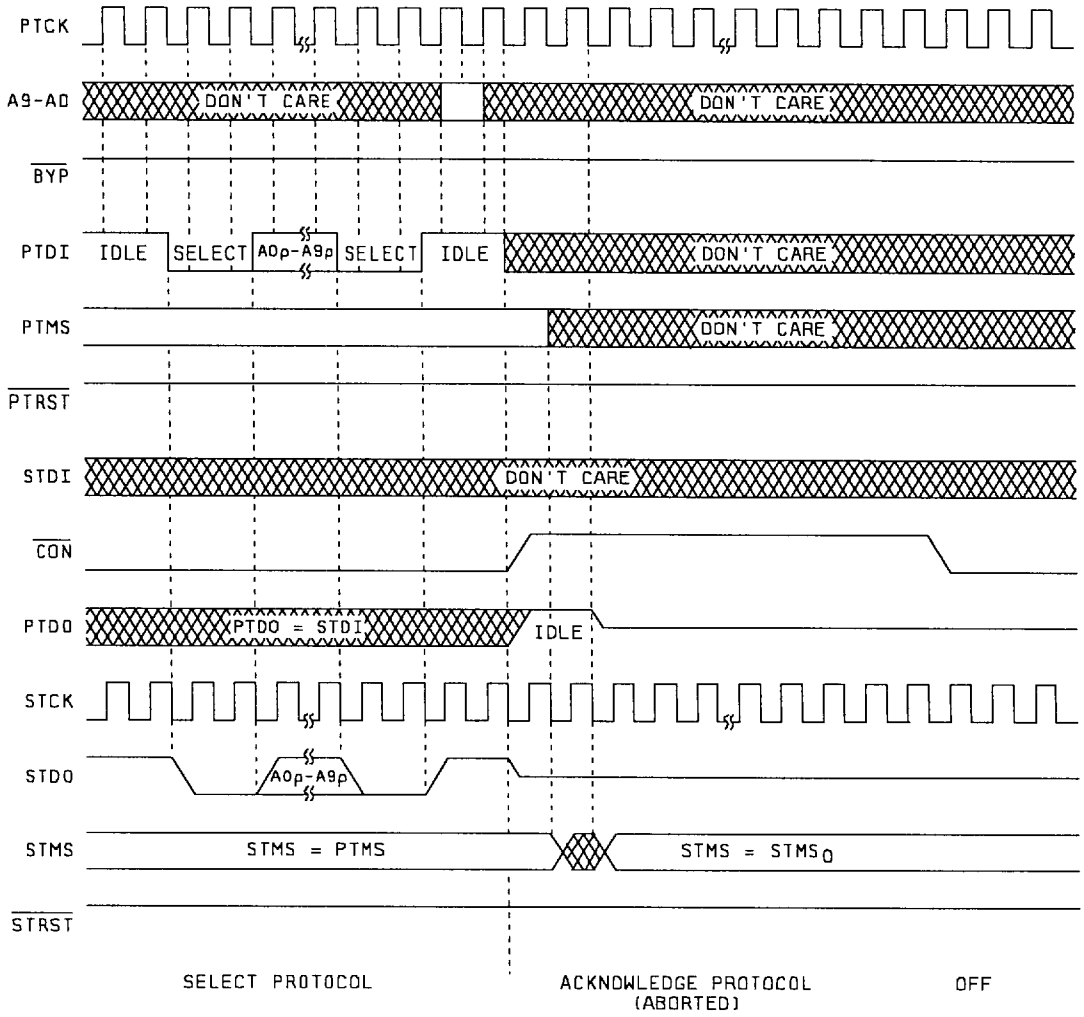


NOTE: The position of PTMS shown in this figure is only one of many that would produce protocol result hard error

FIGURE 19. Protocol result = HARD ERROR (PTMS change during acknowledge protocol), prior connect status = ON.



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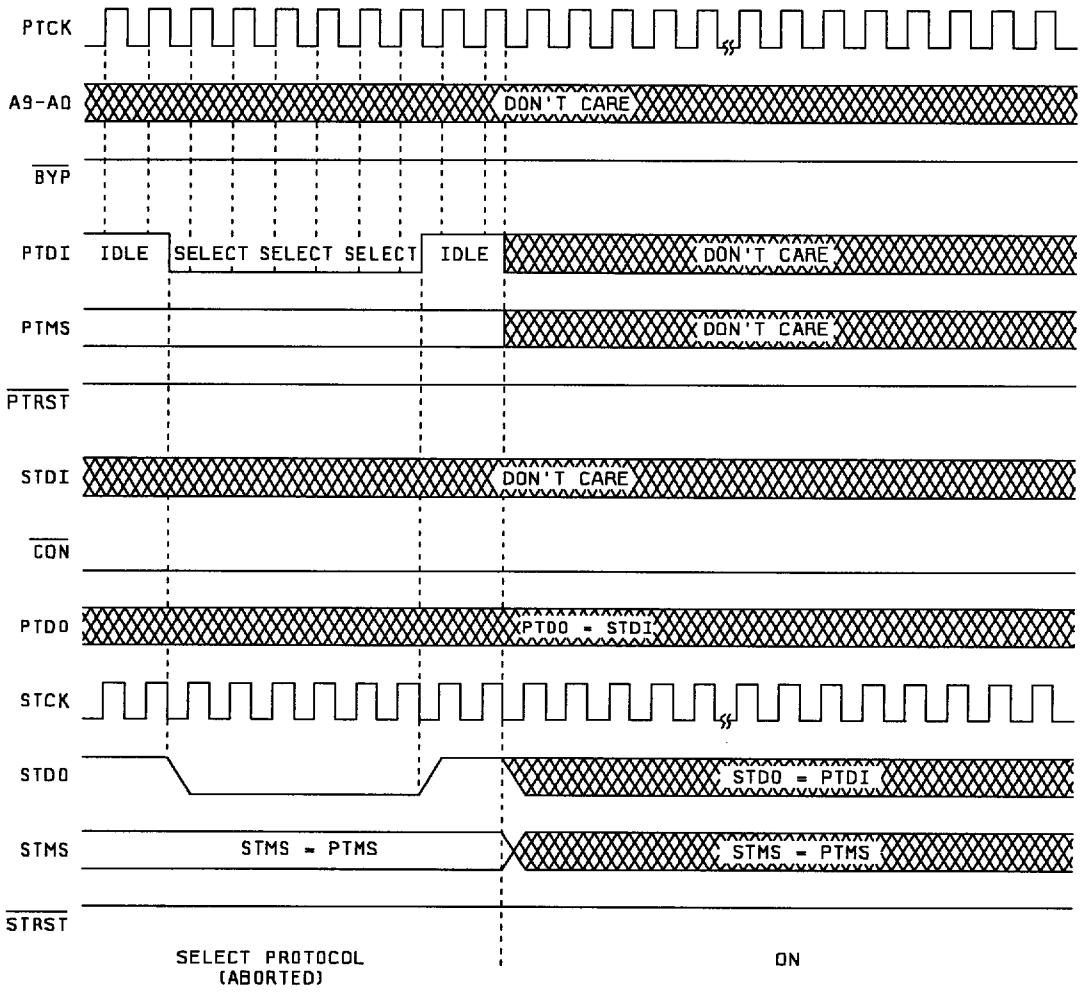


NOTE: The sequence of PTDI bits shown in this figure is only one of many that would produce protocol result soft error.

FIGURE 20. Protocol result = SOFT ERROR, prior connect status = ON.



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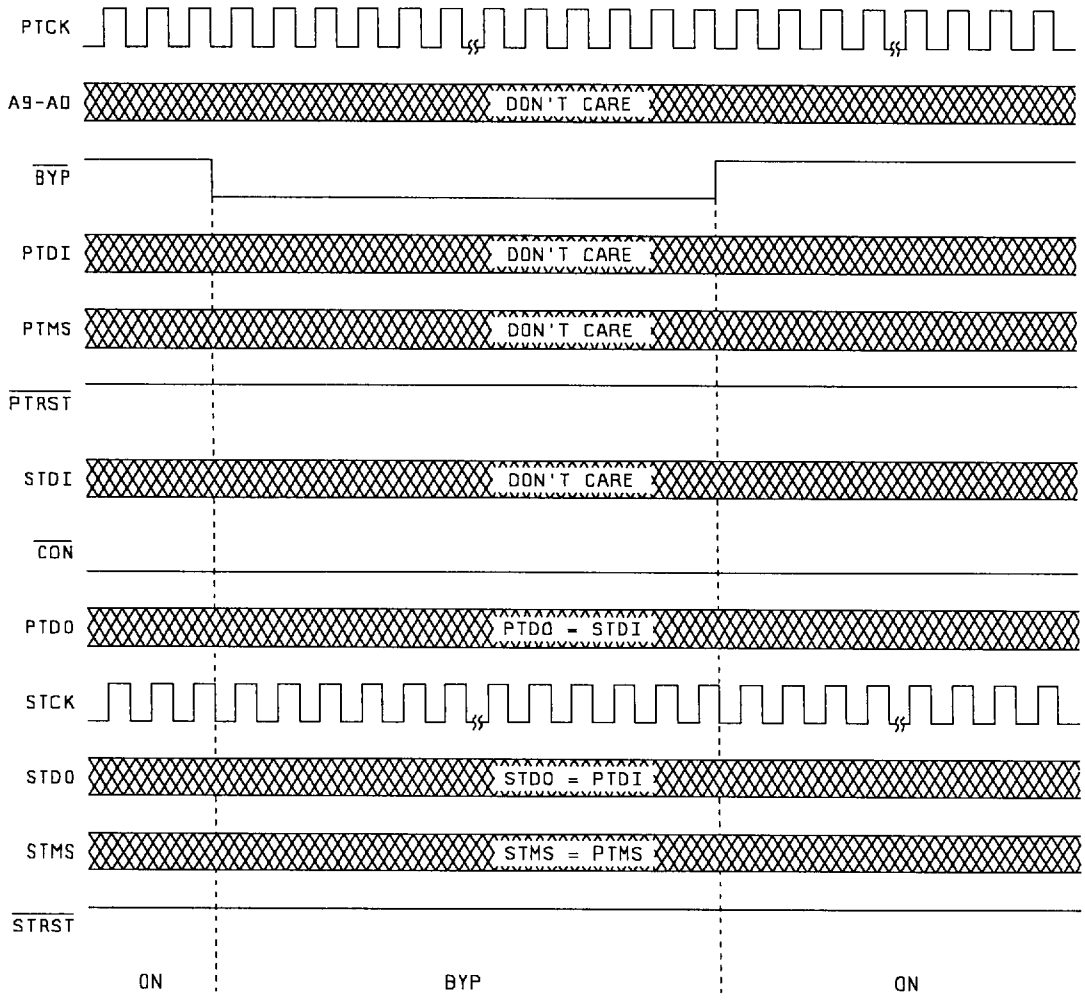


FIGURE 21. Protocol-bypass timing, prior connect status = ON.



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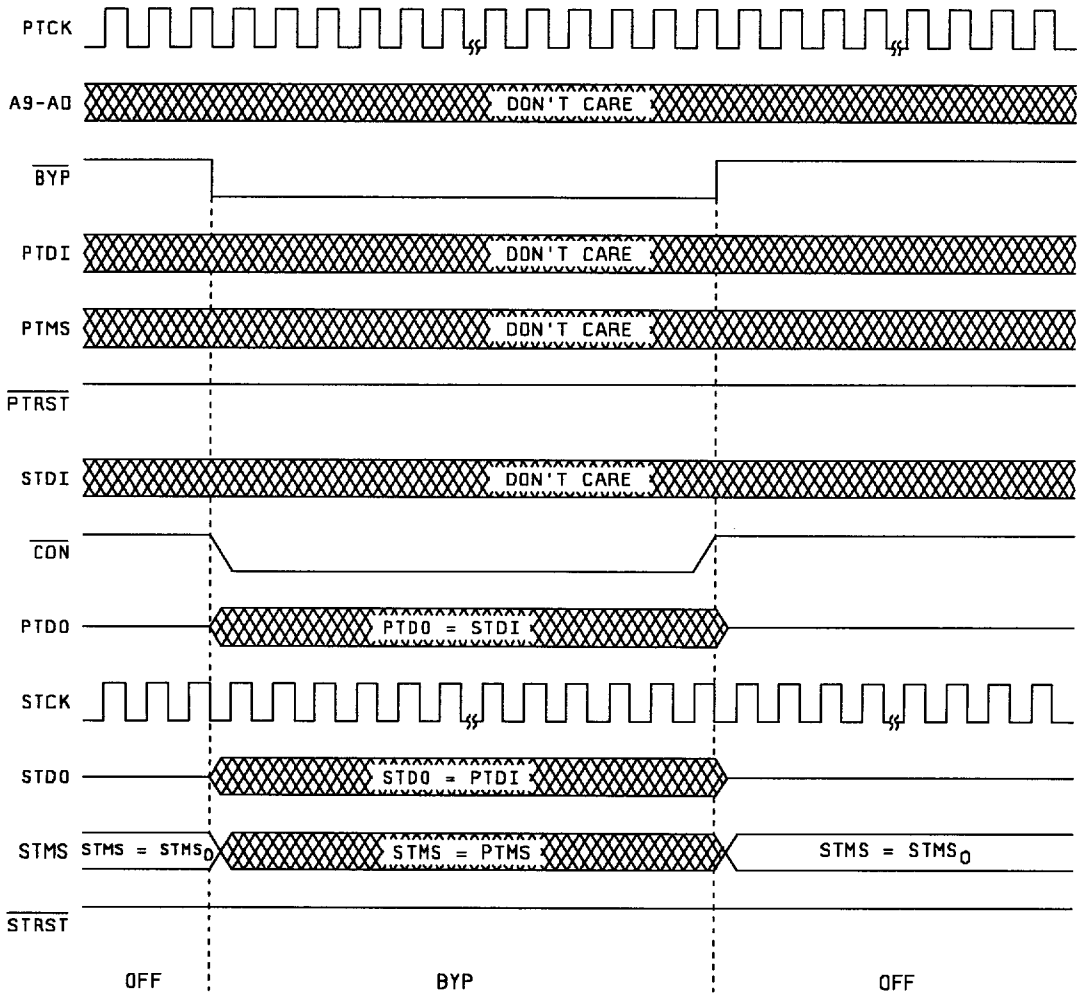


FIGURE 22. Protocol-bypass timing, prior connect status = OFF.



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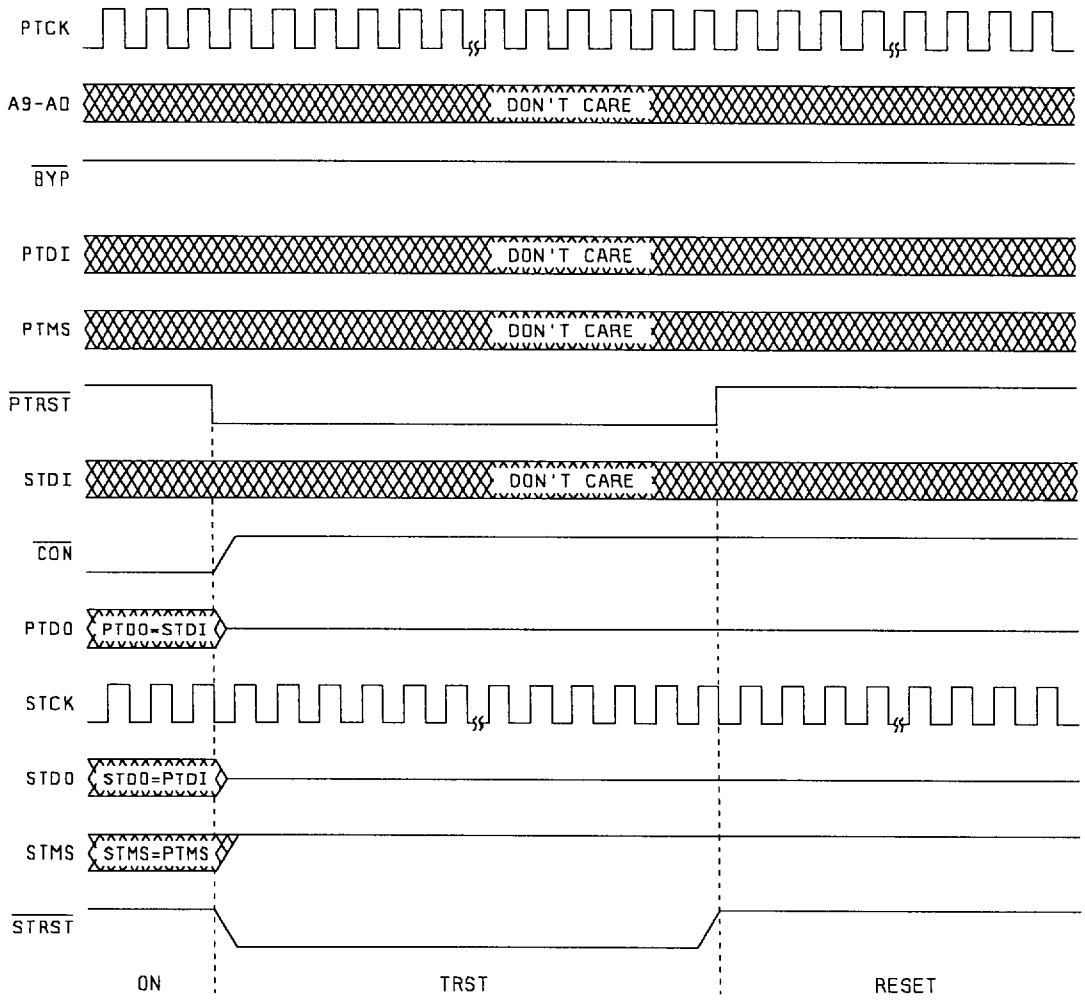


FIGURE 23. Asynchronous reset timing, prior connect status = ON.



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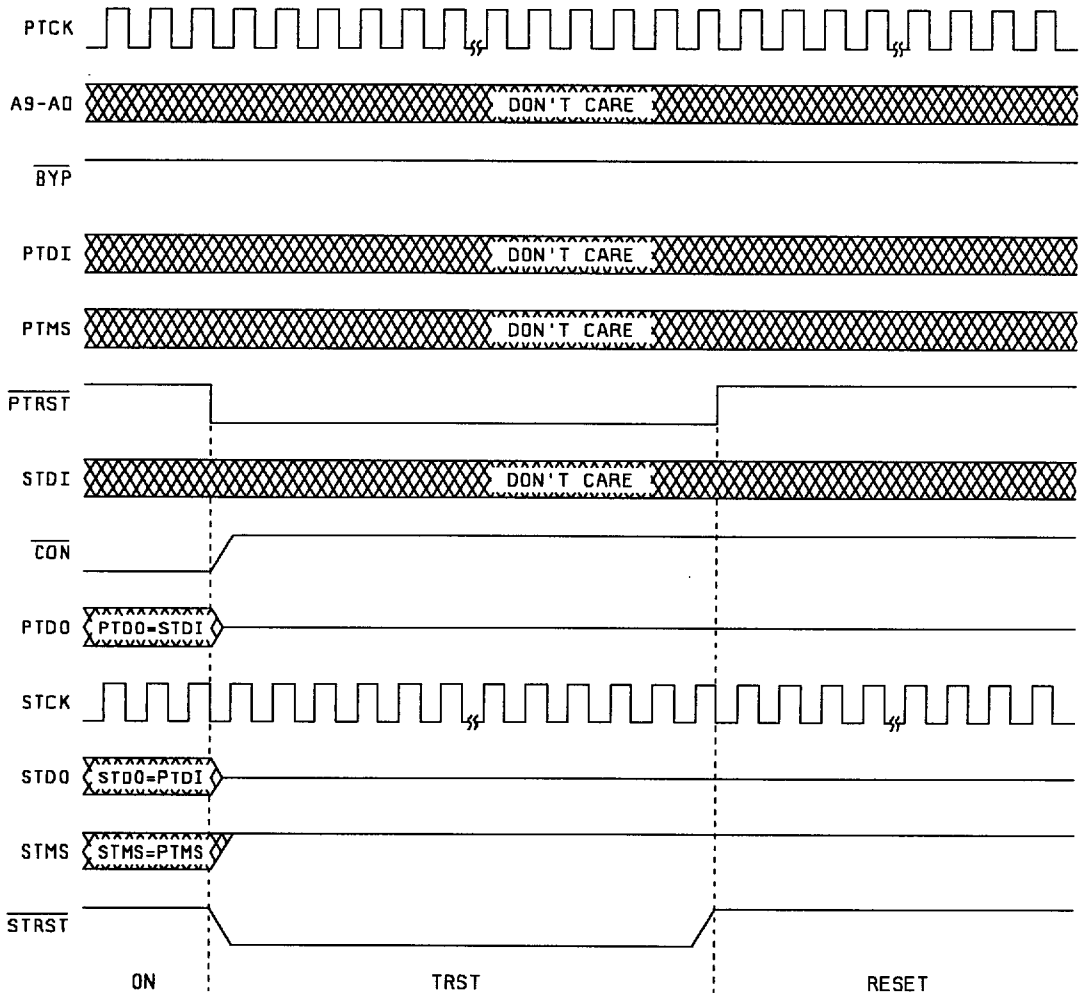


FIGURE 24. Asynchronous reset timing, prior connect status = OFF.



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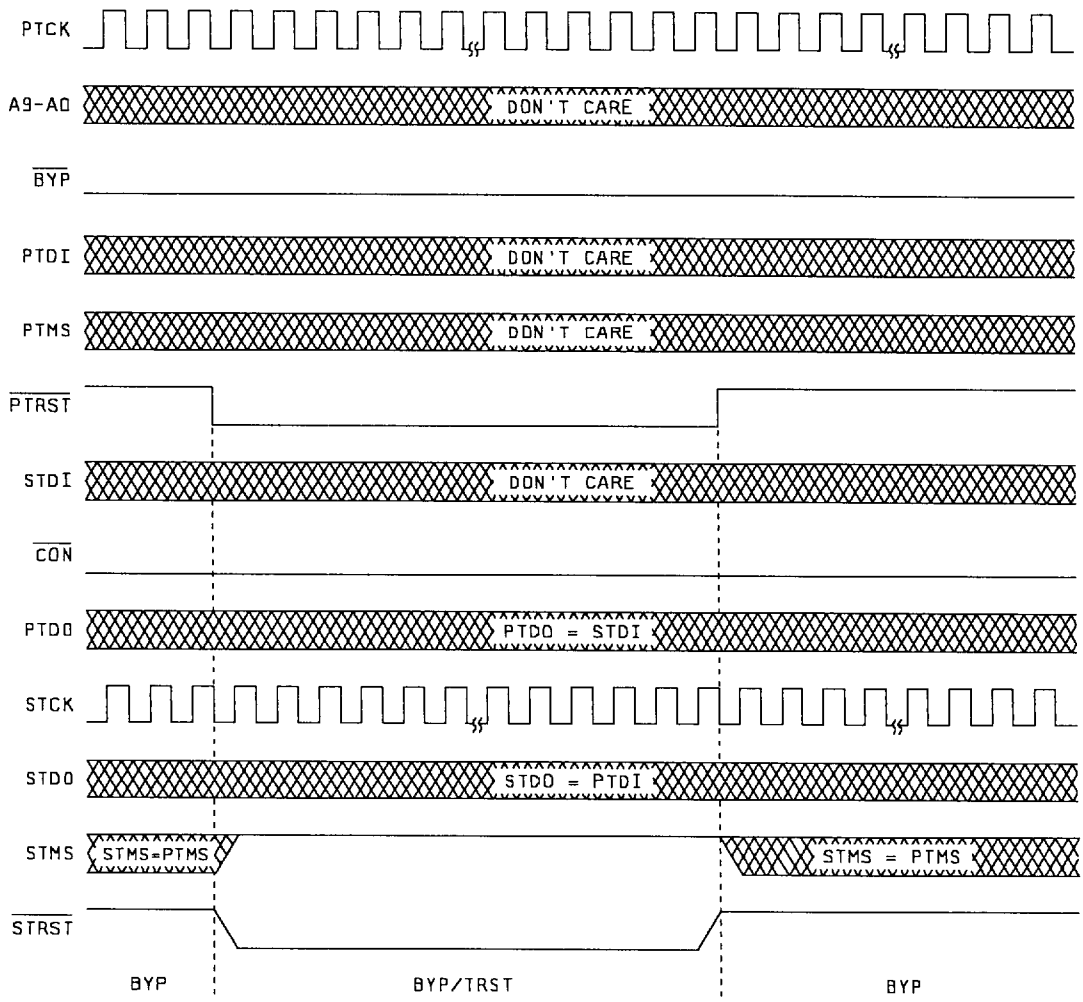


FIGURE 25. Asynchronous reset timing, BYP = L.



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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).



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TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - | 1 |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 2/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. $C_{IN}$ and COUT shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ and $C_{OUT}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz The DC bias for the pin under test ($V_{BIAS}$) = 2.5 V or 3.0 V. For $C_{IN}$ and $C_{OUT}$, test all applicable pins on five devices with zero failures.

For $C_{IN}$ and $C_{OUT}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the $C_{IN}$ and $C_{OUT}$ tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.



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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A$ = +125°C minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.




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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.



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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-10-20

Approved sources of supply for SMD 5962-96812 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9681201QLA | 01295 | SNJ54ABT8996JT |
| 5962-9681201QKA | 01295 | SNJ54ABT8996W |
| 5962-9681201Q3A | 01295 | SNJ54ABT8996FK |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments Incorporated<br>13500 N. Central Expressway<br>P.O. Box 655303<br>Dallas, TX 75265<br>Point of contact: I-20 at FM 1788<br>Midland, TX 79711-0448 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.



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