FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11221-1E

MEMORY
CMOS
2 M × 64 BITS HYPER PAGE MODE DRAM MODULE

MB8502E064AB-60/-70

Buffered, 2 M × 64 BITS Hyper Page Mode DRAM Module, 5 V, 1-bank

PRELIMINARY

■ DESCRIPTION

The Fujitsu MB8502E064AB is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB8117805A devices. The MB8502E064AB is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8502E064AB are the same as the MB8117805A which features hyper page mode (EDO) operation. For ease of memory expansion, the MB8502E064AB is offered in an 168-pin Dual In-line Memory Module package (DIMM).

■ PRODUCT LINE & FEATURES

Parameter		MB8502E064AB-60	MB8502E064AB-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	124 ns min.
Address Access Time		35 ns max.	40 ns max.
$\overline{CAS}$ Access Time		20 ns max.	22 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Power Dissipation	Operating Mode	6600 mW max.	6105 mW max.
	Standby Mode	440 mW max.	440 mW max.

- Conformed to 8-Byte DIMM JEDEC standard
- Organization: 2,097,152 words × 64 bits
- Module Size: 1.00” (height) × 5.25” (length) × 0.350” (thick)
- Memory: MB8117805A (2 M × 8, 2 K ref.), 8 pcs
- TI’s Input Buffers, 2 pcs
- TI’s Input Driver for Buffered PD, 1 pc
- Parallel Presence Detect
- 5.0 V + 10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Hyper Page Operation (EDO)
- $\overline{RAS}$-only Refresh / $\overline{CAS}$-before-$\overline{RAS}$ Refresh
- Package and Ordering Information:
  168-pin DIMM, order as
  MB8502E064AB-××DG (DG = Gold Pad)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

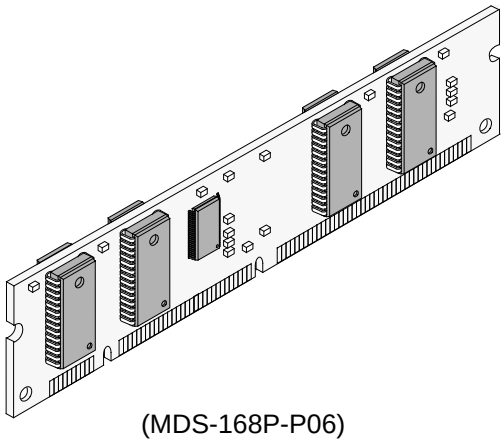
■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	10	W
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

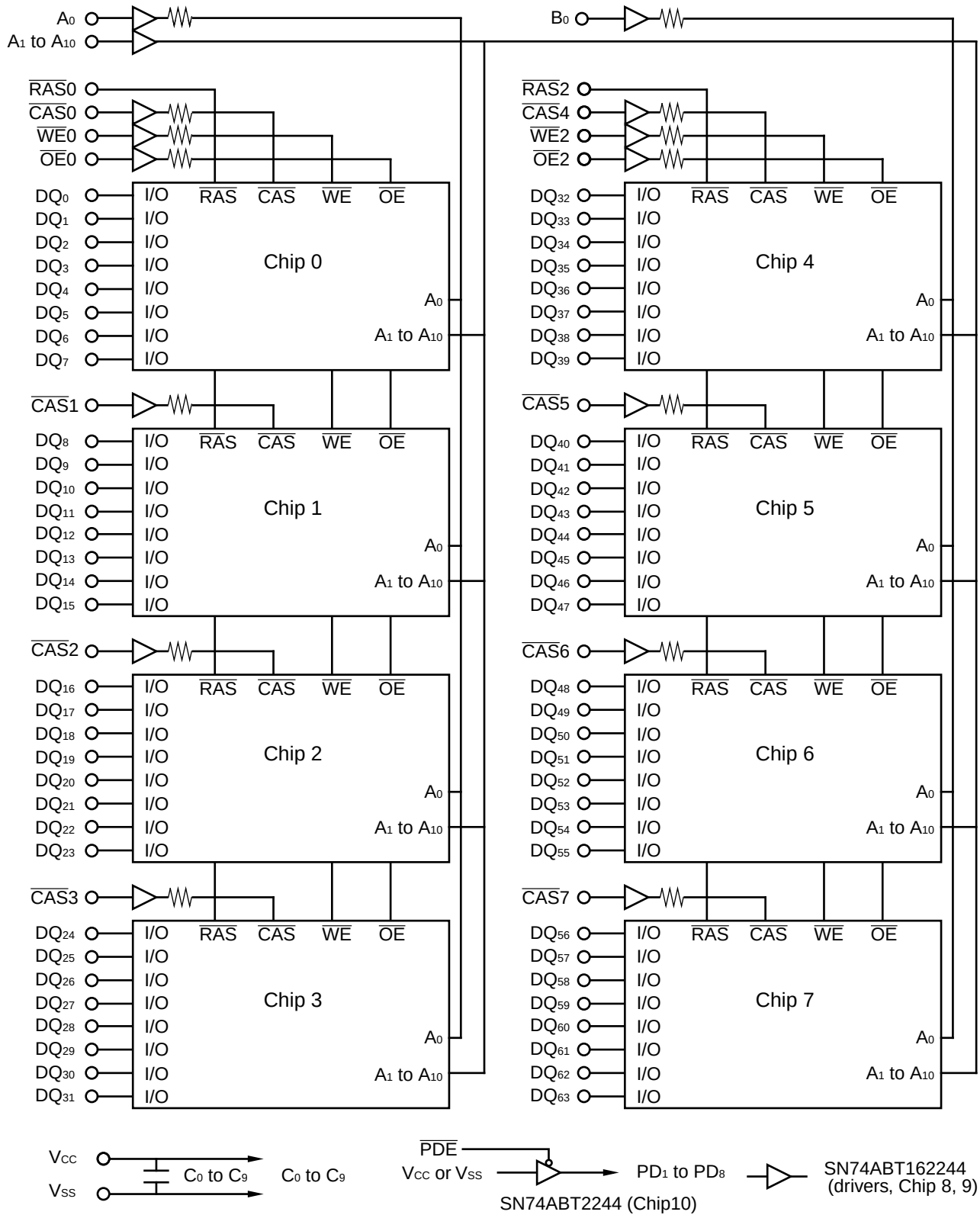
■ PACKAGE

168-pin plastic DIMM (socket type)



(MDS-168P-P06)

Fig. 1 – BLOCK DIAGRAM



■ PIN ASSIGNMENTS

Pin No.	MB8502E064AB	Pin No.	MB8502E064AB	Pin No.	MB8502E064AB	Pin No.	MB8502E064AB
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ_0	44	$\overline{OE}2$	86	DQ_{32}	128	N.C.
3	DQ_1	45	$\overline{RAS}2$	87	DQ_{33}	129	N.C.
4	DQ_2	46	$\overline{CAS}4$	88	DQ_{34}	130	$\overline{CAS}5$
5	DQ_3	47	$\overline{CAS}6$	89	DQ_{35}	131	$\overline{CAS}7$
6	V_{CC}	48	$\overline{WE}2$	90	V_{CC}	132	$\overline{PDE}$
7	DQ_4	49	V_{CC}	91	DQ_{36}	133	V_{CC}
8	DQ_5	50	N.C.	92	DQ_{37}	134	N.C.
9	DQ_6	51	N.C.	93	DQ_{38}	135	N.C.
10	DQ_7	52	DQ_{16}	94	DQ_{39}	136	DQ_{48}
11	N.C.	53	DQ_{17}	95	N.C.	137	DQ_{49}
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ_8	55	DQ_{18}	97	DQ_{40}	139	DQ_{50}
14	DQ_9	56	DQ_{19}	98	DQ_{41}	140	DQ_{51}
15	DQ_{10}	57	DQ_{20}	99	DQ_{42}	141	DQ_{52}
16	DQ_{11}	58	DQ_{21}	100	DQ_{43}	142	DQ_{53}
17	DQ_{12}	59	V_{CC}	101	DQ_{44}	143	V_{CC}
18	V_{CC}	60	DQ_{22}	102	V_{CC}	144	DQ_{54}
19	DQ_{13}	61	N.C.	103	DQ_{45}	145	N.C.
20	DQ_{14}	62	N.C.	104	DQ_{46}	146	N.C.
21	DQ_{15}	63	N.C.	105	DQ_{47}	147	N.C.
22	N.C.	64	N.C.	106	N.C.	148	N.C.
23	V_{SS}	65	DQ_{23}	107	V_{SS}	149	DQ_{55}
24	N.C.	66	N.C.	108	N.C.	150	N.C.
25	N.C.	67	DQ_{24}	109	N.C.	151	DQ_{56}
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{WE}0$	69	DQ_{25}	111	N.C.	153	DQ_{57}
28	$\overline{CAS}0$	70	DQ_{26}	112	$\overline{CAS}1$	154	DQ_{58}
29	$\overline{CAS}2$	71	DQ_{27}	113	$\overline{CAS}3$	155	DQ_{59}
30	$\overline{RAS}0$	72	DQ_{28}	114	N.C.	156	DQ_{60}
31	$\overline{OE}0$	73	V_{CC}	115	N.C.	157	V_{CC}
32	V_{SS}	74	DQ_{29}	116	V_{SS}	158	DQ_{61}
33	A_0	75	DQ_{30}	117	A_1	159	DQ_{62}
34	A_2	76	DQ_{31}	118	A_3	160	DQ_{63}
35	A_4	77	N.C.	119	A_5	161	N.C.
36	A_6	78	V_{SS}	120	A_7	162	V_{SS}
37	A_8	79	PD_1	121	A_9	163	PD_2
38	A_{10}	80	PD_3	122	N.C.	164	PD_4
39	N.C.	81	PD_5	123	N.C.	165	PD_6
40	V_{CC}	82	PD_7	124	V_{CC}	166	PD_8
41	N.C.	83	ID_0	125	N.C.	167	ID_1
42	N.C.	84	V_{CC}	126	B_0	168	V_{CC}

■ PIN DESCRIPTIONS

Symbol	Function	Input/Output	Pin Count
A_0 to A_{10}, B_0	Address Input	Input	12
$\overline{RAS}0$ and $\overline{RAS}2$	Row Address Strobe	Input	2
$\overline{CAS}0$ to $\overline{CAS}7$	Column Address Strobe	Input	8
$\overline{WE}0$ and $\overline{WE}2$	Write Enable	Input	2
$\overline{OE}0$ and $\overline{OE}2$	Output Enable	Input	2
DQ_0 to DQ_{63}	Data Input / Data Output	Input/Output	64
PD_1 to PD_8	Presence Detect	Output	8
ID_0 and ID_1	ID bit	Output	2
$\overline{PDE}$	Presence Detect Enable	Input	1
V_{CC}	Power Supply	—	16
V_{SS}	Ground	—	16
N.C.	No Connection	—	16

■ PRESENCE DETECT (PD) / ID DEFINITION

Symbol	MB8502E064AB-60	MB8502E064AB-70	Description of PD / ID
PD_1	H	H	MODULE DENSITY, DRAM ORGANIZATION AND ADDRESSING; Module Density: 16 MB, Number of Bank: 1 Bank Module Configuration: 2 M × 64 Mounted DRAM Configuration: 2 M × 8 DRAM Address (Row / Column): 11/10
PD_2	L	L	
PD_3	L	L	
PD_4	H	H	
PD_5	H	H	EDO DETECTION; Hyper Page Mode: PD_5 = H
PD_6	H	L	MODULE SPEED; 60 ns: PD_6 = H, PD_7 = H 70 ns: PD_6 = L, PD_7 = H
PD_7	H	H	
PD_8	H	H	ECC/PARITY DETECTION; (parity): PD_8 = H
ID_0	L	L	MODULE TYPE; × 64 (parity): ID_0 = L
ID_1	H	H	REFRESH MODE; Self Refresh: ID_1 = H

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{CC} = +5.0 V)

Parameter	Symbol	Max.	Unit
Input Capacitance, Address	C_{IN1}	20	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}	50	pF
Input Capacitance, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN3}	20	pF
Input/Output Capacitance, DQ_0 to DQ_{63}	C_{DQ}	20	pF

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.0	V
Input Low Voltage, All Inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

* : Undershoots of up to –1.5 volts with a pulse width not exceeding 10 ns are acceptable.

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value		Unit
					Min.	Max.	
Output High Voltage	*1		V_{OH}	I_{OH} = –5.0 mA	2.4	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = +4.2 mA	—	0.4	V
Input Leakage Current		$\overline{RAS}$	$I_{I(L)}$	0 V ≤ V_{IN} ≤ 5.5 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, V_{SS} = 0 V, All other pins not under test = 0 V	–30	30	µA
		Others			–10	10	
Output Leakage Current			$I_{O(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, Data out disabled	–10	10	µA
Operating Current (Average Power Supply Current)	*2	MB8502E064AB-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min	—	1200	mA
		MB8502E064AB-70			—	1110	
Standby Current (Power Supply Current)	*2	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{PDE}$ = V_{IH}	—	80	mA
		CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ = $\overline{PDE}$ ≥ V_{CC} –0.2 V	—	69	
Refresh Current #1 (Average Power Supply Current)	*2	MB8502E064AB-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min	—	1200	mA
		MB8502E064AB-70			—	1110	
Hyper Page Mode Current	*2	MB8502E064AB-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{HPC} = min	—	1200	mA
		MB8502E064AB-70			—	1110	
Refresh Current #2 (Average Power Supply Current)	*2	MB8502E064AB-60	I_{CC5}	$\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min	—	1120	mA
		MB8502E064AB-70			—	1030	
Refresh Current #3 (Average Power Supply Current)			I_{CC9}	Self Refresh; A_0 to A_{10}, B_0, $\overline{WE}$, $\overline{OE}$, $\overline{PDE}$ ≥ V_{CC} –2.1 V	—	30	mA

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3 V.
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8502E064AB-60		MB8502E064AB-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	32.8	—	32.8	ms
2	Random Read/Write Cycle Time		t_{RC}	104	—	124	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	138	—	162	—	ns
4	Access Time from $\overline{RAS}$	*4,7	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	*5,7	t_{CAC}	—	20	—	22	ns
6	Column Address Access Time	*6,7	t_{AA}	—	35	—	40	ns
7	Output Hold Time		t_{OH}	5	—	5	—	ns
8	Output Hold Time from $\overline{CAS}$		t_{OHC}	7		7		ns
9	Output Buffer Turn on Delay Time		t_{ON}	2	—	2	—	ns
10	Output Buffer Turn off Delay Time	*8	t_{OFF}	—	20	—	22	ns
11	Output Buffer Turn off Delay Time from $\overline{RAS}$	*8	t_{OFR}	—	15	—	17	ns
12	Output Buffer Turn off Delay Time from $\overline{WE}$	*8	t_{WEZ}	—	20	—	22	ns
13	Transition Time		t_T	1	16	1	16	ns
14	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	50	—	ns
15	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
16	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	22	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	ns
18	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*9,10	t_{RCD}	12	45	12	53	ns
19	$\overline{CAS}$ Pulse Width		t_{CAS}	10	—	13	—	ns
20	$\overline{CAS}$ Hold Time		t_{CSH}	38	—	48	—	ns
21	$\overline{CAS}$ Precharge Time (Normal)	*17	t_{CPN}	10	—	10	—	ns
22	Row Address Set Up Time		t_{ASR}	5	—	5	—	ns
23	Row Address Hold Time		t_{RAH}	8	—	8	—	ns
24	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
25	Column Address Hold Time		t_{CAH}	10	—	10	—	ns
26	Column Address Hold Time from $\overline{RAS}$		t_{AR}	22	—	22	—	ns
27	$\overline{RAS}$ to Column Address Delay Time	*11	t_{RAD}	10	35	10	40	ns
28	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	35	—	40	—	ns
29	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	23	—	28	—	ns
30	Read Command Set Up Time		t_{RCS}	5	—	5	—	ns

(Continued)

No.	Parameter	Notes	Symbol	MB8502E064AB-60		MB8502E064AB-70		Unit
				Min.	Max.	Min.	Max.	
31	Read Command Hold Time Referenced to $\overline{RAS}$	*12	t_{RRH}	–2	—	–2	—	ns
32	Read Command Hold Time Referenced to $\overline{CAS}$	*12	t_{RCH}	0	—	0	—	ns
33	Write Command Set Up Time	*13,18	t_{WCS}	0	—	0	—	ns
34	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
35	Write Command Hold Time from $\overline{RAS}$		t_{WCR}	22	—	22	—	ns
36	$\overline{WE}$ Pulse Width		t_{WP}	8	—	8	—	ns
37	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	20	—	22	—	ns
38	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	10	—	13	—	ns
39	DIN Set Up Time		t_{DS}	–2	—	–2	—	ns
40	DIN Hold Time		t_{DH}	15	—	15	—	ns
41	Data Hold Time from $\overline{RAS}$		t_{DHR}	24	—	24	—	ns
42	$\overline{RAS}$ to $\overline{WE}$ Delay Time	*18	t_{RWD}	75	—	87	—	ns
43	$\overline{CAS}$ to $\overline{WE}$ Delay Time	*18	t_{CWD}	32	—	36	—	ns
44	Column Address to $\overline{WE}$ Delay Time	*18	t_{AWD}	47	—	54	—	ns
45	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	3	—	3	—	ns
46	$\overline{CAS}$ Set Up Time (C-B-R Refresh)		t_{CSR}	5	—	5	—	ns
47	$\overline{CAS}$ Hold Time (C-B-R Refresh)		t_{CHR}	12	—	14	—	ns
48	Access Time from $\overline{OE}$	*7	t_{OEA}	—	20	—	22	ns
49	Output Buffer Turn off Delay from $\overline{OE}$	*8	t_{WCZ}	—	20	—	22	ns
50	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{WCL}	15	—	15	—	ns
51	$\overline{OE}$ to $\overline{CAS}$ Lead Time		t_{COL}	5	—	5	—	ns
52	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	*14	t_{OEH}	5	—	5	—	ns
53	$\overline{OE}$ to Data in Delay Time		t_{OED}	20	—	22	—	ns
54	$\overline{RAS}$ to Data in Delay Time		t_{RDD}	15	—	15	—	ns
55	$\overline{CAS}$ to Data in Delay Time		t_{CDD}	20	—	22	—	ns
56	DIN to $\overline{CAS}$ Delay Time	*15	t_{DZC}	–2	—	–2	—	ns
57	DIN to $\overline{OE}$ Delay Time	*15	t_{DZO}	–2	—	–2	—	ns
58	$\overline{OE}$ Precharge Time		t_{OEP}	8	—	8	—	ns
59	$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$		t_{OECH}	10	—	10	—	ns
60	$\overline{WE}$ Precharge Time		t_{WPZ}	8	—	8	—	ns

(Continued)

No.	Parameter	Notes	Symbol	MB8502E064AB-60		MB8502E064AB-70		Unit
				Min.	Max.	Min.	Max.	
61	$\overline{WE}$ to Data in Delay Time		t_{WED}	20	—	22	—	ns
62	Hyper Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	—	100000	—	200000	ns
63	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	25	—	30	—	ns
64	Hyper Page Mode Read-Modify-Write Cycle Time		t_{HPRWC}	69	—	79	—	ns
65	Access Time from $\overline{CAS}$ Precharge	*7,16	t_{CPA}	—	40	—	45	ns
66	Hyper Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	ns
67	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	40	—	45	—	ns
68	Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	*18	t_{CPWD}	52	—	59	—	ns
69	$\overline{RAS}$ Pulse Width (Self Refresh)	*19	t_{RASS}	100	—	100	—	µs
70	$\overline{RAS}$ Precharge Time (Self Refresh)	*19	t_{RPS}	104	—	124	—	ns
71	$\overline{CAS}$ Hold Time (Self Refresh)	*19	t_{CHS}	–52	—	–52	—	ns

Notes: *1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$- before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

*2. AC characteristics assume t_T = 5 ns.

*3. V_{IH} (min) and V_{IL} (max) are reference levels for measureing the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).

*4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.

*5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*7. Measured with a load equivalent to two TTL loads and 100 pF.

*8. t_{OFF}, t_{OEZ}, t_{OFR} and t_{WEZ} is specified that output buffer change to high-impedance state.

*9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*10. t_{RCD} (min) = t_{RAH} (min) + 2 t_T + t_{ASC} (min).

*11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*14. Assumes that $t_{WCS} < t_{WCS}$ (min).

*15. Either t_{DZC} or t_{DZO} must be satisfied.

*16. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).

*17. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*18. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high-impedance state thoughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} specifications.

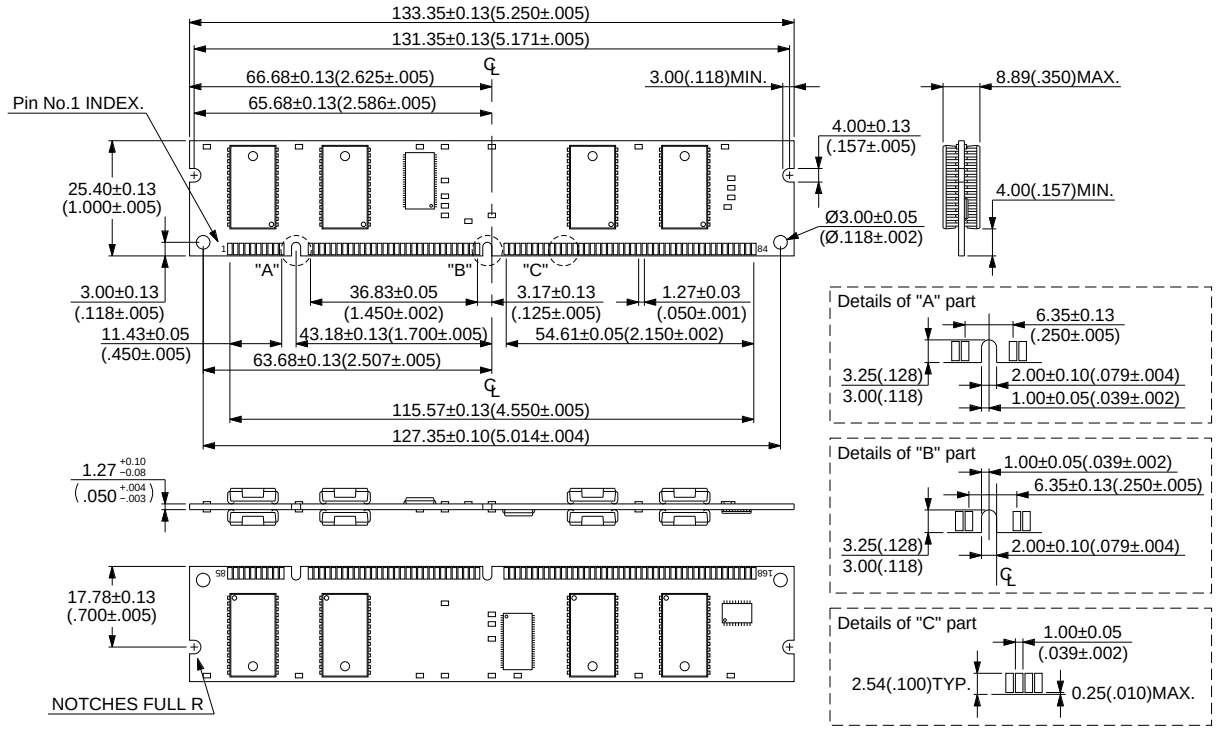
*19. Assumes that self refresh.

*Source: See MB8117805A Data Sheet for details on the electricals.

■ PACKAGE DIMENSIONS

(Suffix: DG)

168 pin, Plastic DIMM
(MDS-168P-P06)



Dimensions in mm(inches).

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FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

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