3.3V CMOS PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET, 5 VOLT TOLERANT I/O

IDT74LVC163A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.635mm pitch QSOP, 0.65mm pitch SSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of – 40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC163A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

• 5V and 3.3V mixed voltage systems
• Data communication and telecommunication systems

DESCRIPTION:

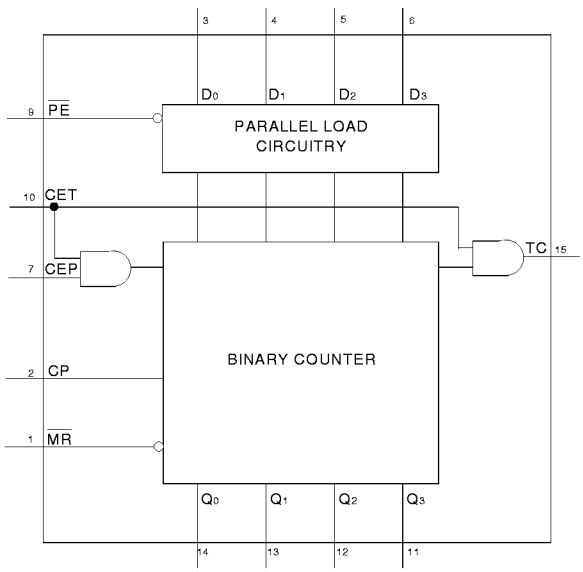
The LVC163A is a synchronous presettable binary counter, which features an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all the flip-flops clocked simultaniously on the positive-going edge of the clock (CP). Outputs (Q_0 to Q_3) may be preset to a high or low level. A low level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to low level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for PE are met).

This action occurs regardless of the levels of CP, $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

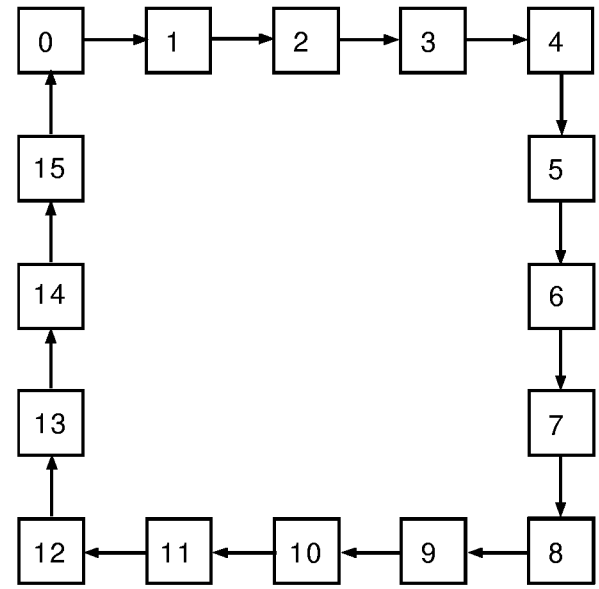
The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be high to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a high output pulse of a duration approximately equal to a high level output of Q_0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{tp_{(max)}\,(CP\ to\ TC) + t_{su}\,(CEP\ to\ CP)}$$

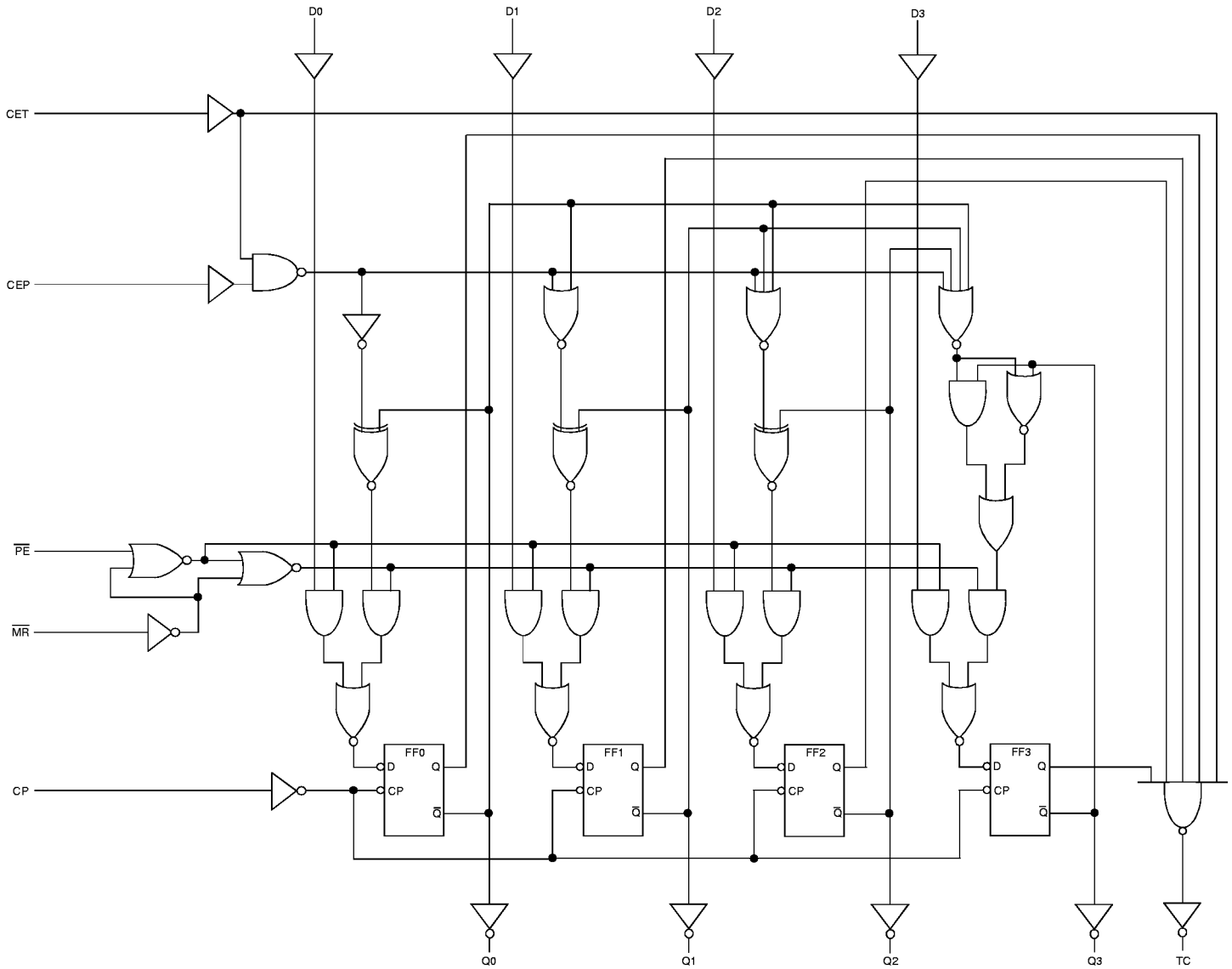
FUNCTIONAL DIAGRAM



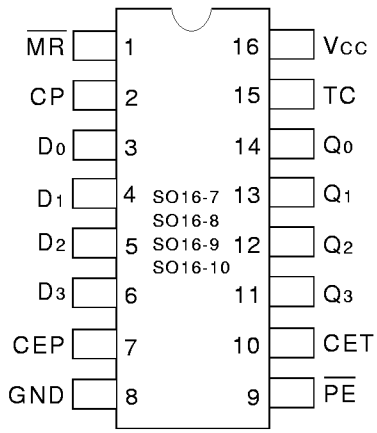
STATE DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

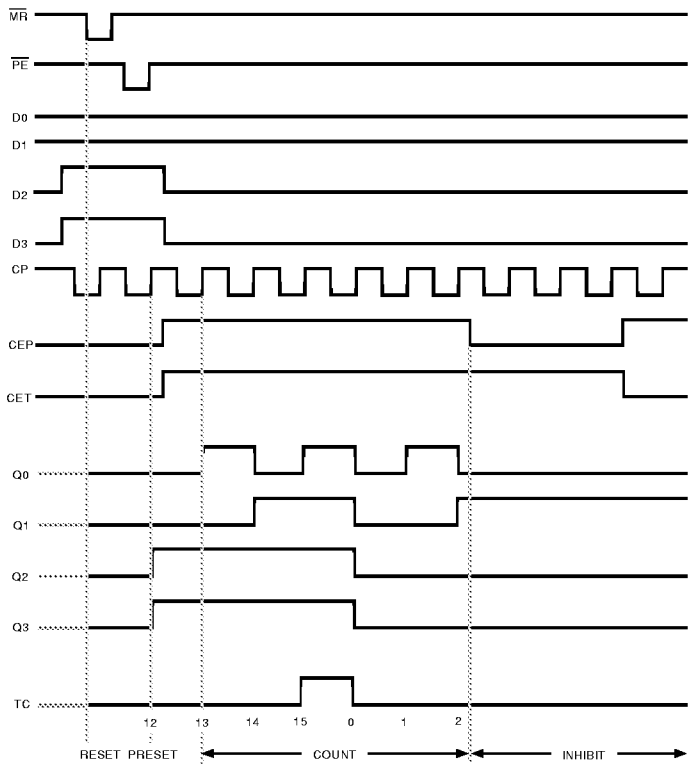


PIN CONFIGURATION



SOIC/ SSOP/ TSSOP/ QSOP
TOP VIEW

TYPICAL TIMING SEQUENCE



FUNCTION TABLE (1)

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dx	Qx	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
Count	h	↑	h	h	h	X	count	*
Hold (do nothing)	h	X	l	X	h	X	Q_0	*
	h	X	X	l	h	X	Q_0	L

NOTE:

1. H = HIGH Voltage Level
   h = HIGH Voltage level one setup time prior to the LOW-to-HIGH clock transition.
   L = LOW Voltage Level
   l = HIGH Voltage level one setup time prior to the LOW-to-HIGH clock transition.
   Q_0 = Indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.
   X = Don't Care
   * = The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH).
   ↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	– 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

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NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Symbol	Description
$\overline{MR}$	Synchronous Master Reset (Active LOW)
CP	Clock Input (LOW-to-HIGH, Edge-Triggered)
Dx	Data Inputs
CEP	Count Enable Inputs
GND	Ground (0V)
$\overline{PE}$	Parallel Enable Input (Active LOW)
CET	Count Enable Carry Input
Qx	Flip-Flop Outputs
TC	Terminal Count Output
Vcc	Positive Supply Voltage

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = – 40°c to +85°c

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level(2)	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V other inputs at V_{CC} or GND		—	—	500	µA

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Clock Pin (CP) requires a minimum V_{IH} of 2.5V.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V Typical	Vcc = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance	C_L = 0pF, f = 10Mhz	—	—	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Vcc = 1.2V Min.	Vcc = 1.2V Max.	Vcc = 2.7V Min.	Vcc = 2.7V Max.	Vcc = 3.3V ± 0.3V Min.	Vcc = 3.3V ± 0.3V Max.	Unit
t_{PHL} t_{PLH}	Propagation Delay CP to Qx	—	—	—	9	—	8	ns
t_{PHL} t_{PLH}	Propagation Delay CP to TC	—	—	—	11	—	9.5	ns
t_{PHL} t_{PLH}	Propagation Delay CET to TC	—	—	—	8.8	—	7.8	ns
t_W	Clock Pulse Width, HIGH or LOW	—	—	5	—	4	—	ns
t_{SU}	Set-up Time Dx to CP	—	—	3.5	—	3	—	ns
t_{SU}	Set-up Time $\overline{MR}$, $\overline{PE}$ to CP	—	—	3.5	—	3	—	ns
t_{SU}	Set-up Time CEP, CET to CP	—	—	5.5	—	5	—	ns
t_H	Hold Time Dx, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	—	—	0	—	0	—	ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = −40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 2.5V ±0.2V	$V_{CC}^{(2)}$= 3.3V ±0.3V & 2.7V	Unit
V_{LOAD}	2 x Vcc	6	V
V_{IH}	Vcc	2.7	V
V_T	Vcc / 2	1.5	V
V_{LZ}	150	300	mV
V_{HZ}	150	300	mV
C_L	30	50	pF

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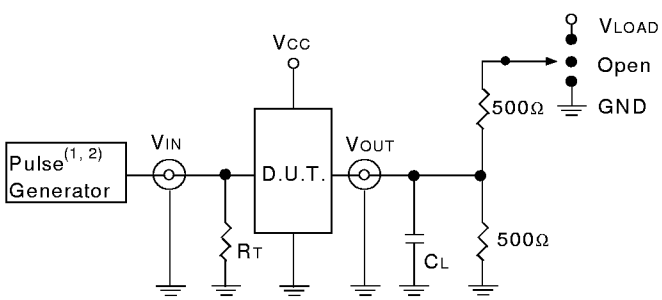
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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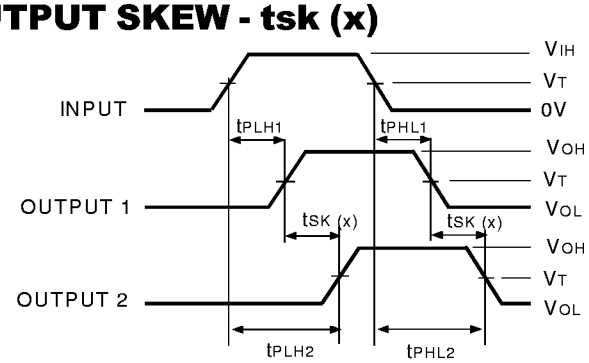
OUTPUT SKEW - tsk (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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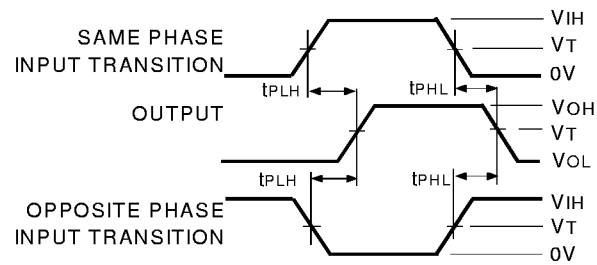
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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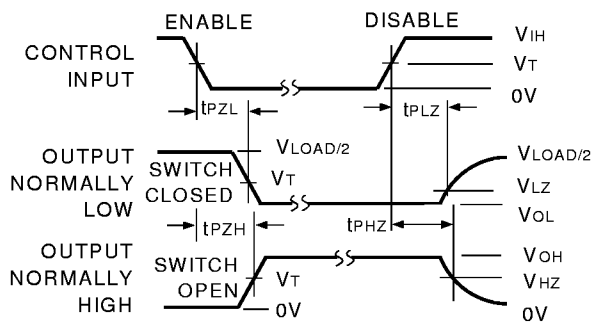
ENABLE AND DISABLE TIMES



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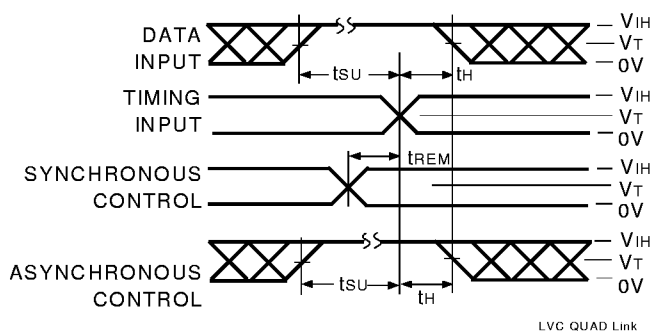
NOTE:

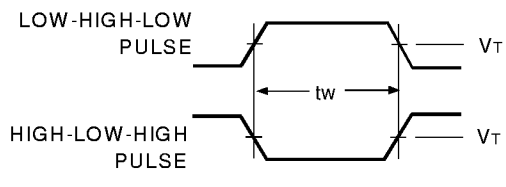
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



LVC QUAD Link

PULSE WIDTH



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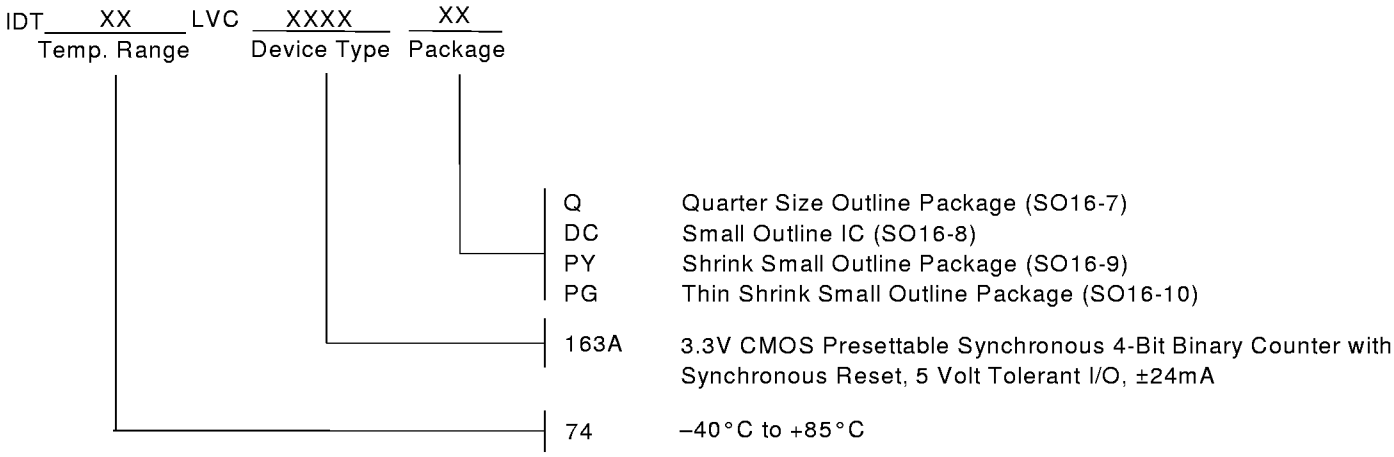
ORDERING INFORMATION



Q	Quarter Size Outline Package (SO16-7)
DC	Small Outline IC (SO16-8)
PY	Shrink Small Outline Package (SO16-9)
PG	Thin Shrink Small Outline Package (SO16-10)
163A	3.3V CMOS Presettable Synchronous 4-Bit Binary Counter with Synchronous Reset, 5 Volt Tolerant I/O, ±24mA
74	–40°C to +85°C

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