

HB56D25632 Series

4496203 0019099 T44 HIT2

262,144-Word x 32-Bit High Density Dynamic RAM Module

T-46-23-17

DESCRIPTION

The HB56D25632B is a 256k x 32 dynamic RAM module, mounted 8 pieces of 1 Mbit DRAM (HM514256JP) sealed in SOJ package. An outline of the HB56D25632B is 72-pin single in-line package. Therefore, the HB56D25632B makes high density mounting possible without surface mount technology. The HB56D25632B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

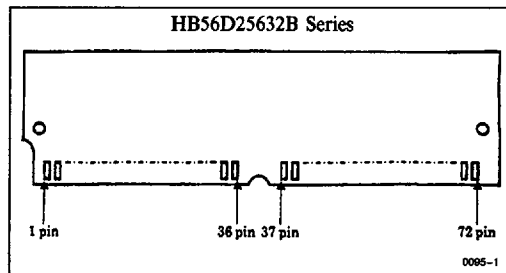
FEATURES

- 72-pin Single In-line Package
 - Lead Pitch 1.27mm
- Single 5V ($\pm 5\%$) Supply
- High Speed
 - Access Time 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
 - Active Mode 3.78W/3.36W/2.772W/2.31W/1.974W (max)
 - Standby Mode 84 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle/8 ms
- 2 Variations of Refresh
 - RAS Only Refresh
 - CAS Before RAS Refresh
- TTL Compatible

ORDERING INFORMATION

Part No.	Access Time	Package
HB56D25632B-6A	60 ns	72-pin SIP Socket Type
HB56D25632B-7A	70 ns	
HB56D25632B-8A	80 ns	
HB56D25632B-10A	100 ns	
HB56D25632B-12A	120 ns	

PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	CAS0	58	DQ28
5	DQ17	23	DQ21	41	CAS2	59	V _{CC}
6	DQ2	24	DQ6	42	CAS3	60	DQ29
7	DQ18	25	DQ22	43	CAS1	61	DQ13
8	DQ3	26	DQ7	44	RAS0	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	WE	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	V _{SS}
14	A2	32	NC	50	DQ24	68	NC
15	A3	33	NC	51	DQ9	69	T.B.D.
16	A4	34	RAS2	52	DQ25	70	T.B.D.
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₈	Address Input
A ₀ -A ₈	Refresh Address Input
DQ ₀ -DQ ₃₁	Data-in/Data-out
CAS ₀ -CAS ₃	Column Address Strobe
RAS ₀ -RAS ₂	Row Address Strobe
WE	Read/Write Enable
V _{CC}	Power (+ 5V)
V _{SS}	Ground
NC	No Connection

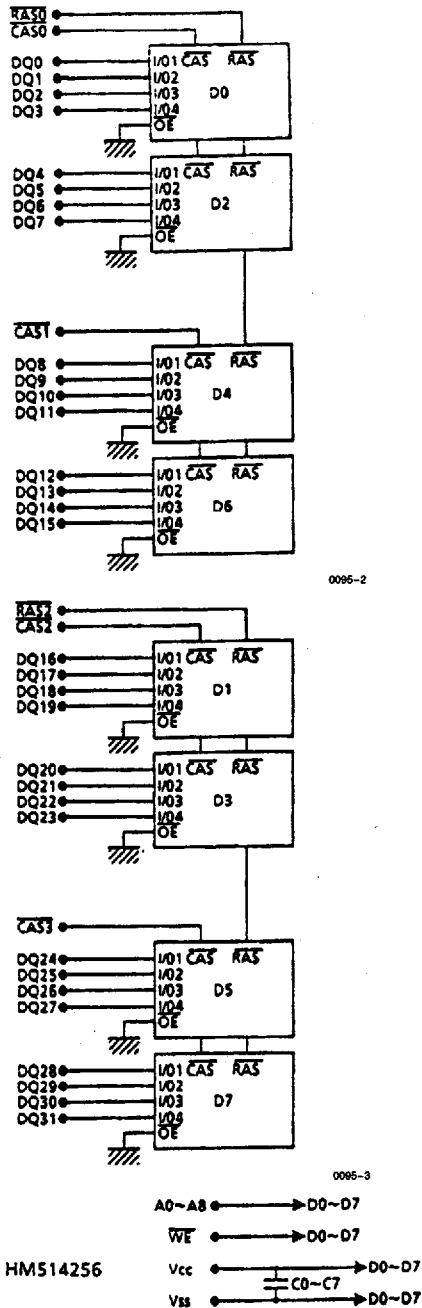
HITACHI/ LOGIC/ARRAYS/MEM 51E D



■ BLOCK DIAGRAM

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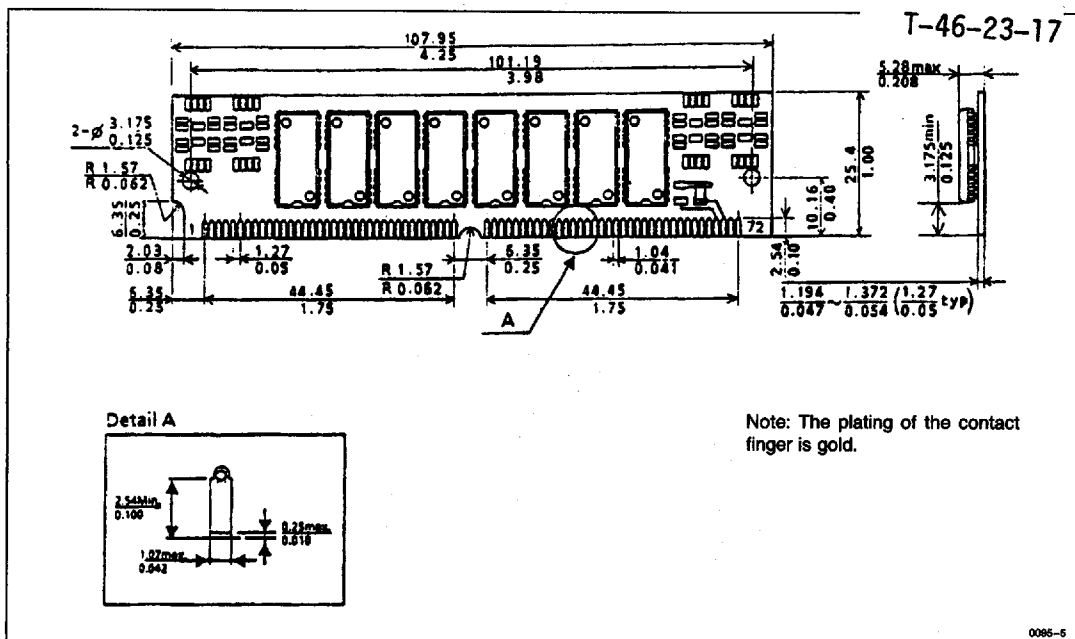


* D0~D7 : HM514256



■ PHYSICAL OUTLINE

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Unit: $\frac{\text{mm}}{\text{inch}}$ 

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input) V_{in}	-1.0 to +7.0	V
	(Output) V_{out}	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note 1. All voltage referenced to V_{SS} .

• DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$)

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Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	720	—	640	—	528	—	440	—	376	mA	$t_{RC} = \text{Min}$	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	mA	TTL Interface RAS, CAS = V_{IH} $D_{out} = \text{High-Z}$	
		—	8	—	8	—	8	—	8	—	8	mA	CMOS Interface RAS, CAS $\geq V_{CC} - 0.2\text{V}$ $D_{out} = \text{High-Z}$	
RAS Only Refresh Current	I_{CC3}	—	720	—	640	—	528	—	440	—	376	mA	$t_{RC} = \text{Min}$	2
Standby Current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	mA	RAS = V_{IH} CAS = V_{IL} $D_{out} = \text{Enable}$	1
CAS Before RAS Refresh Current	I_{CC6}	—	720	—	640	—	528	—	440	—	376	mA	$t_{RC} = \text{Min}$	
Page Mode Current	I_{CC7}	—	720	—	640	—	440	—	440	—	376	mA	$t_{PC} = \text{Min}$	1, 3
Input Leakage Current	I_{LI}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{in} \leq 7\text{V}$	
Output Leakage Current	I_{LO}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{out} \leq 7\text{V}$ $D_{out} = \text{Disable}$	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High $I_{out} = -5\text{mA}$	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low $I_{out} = 4.2\text{mA}$	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.2. Address can be changed less than three times while RAS = V_{IL} .3. Address can be changed once or less while CAS = V_{IH} .• Capacitance ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	68	pF	1
Input Capacitance ($\overline{\text{WE}}$)	C_{I2}	—	76	pF	1
Input Capacitance (RAS)	C_{I3}	—	43	pF	1
Input Capacitance (CAS)	C_{I4}	—	29	pF	1
Output Capacitance (DQ0-DQ31)	C_{LO}	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS = V_{IH} to disable D_{out} .• AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$)^{1, 12}

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	125	—	140	—	160	—	190	—	220	—	ns	
RAS Precharge Time	t_{RP}	55	—	60	—	70	—	80	—	90	—	ns	
RAS Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
CAS Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	

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Read, Write and Refresh Cycle (Common Parameters) (continued)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
RAS to CAS Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
RAS to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
RAS Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
CAS Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ns	15

Read Cycle

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Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from RAS	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from CAS	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to CAS	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to RAS	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

Write Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
RAS Precharge to CAS Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	



Fast Page Mode Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode CAS Precharge Time	t_{CP}	10	—	10	—	10	—	15	—	20	—	ns	
Fast Page Mode RAS Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from CAS Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
RAS Hold Time from CAS Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$, $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$, $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. Early write cycle only ($t_{WCS} \geq t_{WCS}(\text{min})$).
 11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle.
 12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ only refresh).
 13. t_{RASC} is determined by $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 15. t_{REF} is determined by 512 refresh cycles.

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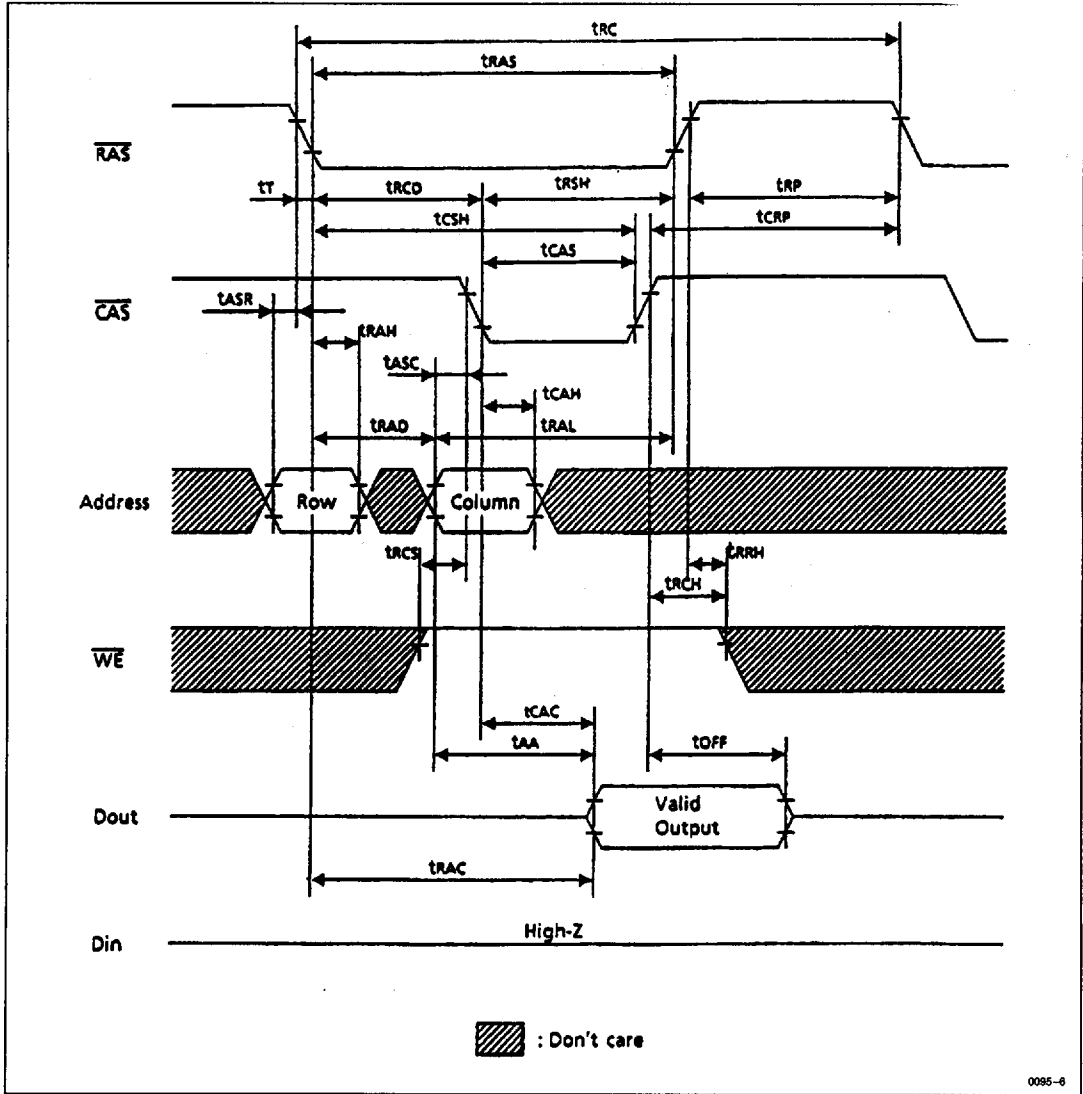


■ TIMING WAVEFORM

• Read Cycle

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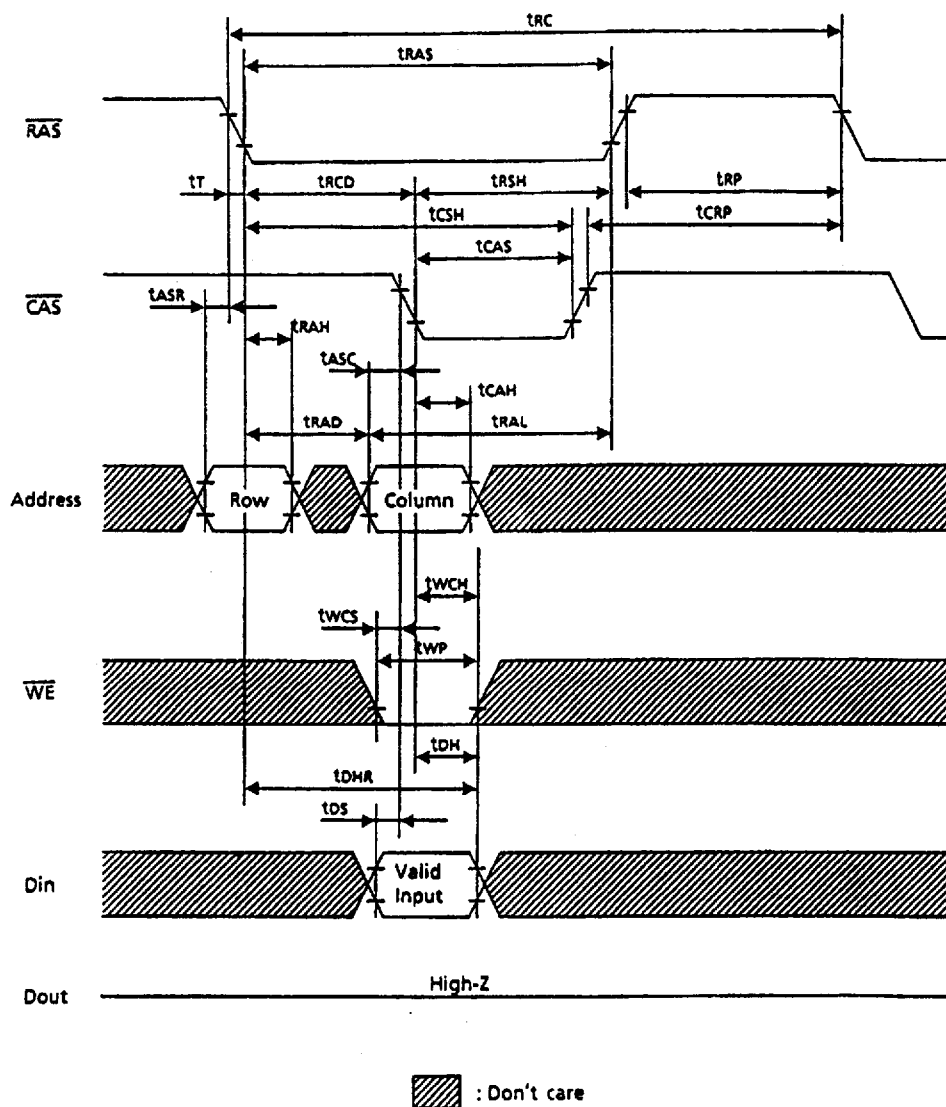


0095-6



■ Early Write Cycle

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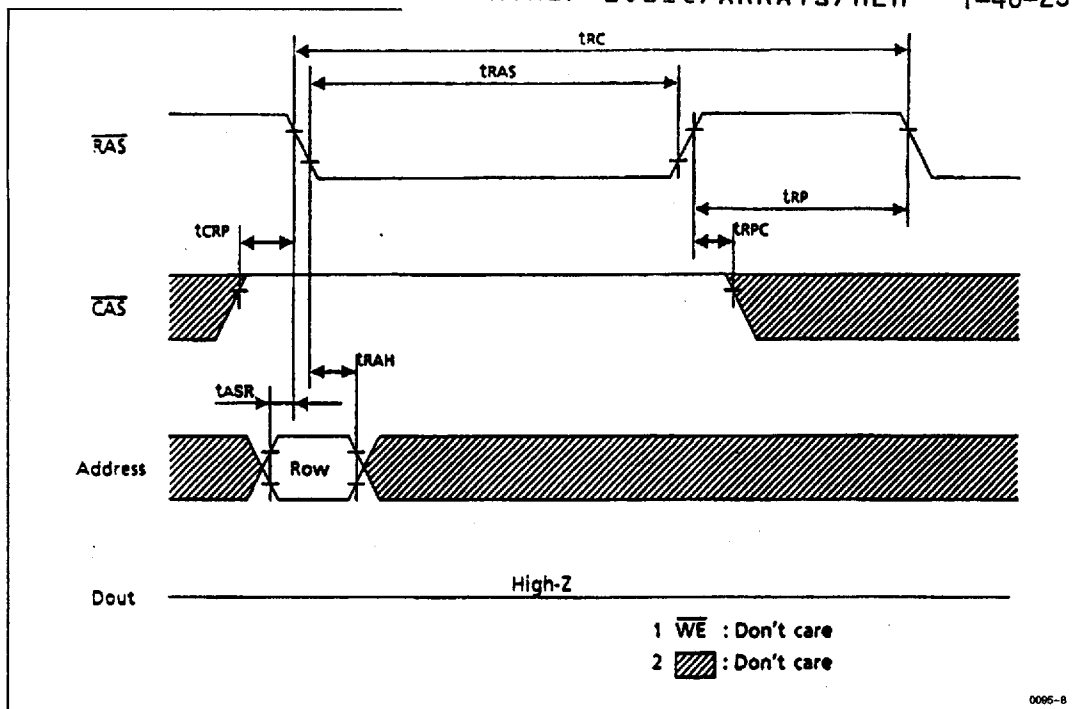


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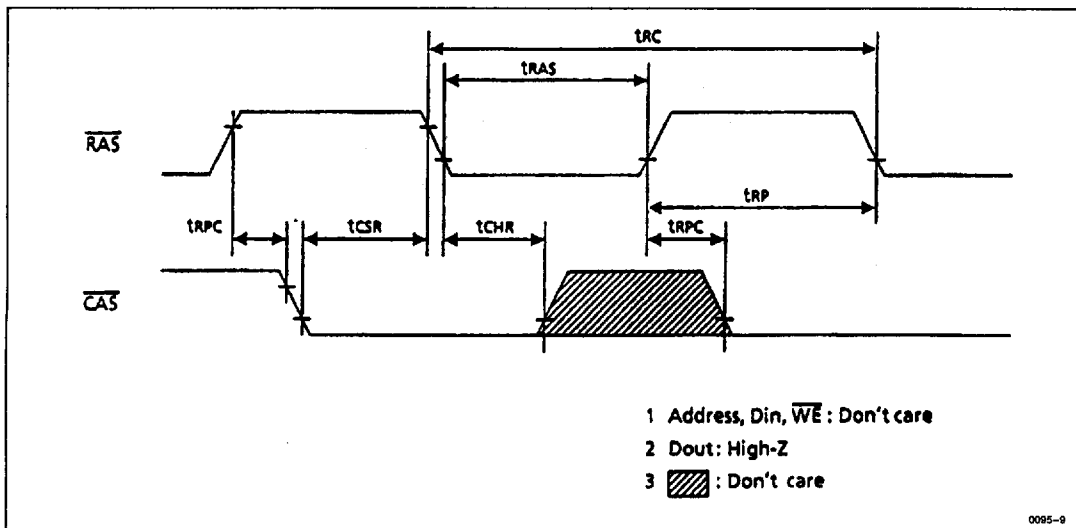


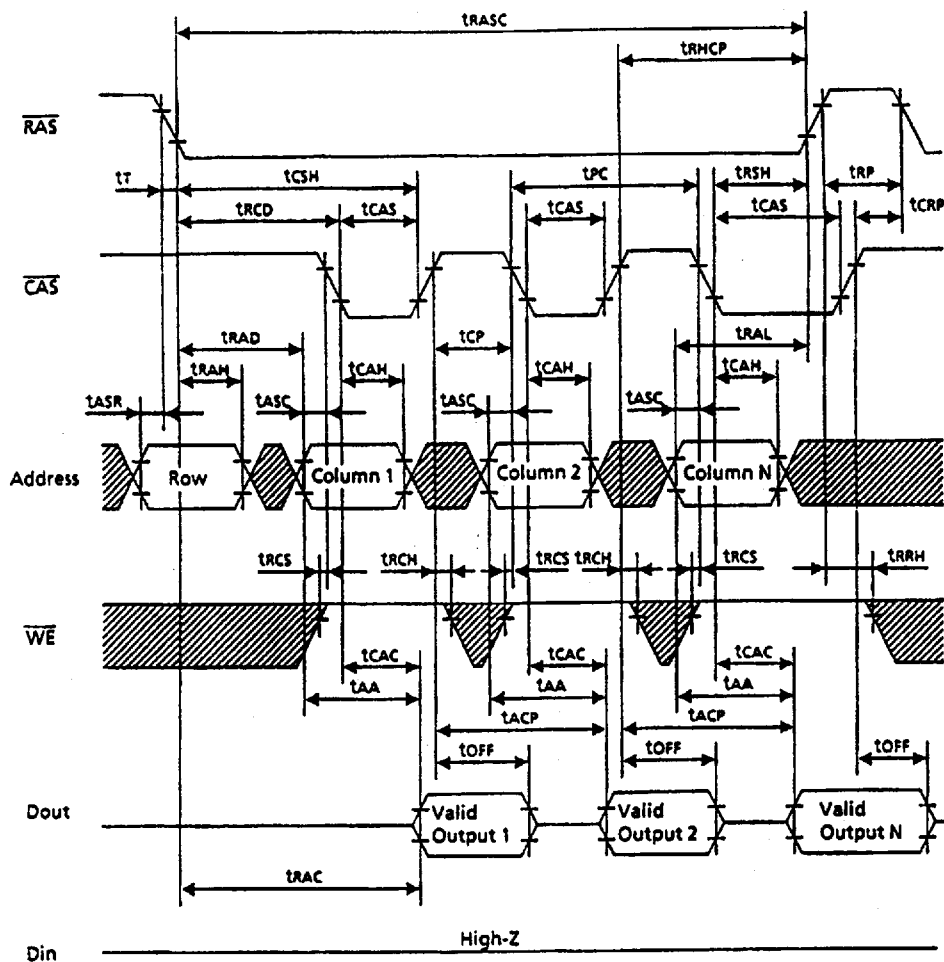
• RAS Only Refresh Cycle

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• CAS Before RAS Refresh Cycle





 : Don't care

0095-10

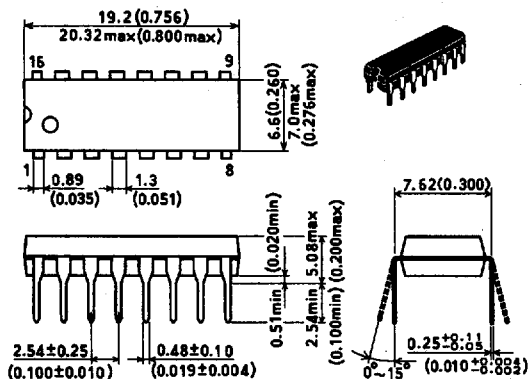


T-90-20

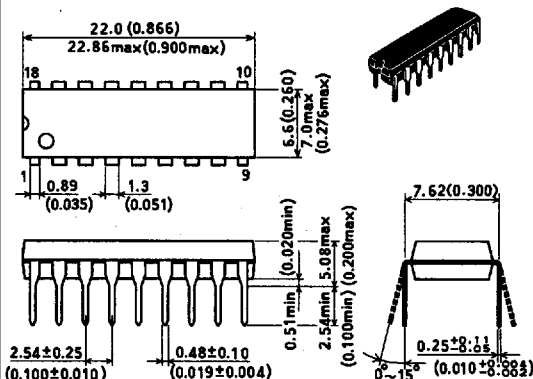
Unit: mm (inch) Scale 3/2

• Dual-in-line Plastic

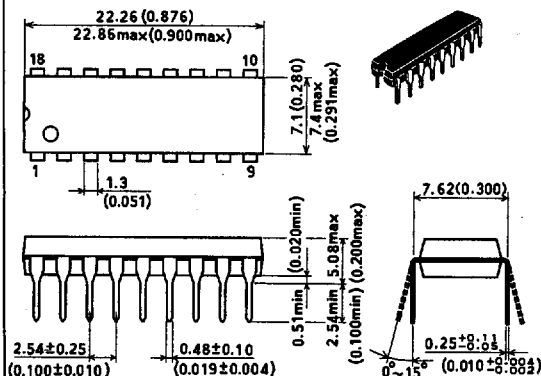
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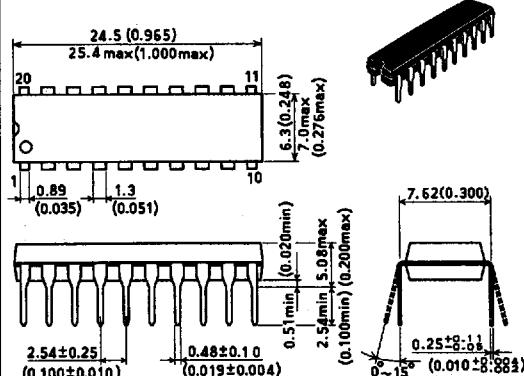
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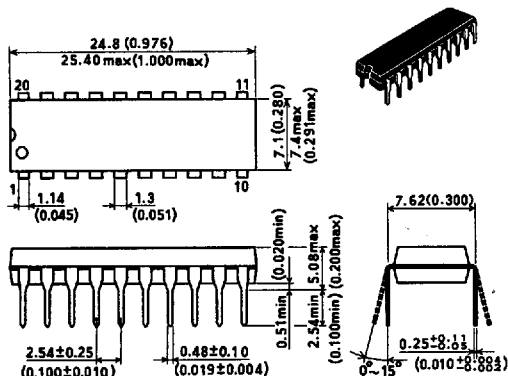
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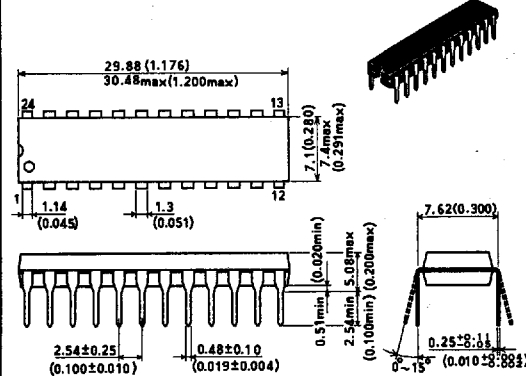
• DP-20N



• DP-20NA



• DP-20NC

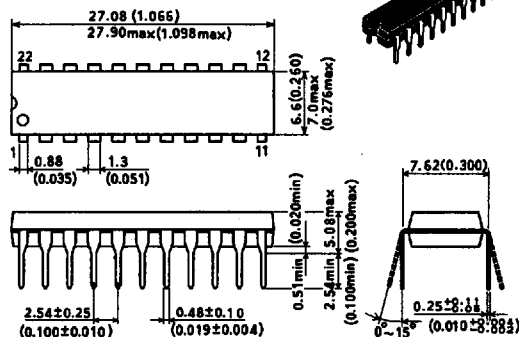


• Dual-In-line Plastic

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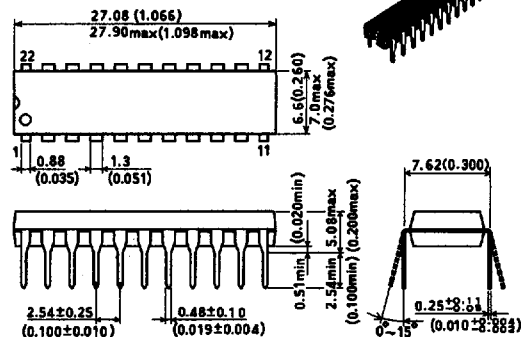
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• DP-22N

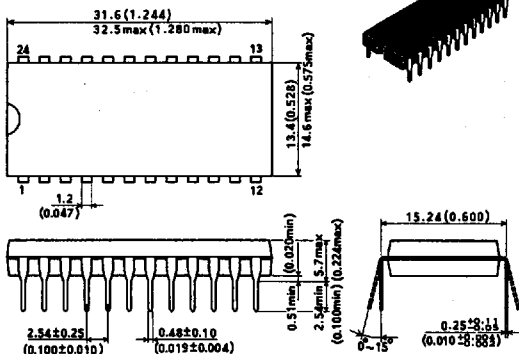


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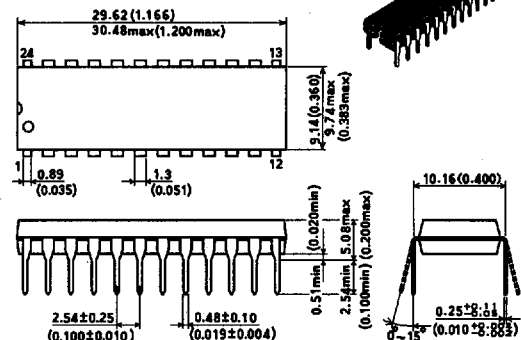
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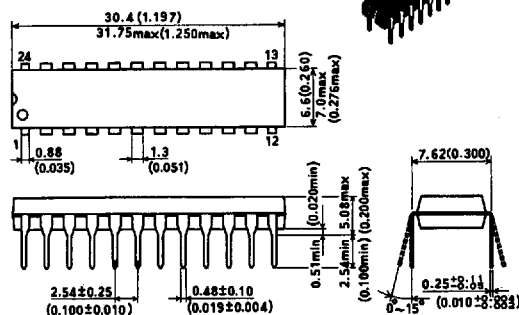
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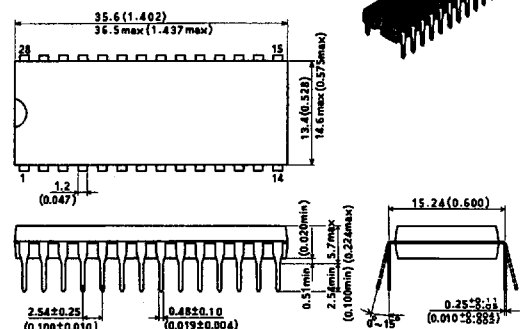
• DP-24A



• DP-24N



• DP-28

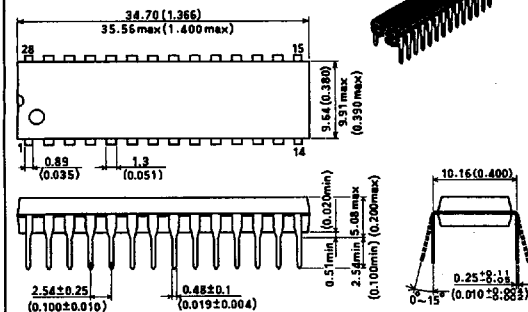


• Dual-in-line Plastic

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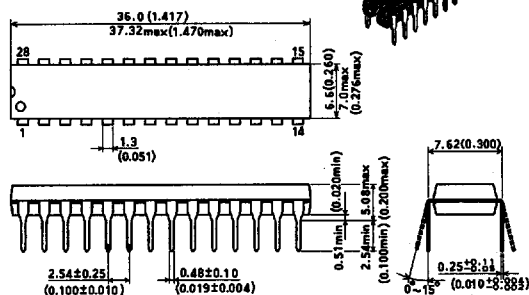
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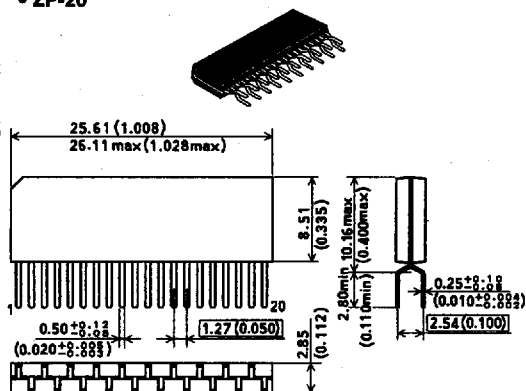


• DP-28N

T-90-20

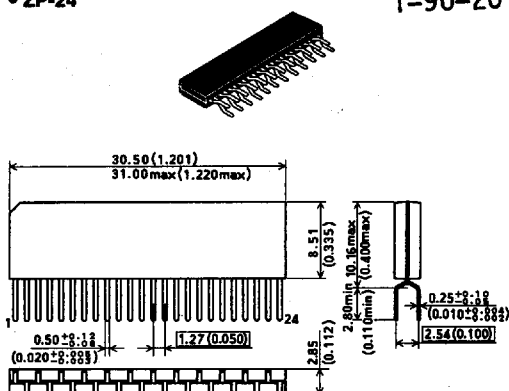


• ZP-20

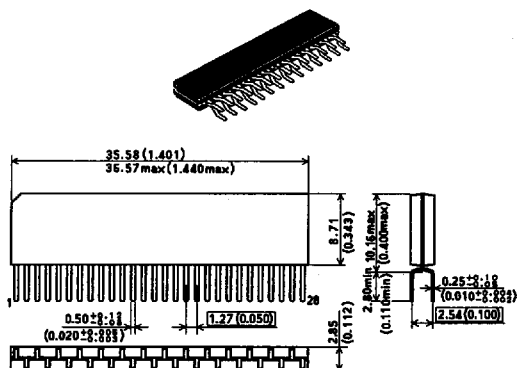


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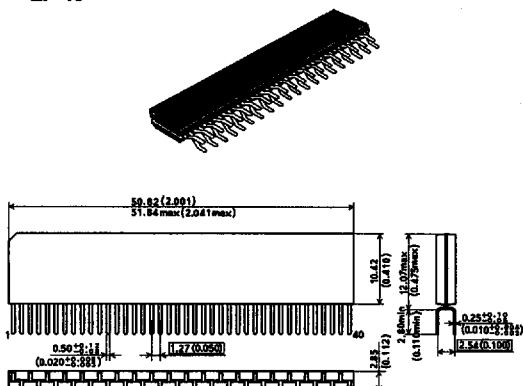
T-90-20



• ZP-28



• ZP-40



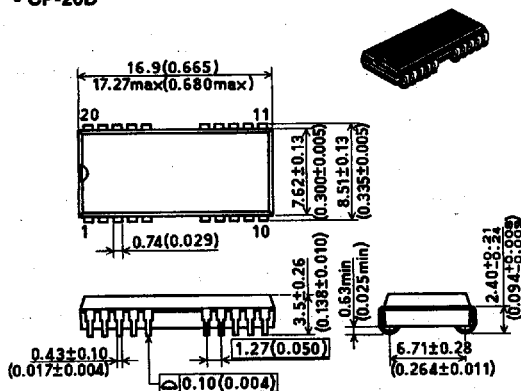
• Flat Package (J-bend Leads)

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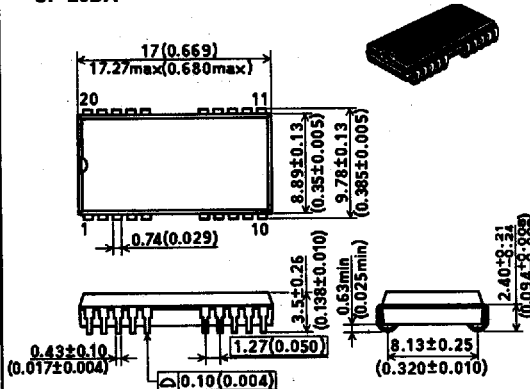
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T-90-20

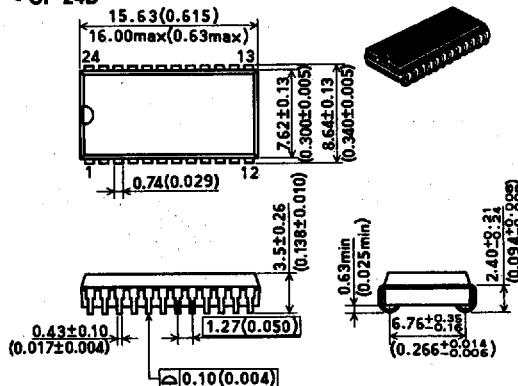
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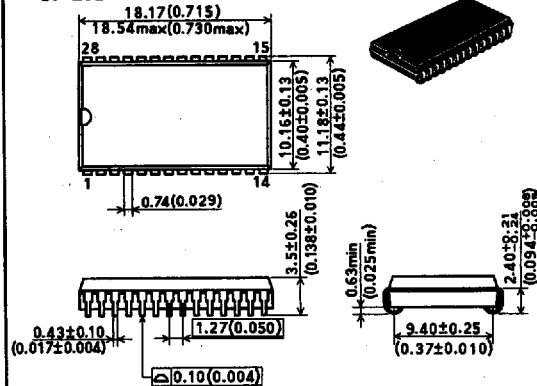
• CP-20DA



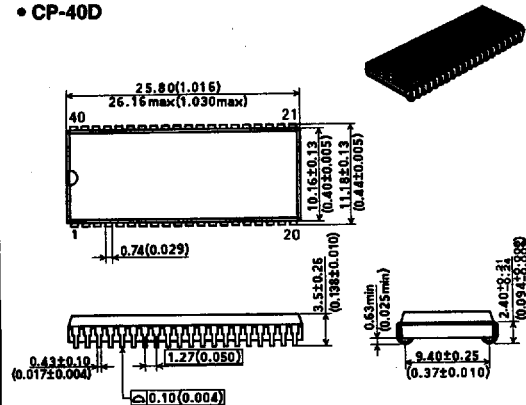
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• CP-28D



• CP-40D

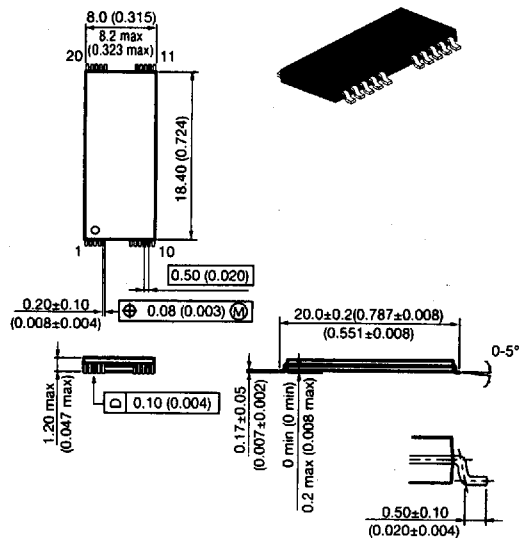


• TSOP (Thin Small Outline Package)

HITACHI/ LOGIC/ARRAYS/MEM

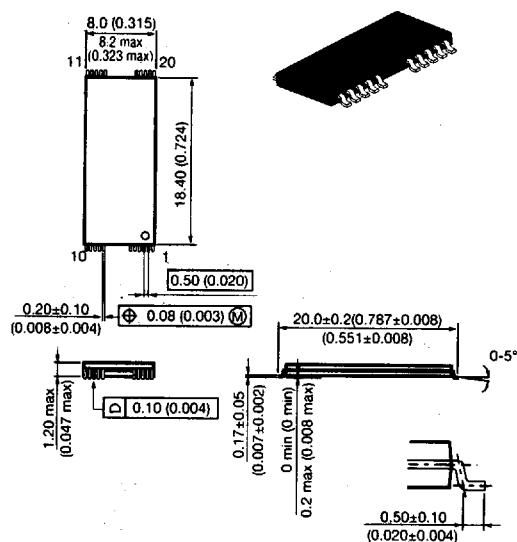
Unit: mm (inch) Scale 3/2

• TFP-20DA

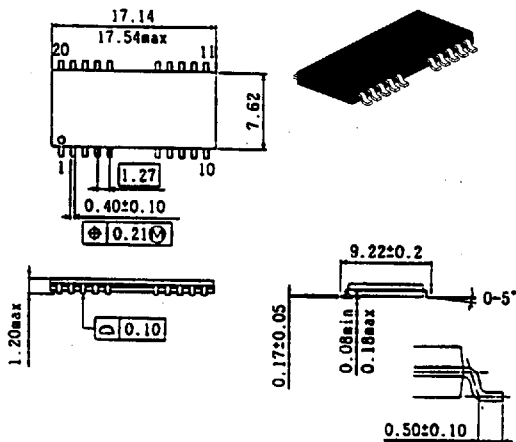


• TFP-20DAR

T-90-20



• TTP-20D



• TTP-20DR

