



LG Semicon Co.,Ltd.

REVISION HISTORY

/ Revision 1.0: July 1998

- Add PC100,7K(2-2-2) Specifications.
 - Update Icc Specifications.
 - Change Input Test Condition from 2.8/0.0V to 2.4/0.4V.
 - Added post SPD Information separately(7K/7J/10K) for Modules.
 - Add Minimum Capacitance Value for Component.
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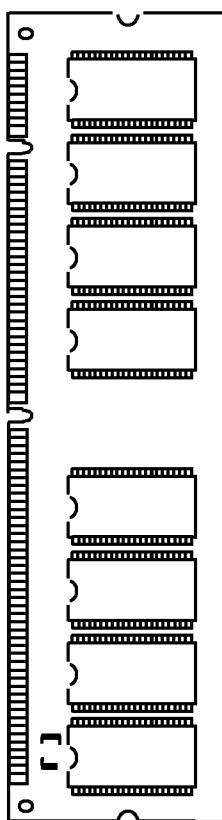


Description

The GMM26416233CNTG is a 16M x 64bits Synchronous Dynamic RAM MODULE which is assembled 16 pieces of 8M x 8bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM26416233CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM26416233CNTG provides common data inputs and outputs.

GMM26416233CNTG (Double Side)



Features

- * PC100,PC66 Compatible
7K(2-2-2),7J(3-2-2),10K(PC66)
- * 3.3V +/- 0.3V Power supply
- * Maximum Clock frequency
100 / 125 MHz
- * LVTTTL Interface
- * Burst read/write operation and burst read/
single write operation capability
- * Programmable burst length ;
1, 2, 4, 8, Full page
- * Programmable burst sequence
Sequential / Interleave
- * Full Page burst length capability
Sequential burst
Burst stop capability
- * Programmable $\overline{\text{CAS}}$ Latency ; 2, 3
- * CKE power down mode
- * Input / Output data masking
- * 4096 Refresh Cycles / 64ms
- * Auto refresh / Self refresh Capability
- * Serial Presence Detect with EEPROM

Pin Name

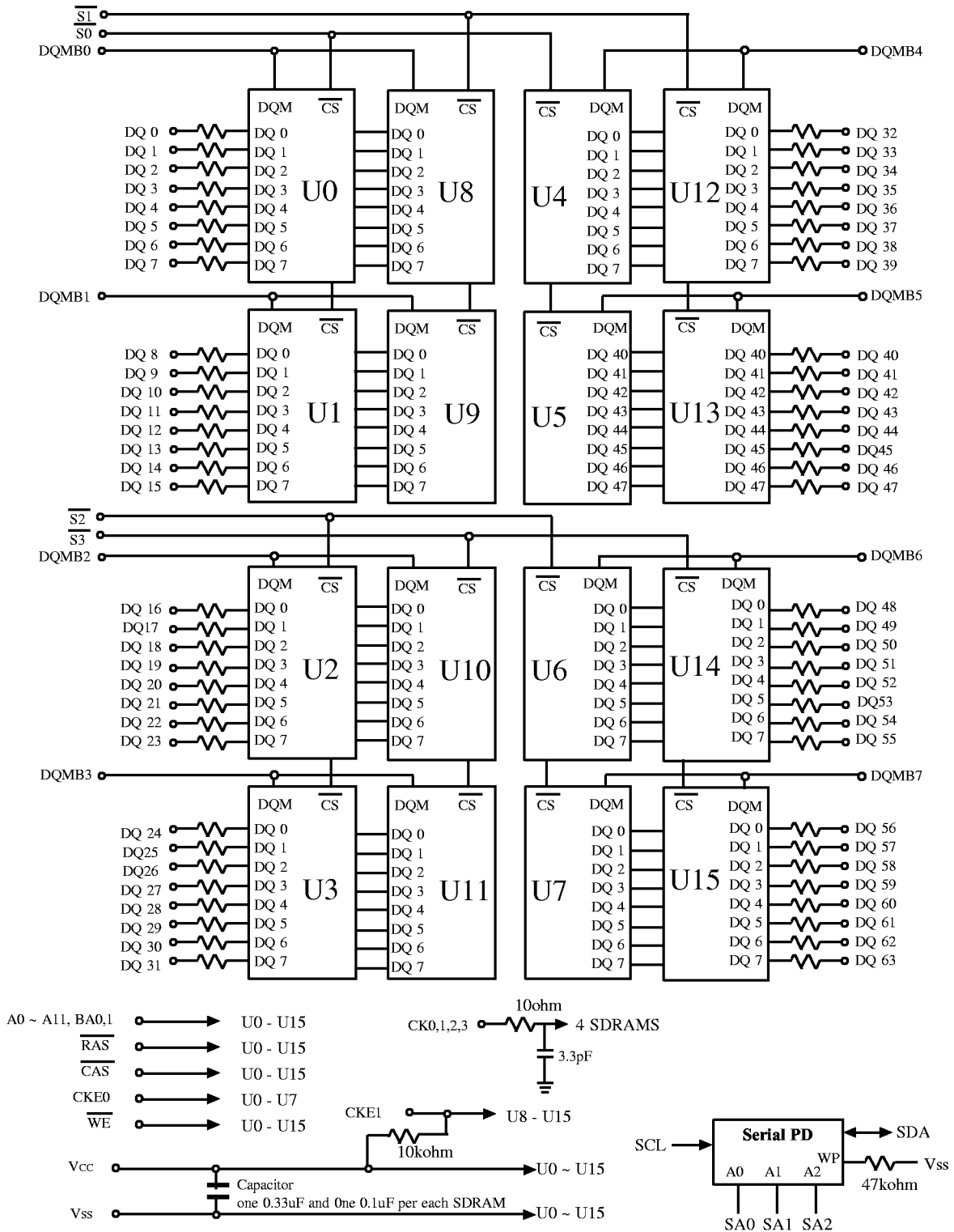
CK0, 1, 2, 3	Clock input
$\overline{\text{CKE0,1}}$	Clock Enable
$\overline{\text{S0,1,2,3}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
VCC	Power for internal circuit
VSS	Ground for internal circuit
NC	No Connect
VREF	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

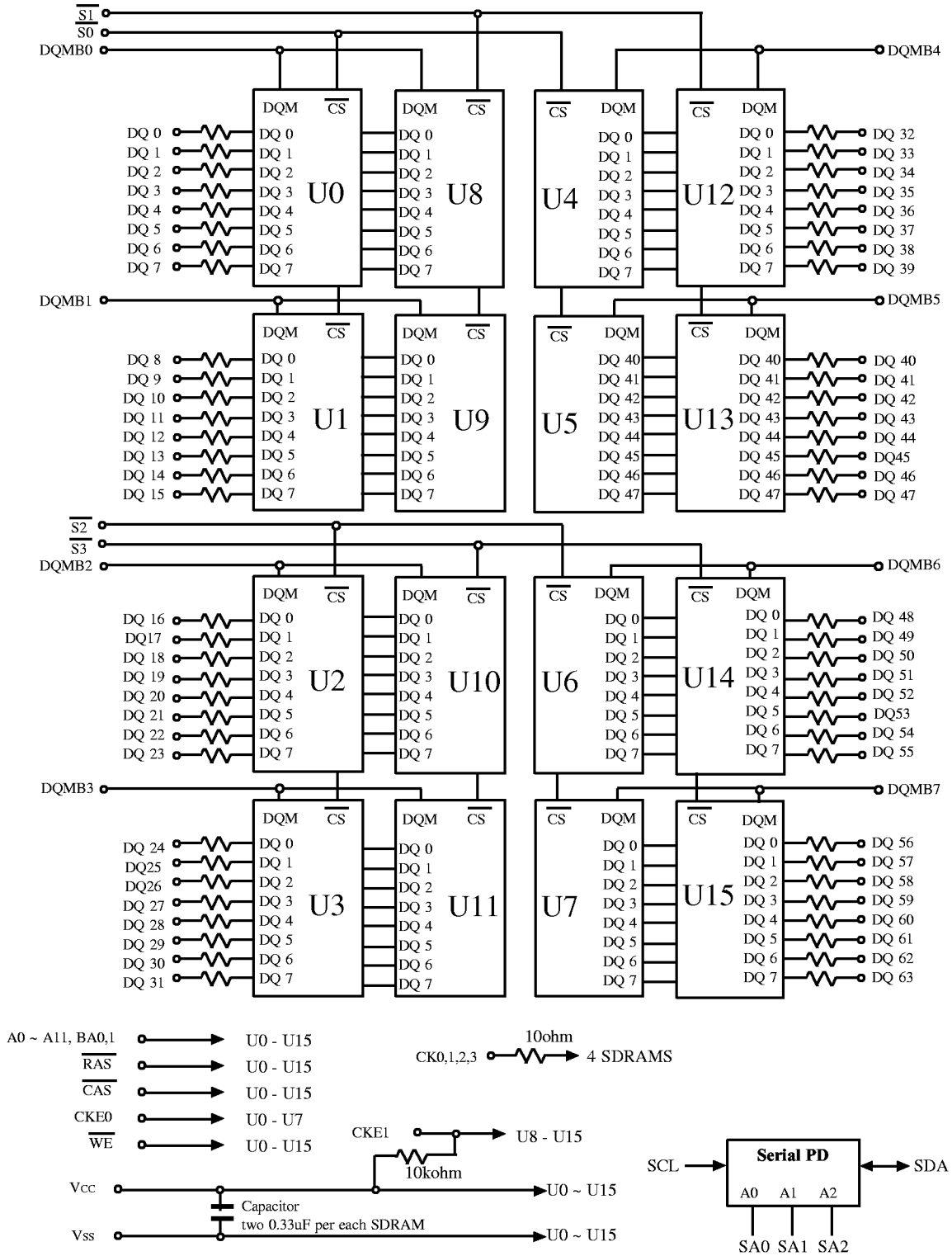
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP/NC	109	NC	137	*CB7	165	SA0
26	$\overline{Vcc}$	54	Vss	82	SDA	110	$\overline{Vcc}$	138	Vss	166	SA1
27	WE	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram (-7K,7J)



Block Diagram (-10K)



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0,1 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0,1,2,3}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. * Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. * Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
Vcc (power supply pins)	3.3 V is applied. (Vcc is for the internal circuit)
Vss (power supply pins)	Ground is connected. (Vss is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION(-7K)

- * Serial PD Interface Protocol : I²C
- * Current sink capability of SDA driver <= 3mA
- * Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t _{CK3} =10ns	A0h	
10	SDRAM access time from clock	t _{AC3} =6.0ns	60h	
11	DIMM configuration type	Non-Parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	N/A	00h	
15	Minimum clock delay, Back to Back Random Column Address	t _{CCD} =1	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	4 banks	04h	
18	CAS # Latency	2 & 3	06h	
19	CS # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t _{CK2} =10ns	A0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	$t_{AC2}=6.0ns$	60h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	$t_{RP}=20ns$	14h	
28	Minimum Row Active to Row Active Delay	$t_{RRD}=20ns$	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	$t_{RCD}=20ns$	14h	
30	Minimum $\overline{RAS}$ Pulse Width	$t_{RAS}=50ns$	32h	
31	Module Bank Density	64 MBytes	10h	
32	Command & address signal input setup time	$t_{AS} = 2ns$	20h	
33	Command & address signal input hold time	$t_{AH} = 1ns$	10h	
34	Data signal input setup time	$t_{DS} = 2ns$	20h	
35	Data signal input hold time	$t_{DH} = 1ns$	10h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1.2	12h	
63	Checksum for bytes 0 ~ 62		07h	
64	Manufacturer JEDEC ID code per JEP-106E	LGS	E0h	
65~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM26416233CNTG-7K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			31h	1
80			36h	6
81			32h	2
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			33h	3
84			43h	C
85			4Dh	N
86			54h	T
87			47h	G
88			2Dh	-
89			37h	7
90			4Bh	K
91~92	Revision Code	Rev. 0	00h	Rev.0
93	Date Code	WW	10h	16 week
94		YY	62h	98 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		FFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

SERIAL PRESENCE DETECT INFORMATION(-7J)* Serial PD Interface Protocol : I²C

* Current sink capability of SDA driver <= 3mA

* Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t _{CK3} =10ns	A0h	
10	SDRAM access time from clock	t _{AC3} =6.0ns	60h	
11	DIMM configuration type	Non-Parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	N/A	00h	
15	Minimum clock delay, Back to Back Random Column Address	t _{CCD} =1	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	4 banks	04h	
18	CAS # Latency	2 & 3	06h	
19	CS # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t _{CK2} =15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	$t_{AC2}=8.0ns$	80h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	$t_{RP}=20ns$	14h	
28	Minimum Row Active to Row Active Delay	$t_{RRD}=20ns$	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	$t_{RCD}=20ns$	14h	
30	Minimum $\overline{RAS}$ Pulse Width	$t_{RAS}=50ns$	32h	
31	Module Bank Density	64 MBytes	10h	
32	Command & address signal input setup time	$t_{AS} = 2ns$	20h	
33	Command & address signal input hold time	$t_{AH} = 1ns$	10h	
34	Data signal input setup time	$t_{DS} = 2ns$	20h	
35	Data signal input hold time	$t_{DH} = 1ns$	10h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1.2	12h	
63	Checksum for bytes 0 ~ 62		77h	
64	Manufacturer JEDEC ID code per JEP-106E	LGS	E0h	
65~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM26416233CNTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			31h	1
80			36h	6
81			32h	2
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			33h	3
84			43h	C
85			4Dh	N
86			54h	T
87			47h	G
88			2Dh	-
89			37h	7
90			4Ah	J
91~92	Revision Code	Rev 1.0	10h	Rev.1.0
93	Date Code	WW	10h	16 week
94		YY	62h	98 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		FDh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

SERIAL PRESENCE DETECT INFORMATION(-10K)* Serial PD Interface Protocol : I²C

* Current sink capability of SDA driver <= 3mA

* Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t _{CK3} =10ns	A0h	
10	SDRAM access time from clock	t _{AC3} =8.0ns	80h	
11	DIMM configuration type	Non-Parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	N/A	00h	
15	Minimum clock delay, Back to Back Random Column Address	t _{CCD} =1	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	4 banks	04h	
18	CAS # Latency	2 & 3	06h	
19	CS # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t _{CK2} =15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	$t_{AC2}=9.0ns$	90h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	$t_{RP}=30ns$	1Eh	
28	Minimum Row Active to Row Active Delay	$t_{RRD}=20ns$	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	$t_{RCD}=30ns$	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	$t_{RAS}=60ns$	3Ch	
31	Module Bank Density	64 MBytes	10h	
32	Command & address signal input setup time	$t_{AS} = 2ns$	20h	
33	Command & address signal input hold time	$t_{AH} = 1ns$	10h	
34	Data signal input setup time	$t_{DS} = 2ns$	20h	
35	Data signal input hold time	$t_{DH} = 1ns$	10h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1.2	12h	
63	Checksum for bytes 0 ~ 62		C5h	
64	Manufacturer JEDEC ID code per JEP-106E	LGS	E0h	
65~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM26416233CNTG-10K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			31h	1
80			36h	6
81			32h	2
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			33h	3
84			43h	C
85			4Dh	N
86			54h	T
87			47h	G
88			2Dh	-
89			41h	10
90			4Bh	K
91~92	Revision Code	Rev 1.0	10h	Rev.1.0
93	Date Code	WW	0Ah	10 week
94		YY	62h	98 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	66MHz	66h	
127	Intel specification details for 100Mhz support		FFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V _T	-0.5 to V _{CC} +0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to Vss	V _{CC}	-0.5 to +4.6	V	1
Short circuit output current	I _{OUT}	50	mA	
Power dissipation	P _T	1.0	W	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +125	°C	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (T_a = 0 to + 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V _{CC} , V _{CCQ}	3.0	3.6	V	1
	V _{SS} , V _{SSQ}	0	0	V	
Input high voltage	V _{IH}	2.0	V _{CC} + 0.3	V	1, 2
Input low voltage	V _{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 4.6V for pulse width ≤ 5ns

3. V_{IL} (min) = -1.5V for pulse width ≤ 5ns

DC Characteristics (Ta = 0 to 70°C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter	Symbol	- 7K	- 7J	- 8	- 10K	Unit	Test conditions	Notes
		Max	Max	Max	Max			
Operating current	I _{CC1}	680	680	680	650	mA	Burst length= 1 t _{RC} = min	1, 2, 3
Standby current in power down	I _{CC2P}	24	24	24	24	mA	CKE = V _{IL} , t _{CK} = 12 ns	5
Standby current in power down (input signal stable)	I _{CC2PS}	16	16	16	16	mA	CKE=V _{IL} , t _{CK} = Infinity	6
Standby current in non power down (CAS latency=2)	I _{CC2N}	160	160	160	160	mA	CKE,CS = V _{IL} , t _{CK} = 12ns	4
Standby current in non power down (input signal stable)	I _{CC2NS}	64	64	64	64	mA	CKE = V _{IL} , t _{CK} = infinity	8
Active standby current in power down	I _{CC3P}	80	80	80	80	mA	CKE = V _{IL} , t _{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)	I _{CC3PS}	64	64	64	64	mA	CKE = V _{IL} , t _{CK} = infinity	2,6
Active standby current in non power down	I _{CC3N}	400	400	400	400	mA	CKE,CS = V _{IH} , t _{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)	I _{CC3NS}	200	200	200	200	mA	CKE = V _{IH} , t _{CK} = infinity	2,8
Burst operating current	(CL=2)	I _{CC4}	1000	720	920	mA	t _{CK} = min BL = 4	1,2,3
	(CL=3)		1000	1000	1200			
Refresh current	I _{CC5}	900	900	900	840	mA	t _{RC} = min	3
Self refresh current	I _{CC6}	16	16	16	16	mA	V _{IH} >= V _{CC} - 0.2 V _{IL} >= 0.2V	7

DC Characteristics ($T_a = 0$ to 70°C , V_{CC} , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$, V_{SS} , $V_{SSQ} = 0\text{ V}$)

Parameter	Symbol	- 7K, - 7J, - 8, - 10K		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	I_{LI}	-1	1	μA	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	I_{LO}	-1.5	1.5	μA	$0 \leq V_{out} \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	V	$I_{OH} = -2\text{ mA}$	
Output low voltage	V_{OL}	-	0.4	V	$I_{OL} = 2\text{ mA}$	

Notes : 1. I_{CC} depends on output load condition when the device is selected. $I_{CC}(\text{max})$ is specified at the output open condition.

2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance ($T_a = 25^\circ\text{C}$, V_{CC} , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance ($A0 \sim A11$, $BA0,1$)	-	100	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CKE}$)	-	100	pF	1, 3
C_{I3}	Input capacitance ($CK0$, $CK1$, $CK2$, $CK3$)	-	47	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0} \sim \overline{S3}$)	-	37	pF	1, 3
C_{I5}	Input capacitance ($DQMB0 \sim DQMB7$)	-	20	pF	1, 3
$C_{I/O}$	I/O capacitance ($DQ0 \sim 63$)	-	20	pF	1, 2, 3

- Note :
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. DQMB = V_{IH} to disable Dout.
 3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, Vcc, Vccq = 3.3 V +/- 0.3 V, Vss, Vssq = 0 V)

Parameter		Symbol	- 7K		- 7J		- 8		- 10K		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t _{CK}	10	-	15	-	12	-	15	-	ns	1
	(CL=3)	t _{CK}	10	-	10	-	8	-	10	-		
CLK high pulse width		t _{CKH}	3	-	3	-	3	-	3	-	ns	1
CLK low pulse width		t _{CKL}	3	-	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t _{AC}	-	6	-	8	-	8	-	9	ns	1, 2
	(CL=3)	t _{AC}	-	6	-	6	-	6	-	8		
Data-out hold time		t _{OH}	3	-	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedance		t _{LZ}	2	-	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2,3)		t _{HZ}	-	6	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t _{DS}	2	-	2	-	2	-	2	-	ns	1
Data-in hold time		t _{DH}	1	-	1	-	1	-	1	-	ns	1
Address setup time		t _{AS}	2	-	2	-	2	-	2	-	ns	1
Address hold time		t _{AH}	1	-	1	-	1	-	1	-	ns	1
CKE setup time		t _{CES}	2	-	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t _{CESP}	2	-	2	-	2	-	2	-	ns	1
CKE hold time		t _{CEH}	1	-	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t _{CS}	2	-	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t _{CH}	1	-	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t _{RC}	70	-	70	-	72	-	90	-	ns	1
Active to Precharge command period		t _{RAS}	50	120000	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t _{RCD}	20	-	20	-	24	-	30	-	ns	1
Precharge to active command period		t _{RP}	20	-	20	-	24	-	30	-	ns	1

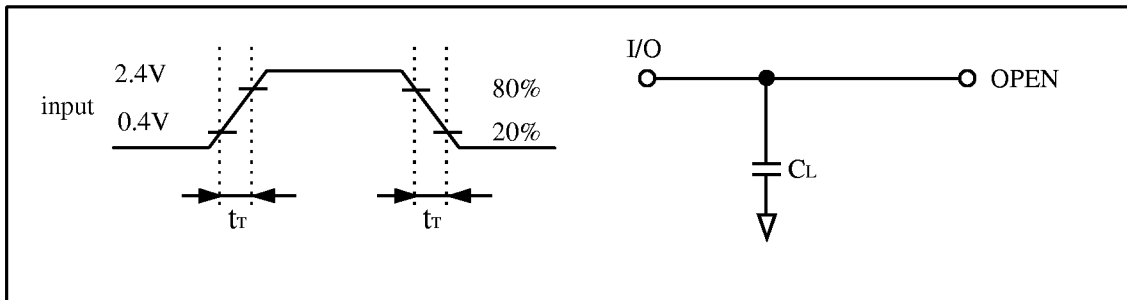
AC Characteristics ($T_a = 0$ to 70°C , $V_{CC}, V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS}, V_{SSQ} = 0\text{ V}$)
(Continued)

Parameter	Symbol	- 7K		- 7J		- 8		- 10K		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	-	64	ms	

- Notes : 1. AC measurement assumes $t_T = 1\text{ ns}$. Reference level for timing of input signals is 1.40V.
 2. Access time is measured at 1.40V. Load condition is $C_L = 50\text{ pF}$ without termination.
 3. $t_{LZ}(\text{min})$ defines the time at which the outputs achieves the low impedance state.
 4. $t_{HZ}(\text{max})$ defines the time at which the outputs achieves the high impedance state.
 5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- * Input and output-timing reference levels: 1.4V
- * Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

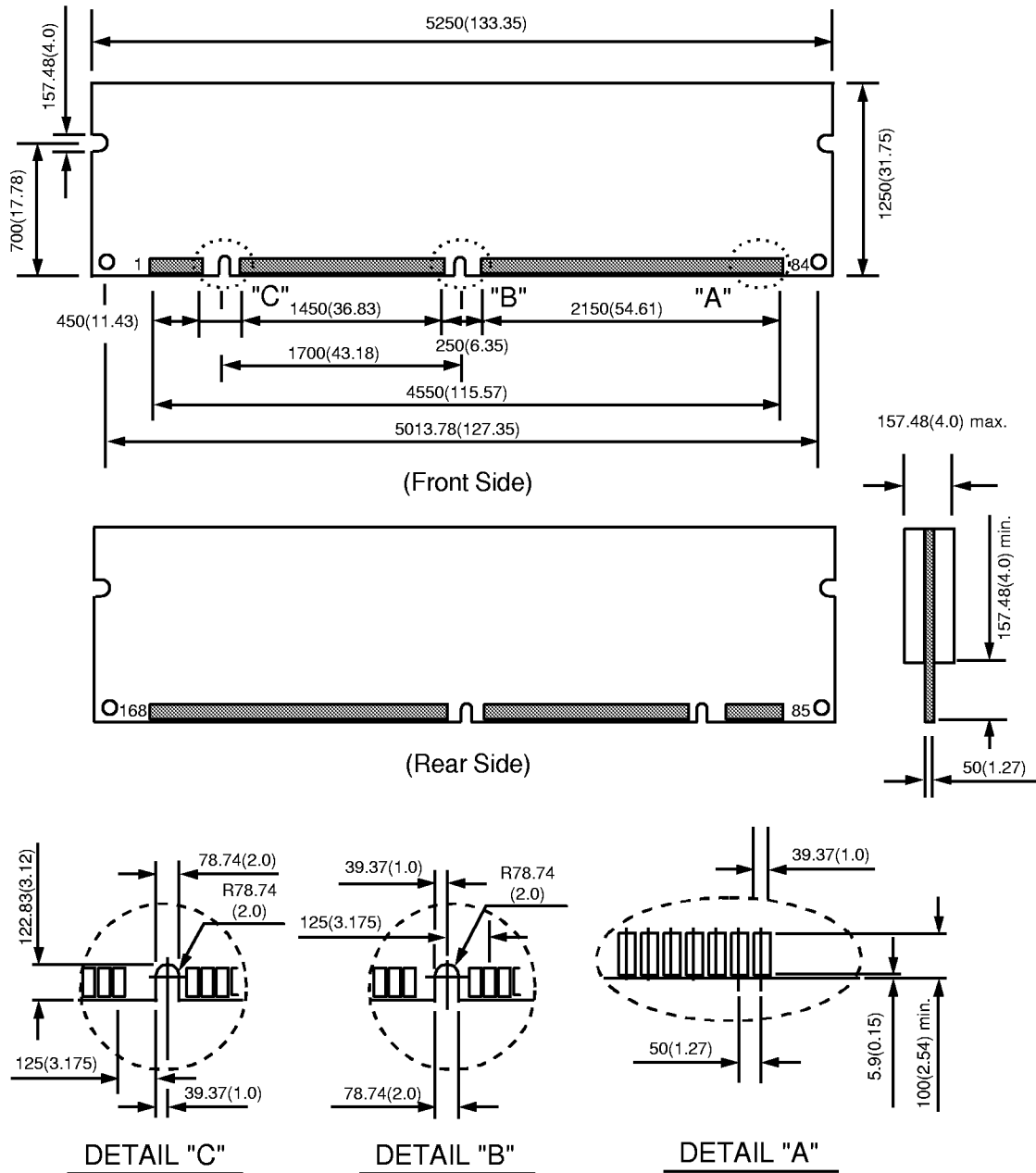
Parameter		Symbol	- 7K	- 7J		- 8		- 10K		Notes
Frequency(MHz)			100	100	66	125	83	100	66	
t _{CK} (ns)			10	10	15	8	12	10	15	
Active command to column command (same bank)		t _{RCD}	2	2	2	3	2	3	2	1
Active command to active command period (same bank)		t _{RC}	7	7	6	9	6	9	6	= [t _{RAS} + t _{RP}], 1
Active command to precharge command (same bank)		t _{RAS}	5	5	4	6	4	6	4	1
Precharge command to active command (same bank)		t _{RP}	2	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)		t _{RWL}	1	1	1	2	1	1	1	1
Active command to active command (different bank)		t _{RRD}	2	2	2	2	2	2	2	1
Self refresh exit time		t _{SREX}	1	1	1	1	1	1	1	
Last data in to active command (Auto precharge, same bank)		t _{APW}	3	3	3	5	3	4	3	= [t _{RWL} + t _{RP}], 1
Self refresh exit to command input		t _{SEC}	9	9	6	9	6	9	6	= [t _{RC}]
Precharge command to high impedance	(CL=2)	t _{HZP}	2	-	2	-	2	-	2	
	(CL=3)	t _{HZP}	3	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)		t _{APR}	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=2)	t _{EP}	-1	-	- 1	-	- 1	-	- 1	
	(CL=3)	t _{EP}	-2	-2	- 2	-2	- 2	-2	- 2	
Column command to column command		t _{CCD}	1	1	1	1	1	1	1	
Write command to data in latency		t _{WCD}	0	0	0	0	0	0	0	
DQM to data in		t _{DID}	0	0	0	0	0	0	0	
DQM to data out		t _{DOD}	2	2	2	2	2	2	2	
CKE to CLK disable		t _{CLE}	1	1	1	1	1	1	1	
Register set to active command		t _{RSA}	1	1	1	1	1	1	1	
CS̄ to command disable		t _{CDD}	0	0	0	0	0	0	0	
Power down exit to command input		t _{PEC}	1	1	1	1	1	1	1	

Parameter		Symbol	- 7K	- 7J		- 8		- 10K		Notes
Frequency(MHz)			100	100	66	125	83	100	66	
t _{CK} (ns)			10	10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l _{BSR}	1	-	1	-	1	-	1	
	(CL=3)	l _{BSR}	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	l _{BSH}	2	-	2	-	2	-	2	
	(CL=3)	l _{BSH}	3	3	3	3	3	3	3	
Burst stop to write data ignore		l _{BSW}	0	0	0	0	0	0	0	

Notes : 1. I_{RCD} to I_{RRD} are recommended value.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions +/-5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.