

Structure Silicon Monolithic Integrated Circuit

Product Name Step-up DC/DC converter for medium size LCD panel

Type **BD6583MUV**

Features High efficiency PWM step-up DC/DC converter (fsw=1MHz)
High accuracy and good matching current driver 6ch
Drive up to 12 in series x 6 strings in parallel =72 white LEDs
(*white LED Vf=3.5Vmax)

○Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Condition
Maximum applied voltage1	VMAX1	7	V	TEST,VREG,SENSP,SENSN, SW,RSTB,PWMPW,PWM DRV, FAILSEL,ISETH,ISETL
Maximum applied voltage2	VMAX2	25	V	LED1, LED2, LED3, LED4, LED5, LED6, VBAT
Maximum applied voltage3	VMAX3	50.5	V	VDET
Power dissipation1	Pd1	500	mW	*1
Power dissipation2	Pd2	780	mW	*2
Power dissipation3	Pd3	1510	mW	*3
Operating temperature range	Topr	-30 ~ +85	°C	-
Storage temperature range	Tstg	-55 ~ +150	°C	-

(*1) It will be reduced every 4.0mW/°C (Ta>25°C) when it's not mounted on a heat radiation Board.

(*2) it will be reduced every 6.2mW/°C (Ta>25°C) when It's not mounted on 1 layer board (ROHM Standard board) and Copper foil area 0mm²

(*3) It will be reduced every 12.1mW/°C (Ta>25°C) when it's mounted on 4 layer board (JEDEC Compliant board) and Copper foil area 6.28mm² on 1st layer and Copper foil area 5655.04mm². 2nd-4th layer.

○Operating conditions (Ta=-30 to +85°C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ	Max		
Supply voltage	VBAT	2.7 ~ 22.0			V	

This product isn't designed to protect itself against radioactive rays.

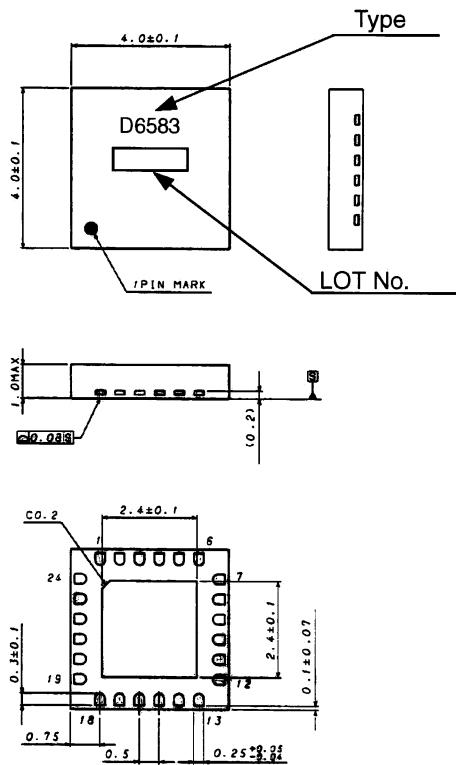
○Electrical Characteristics

(Unless otherwise noted, VBAT=12V, RSTB=2.5V, Ta = +25 °C)

Parameter	Symbol	Spec			Unit	Condition
		Min.	Typ.	Max.		
FAILSEL, PWMDRV Terminal						
Low Input Voltage range	VthL	0	-	0.2	V	
High Input Voltage range1	VthH1	1.4	-	5.0	V	VBAT>5.0V
High Input Voltage range2	VthH2	1.4	-	VBAT	V	VBAT<5.0V
Input current	lin	-	8.3	14.0	μA	Input voltage =2.5V
PWMPOW Terminal						
Low Input Voltage range	PWML	0	-	0.2	V	
High Input Voltage range1	PWMH1	1.4	-	5.0	V	VBAT>5.0V
High Input Voltage range2	PWMH2	1.4	-	VBAT	V	VBAT<5.0V
PWM pull down resistor	PWMR	300	500	700	kΩ	
RSTB Terminal						
Low Input Voltage range	RSTBL	0	-	0.2	V	
High Input Voltage range1	RSTBH1	2.25	2.5	5.0	V	VBAT>5.0V
High Input Voltage range2	RSTBH2	2.25	2.5	VBAT	V	VBAT<5.0V
Current Consumption	IRSTB	-	89	134	μA	RSTB=2.5V, LED1-6=3V
Regulator						
VREG Voltage	VREG	4.0	5.0	6.0	V	No load
Under Voltage Lock Out	UVLO	2.05	2.25	2.65	V	
Switching Regulator						
Quiescent Current 1	Iq1	-	0.6	3.4	μA	RSTB=0V, VBAT=12V
Quiescent Current 2	Iq2	-	4.6	10	μA	RSTB=0V, VBAT=22V
Current Consumption	Idd	-	3.4	5.1	mA	VDET=0V,ISETH=24kΩ
LED Control voltage	VLED	0.4	0.5	0.6	V	
Over Current Limit voltage	Ocp	70	100	130	mV	*1
SBD Open Protect	Sop	-	-	0.1	V	Detect voltage of VDET pin
Switching frequency	fSW	0.8	1.0	1.2	MHz	
Duty cycle limit	Duty	92.5	95.0	99.0	%	LED1-6=0.3V
Over Voltage Limit	Ovl	43.0	44.7	46.4	V	LED1-6=0.3V
Current driver						
LED maximum current	ILMAX	-	-	25	mA	
LED current accuracy	ILACCU	-	-	±5	%	ILED=16mA
LED current matching	ILMAT	-	-	±3	%	•Each LED current/Average (LED1- 6 current) •ILED=16mA
ISET voltage	Iset	0.5	0.6	0.7	V	
LED current limiter	ILOCP	35	60	90	mA	ISET resistance 4.7kΩg LED1, 2, 3, 4, 5, 6=0.5V
LED Terminal OverVoltage Protect	LEDOVP	10.0	11.5	13.0	V	RSTB=PWMDRV=2.5V

*1. This parameter is tested with dc measurement.

○Package outline drawing (Unit : mm)

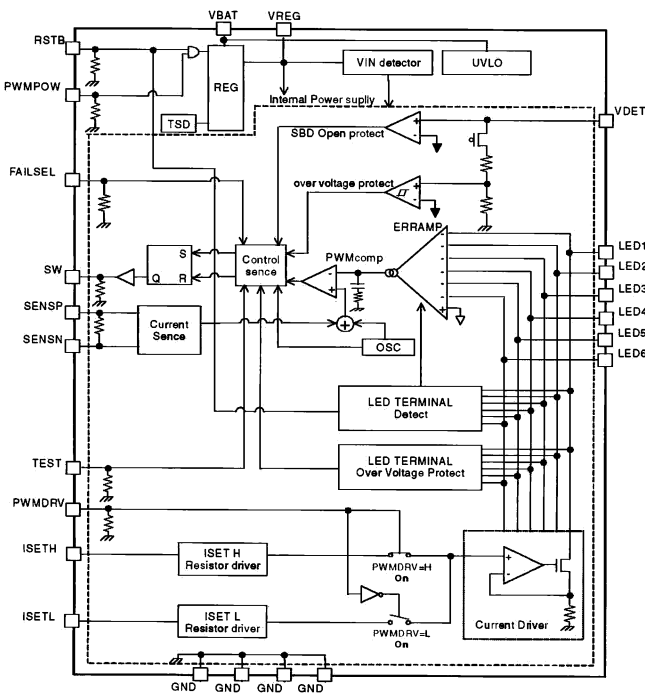


VQFN024V4040

○Terminals

PIN	PIN Name
1	VDET
2	N.C.
3	GND
4	SW
5	SENSP
6	TEST
7	SENSN
8	GND
9	ISETH
10	ISETL
11	PWMDRV
12	LED1
13	LED2
14	LED3
15	GND
16	LED4
17	LED5
18	LED6
19	FAILSEL
20	GND
21	RSTB
22	VREG
23	PWMPW
24	VBAT

○Block diagram



○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics. And, as the unused input terminals may make unstable state occur in the internal circuit, please connect them to I/O GND.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 175°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) DC/DC converter

Please select the low DCR inductors to decrease power loss for DC/DC converter.

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