Data Sheet | April 20, 2007 | FN3044.3

Radiation Hardened CMOS Static Clock Controller/Generator

The Intersil HS-82C85RH is a high performance, radiation hardened CMOS Clock Controller/Generator designed to support systems utilizing radiation hardened static CMOS microprocessors such as the HS-80C86RH. The HS-82C85RH contains a crystal controlled oscillator, reset pulse conditioning, halt/restart logic, and divide-by-256 circuitry. These features provide the means to stop the system clock, stop the clock oscillator, or run the system at a low frequency (CLK/256), enhancing control of static system power dissipation and allowing system shut-down during periods of external stress.

Static CMOS circuit design insures low operating power and permits operation with an external frequency source from DC to 15MHz. Crystal controlled operation to 15MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors. Outputs are guaranteed compatible with both CMOS and TTL specifications. The Intersil hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95820. A "hot-link" is provided on our homepage for downloading.
http://www.intersil.com/military/

Features

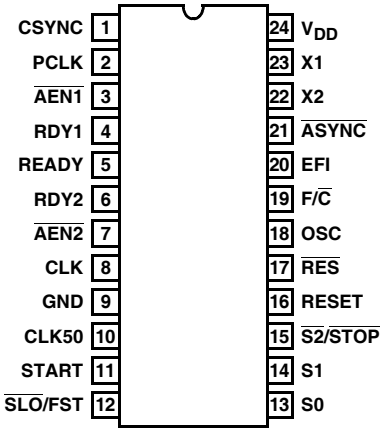
- Electrically Screened to SMD # 5962-95820
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardened
  - Total Dose . . . . . 100 krad(Si) (Max)
  - Transient Upset . . . . . $>10^8$ rad(Si)/s
  - Latch Up Free EPI-CMOS
- Very Low Power Consumption
- Pin Compatible with NMOS 8285 and Intersil 82C85
- Generates System Clocks for Microprocessors and Peripherals
- Complete Control Over System Clock Operation for Very Low System Power
  - Stop-Oscillator
  - Stop-Clock
  - Low Frequency (Slo) Mode
  - Full Speed Operation
- DC to 15MHz Operation (DC to 5MHz System Clock)
- Generates Both 50% and 33% Duty Cycle Clocks (Synchronized)
- Uses Either Parallel Mode Crystal Circuit or External Frequency Source
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range . . . . . -55°C to +125°C

Ordering Information

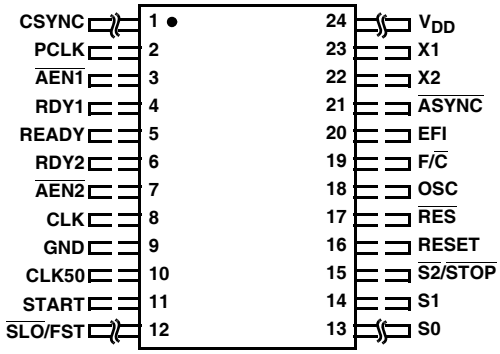
ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962R9582001VJC	HS1-82C85RH-Q	Q 5962R95 82001VJC	-55 to +125	24 Ld SBDIP	D24.6
5962R9582001VXC	HS9-82C85RH-Q	Q 5962R95 82001VXC	-55 to +125	24 Ld Flatpack	K24.A
5962R9582001QJC	HS1-82C85RH-8	Q 5962R95 82001VJC	-55 to +125	24 Ld SBDIP	D24.6
5962R9582001QXC	HS9-82C85RH-8	Q 5962R95 82001VXC	-55 to +125	24 Ld Flatpack	K24.A

Pinouts

24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T24
TOP VIEW



24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F24
TOP VIEW



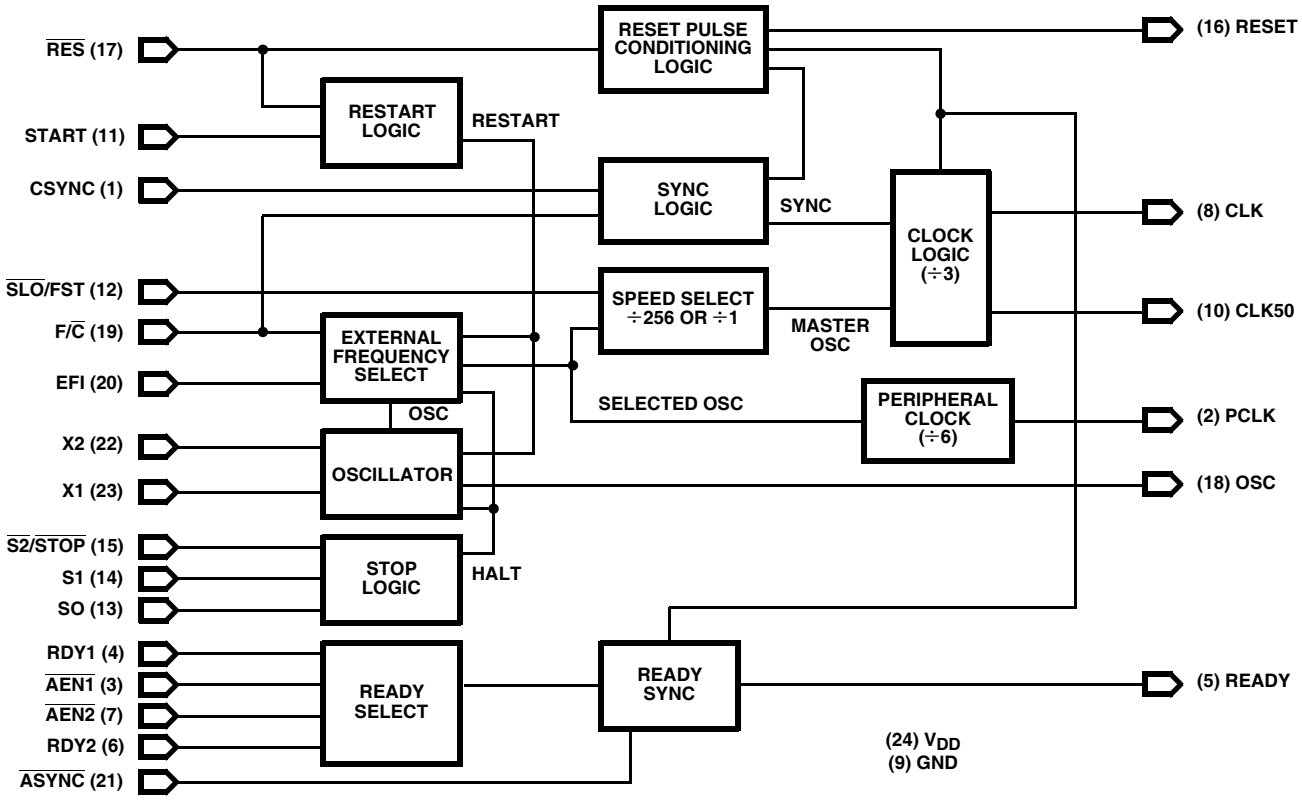
Pin Descriptions

PIN	PIN NUMBER	TYPE	DESCRIPTION
X1 X2	23 22	I O	CRYSTAL CONNECTIONS: X1 and X2 are the crystal oscillator connections. The crystal frequency must be three times the maximum desired processor clock frequency. X1 is the oscillator circuit input and X2 is the output of the oscillator circuit.
EFI	20	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input signal. This input signal should be a square wave with a frequency of three times the maximum desired CLK output frequency.
F/$\overline{C}$	19	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ selects either the crystal oscillator or the EFI input as the main frequency source. When F/$\overline{C}$ is LOW, the HS-82C85RH clocks are derived from the crystal oscillator circuit. When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input. F/$\overline{C}$ cannot be dynamically switched during normal operation.
START	11	I	A low-to-high transition on START will restart the CLK, CLK50 and PCLK outputs after the appropriate restart sequence is completed. When in the crystal mode (F/$\overline{C}$ LOW) with the oscillator stopped, the oscillator will be restarted when a Start command is received. The CLK, CLK50 and PCLK outputs will start after the oscillator input signal (X1) reaches the Schmitt trigger input threshold and an 8K internal counter reaches terminal count. If F/$\overline{C}$ is HIGH (EFI mode), CLK, CLK50 and PCLK will restart within 3 EFI cycles after START is recognized. The HS-82C85RH will restart in the same mode ($\overline{SLO}$/FST) in which it stopped. A high level on START disables the STOP mode.
S0 S1 $\overline{S2}$/$\overline{STOP}$	13 14 15	I I I	$\overline{S2}$/$\overline{STOP}$, S1, S0 are used to stop the HS-82C85RH clock outputs (CLK, CLK50, PCLK) and are sampled by the rising edge of CLK. CLK, CLK50 and PCLK are stopped by $\overline{S2}$/$\overline{STOP}$, S1, S0 being in the LHH state on the low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low). When in the crystal mode (F/$\overline{C}$) low and a STOP command is issued, the HS-82C85RH oscillator will stop along with the CLK, CLK50 and PCLK outputs. When in the EFI mode, only the CLK, CLK50 and PCLK outputs will be halted. The oscillator circuit if operational, will continue to run. The oscillator and/or clock is restarted by the START input signal going true (HIGH) or the reset input ($\overline{RES}$) going low.

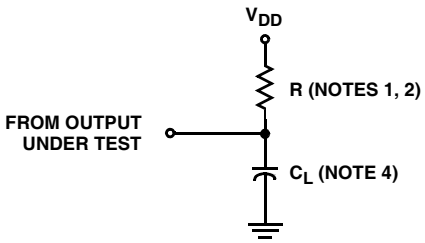
Pin Descriptions (Continued)

PIN	PIN NUMBER	TYPE	DESCRIPTION
$\overline{SLO}$/FST	12	I	$\overline{SLO}$/FST is a level-triggered input. When HIGH, the CLK and CLK50 outputs run at the maximum frequency (crystal or EFI frequency divided by 3). When LOW, CLK and CLK50 frequencies are equal to the crystal or EFI frequency divided by 768. $\overline{SLO}$/FST mode changes are internally synchronized to eliminate glitches on the CLK and CLK50. START and STOP control of the oscillator or EFI is available in either the SLOW or FAST frequency modes. The $\overline{SLO}$/FST input must be held LOW for at least 195 OSC/EFI clock cycles before it will be recognized. This eliminates unwanted frequency changes which could be caused by glitches or noise transients. The $\overline{SLO}$/FST input must be held HIGH for at least 6 OSC/EFI clock pulses to guarantee a transition to FAST mode operation.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the HS-80C86RH processor and other peripheral devices. When $\overline{SLO}$/FST is high, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by three. When $\overline{SLO}$/FST is low, CLK has an output frequency which is equal to the crystal or EFI input frequency divide by 768. CLK has a 33% duty cycle.
CLK50	10	O	50% DUTY CYCLE CLOCK: CLK50 is an auxiliary clock with a 50% duty cycle and is synchronized to the falling edge of CLK. When $\overline{SLO}$/FST is high, CLK50 has an output frequency which is equal to the crystal or EFI input frequency divided by 3. When $\overline{SLO}$/FST is low, CLK50 has an output frequency equal to the crystal or EFI input frequency divided by 768.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is equal to the crystal or EFI input frequency divided by six and has a 50% duty cycle. PCLK frequency is unaffected by the state of the $\overline{SLO}$/FST input.
OSC	18	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal oscillator circuit. OSC is unaffected by the state of the $\overline{SLO}$/FST input. When the HS-82C85RH is in the crystal mode (F/$\overline{C}$ LOW) and a STOP command is issued, the OSC output will stop in the HIGH state. When the HS-82C85RH is in the EFI mode (F/$\overline{C}$ HIGH), the oscillator (if operational) will continue to run when a STOP command is issued and OSC remains active.
$\overline{RES}$	17	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The HS-82C85RH provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. $\overline{RES}$ starts crystal oscillator operation.
RESET	16	O	RESET: RESET is an active HIGH signal which is used to reset the HS-80C86RH processor. Its timing characteristics are determined by $\overline{RES}$. RESET is guaranteed to be HIGH for a minimum of 16 CLK pulses after the rising edge of $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple HS-82C85RHs to be synchronized to provide multiple in-phase clock signals. When CSYNC is HIGH, the internal counters are reset and force CLK, CLK50 and PCLK into a HIGH state. When CSYNC is LOW, the internal counters are allowed to count and the CLK, CLK50 and PCLK outputs are active. CSYNC must be externally synchronized to EFI.
$\overline{AEN1}$ $\overline{AEN2}$	3 7	I I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses.
RDY1 RDY2	4 6	I I	BUS READY: (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	21	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is used to inform the HS-80C86RH that it may conclude a pending data transfer.
GND	9	I	Ground
V_{DD}	24	I	+5V power supply

Functional Diagram



AC Test Circuit



NOTES:

1. R = 370Ω at V = 2.25 for CLK and CLK50 outputs.
2. R = 494Ω at V = 2.87 for all other outputs.
3. C_L = 50pF.
4. C_L Includes probe and jig capacitance.

Waveforms

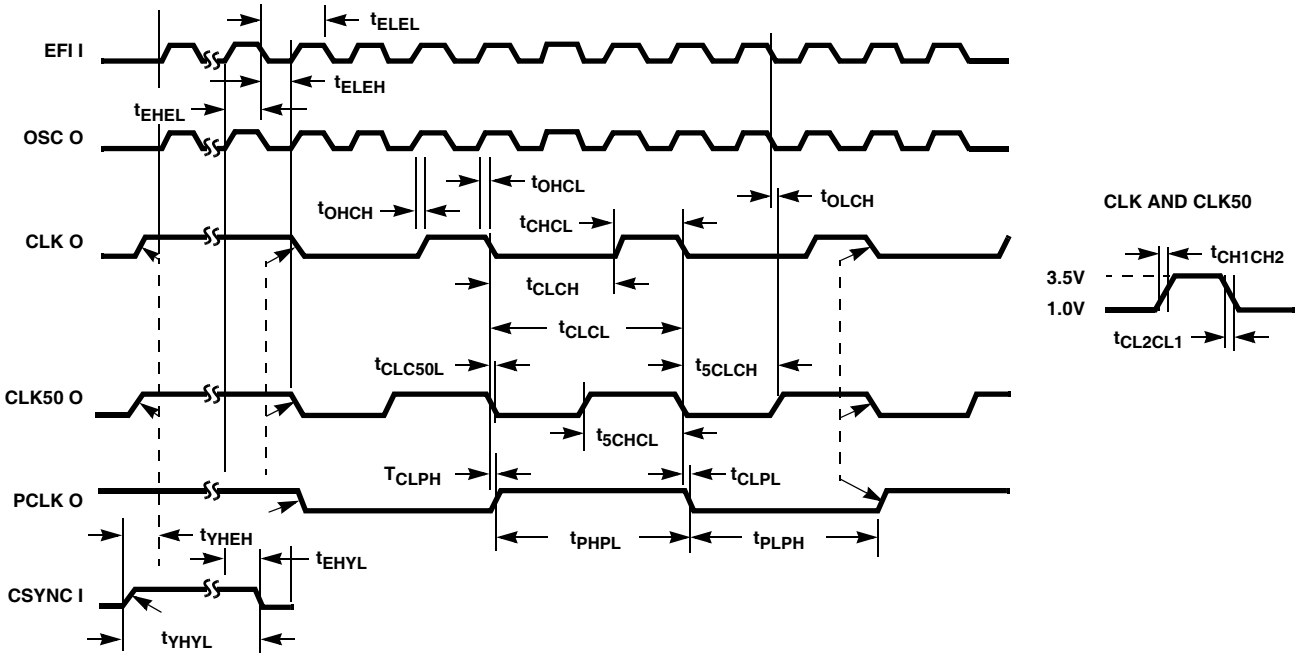


FIGURE 1. WAVEFORMS FOR CLOCKS

NOTE: All timing measurements are made at 1.5V, unless otherwise noted.

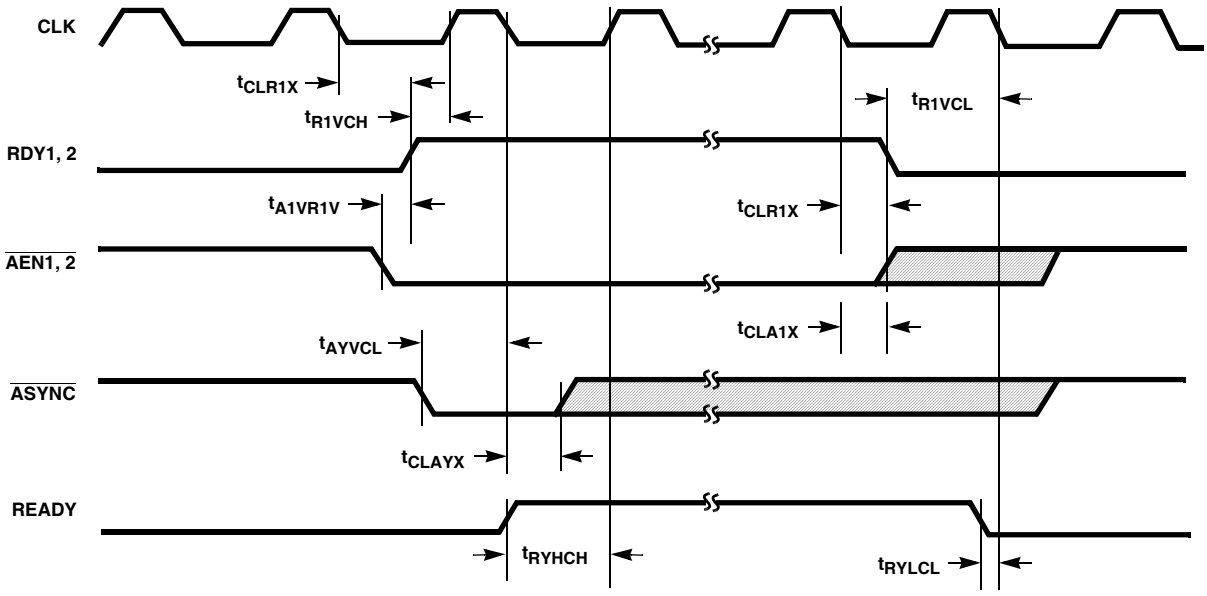


FIGURE 2. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

Waveforms (Continued)

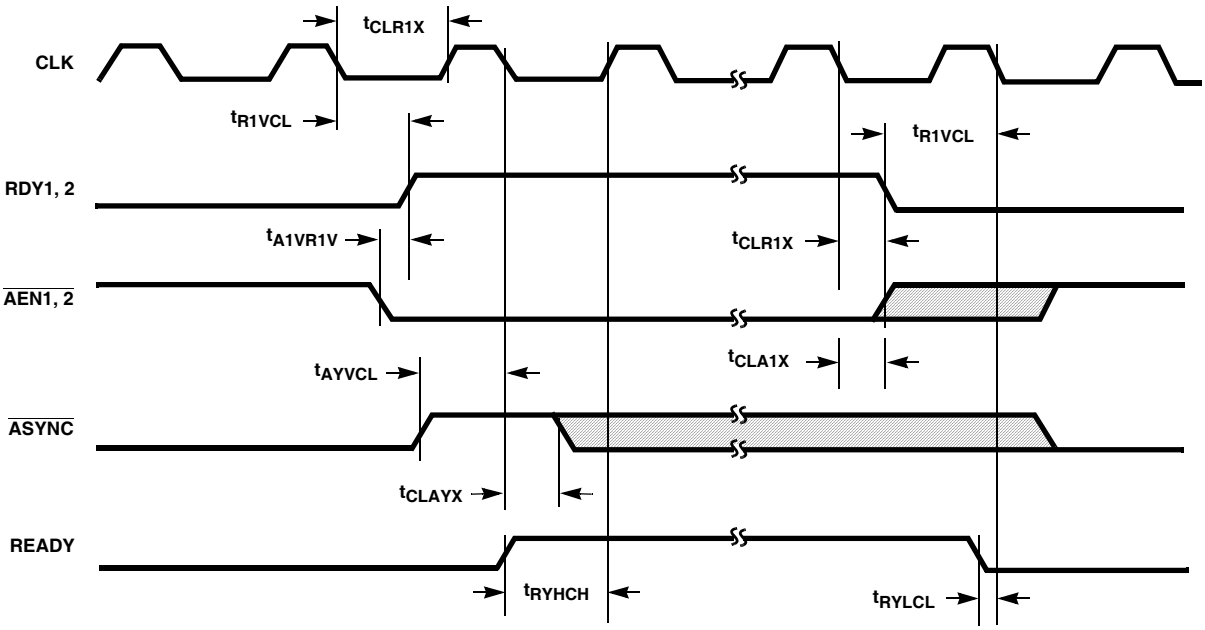


FIGURE 3. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

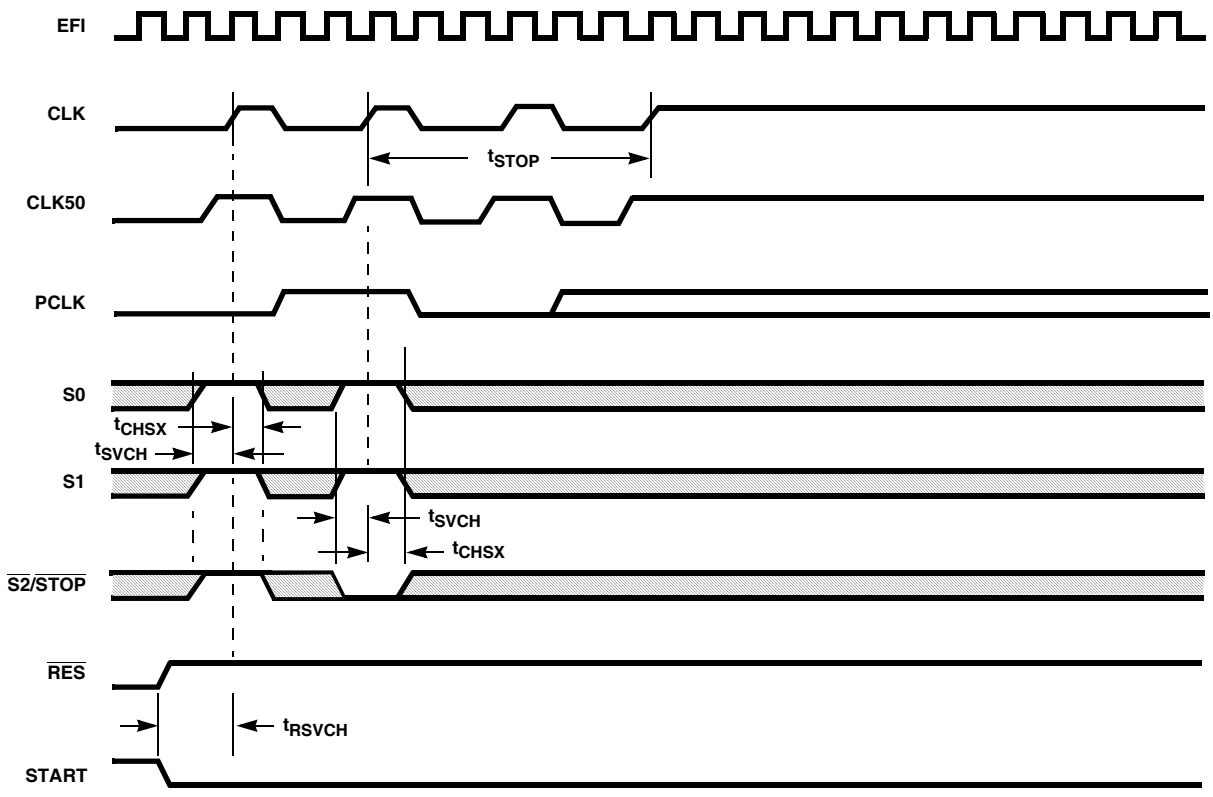


FIGURE 4. CLOCK STOP (F/$\overline{C}$ HIGH OR F/$\overline{C}$ LOW)

Waveforms (Continued)

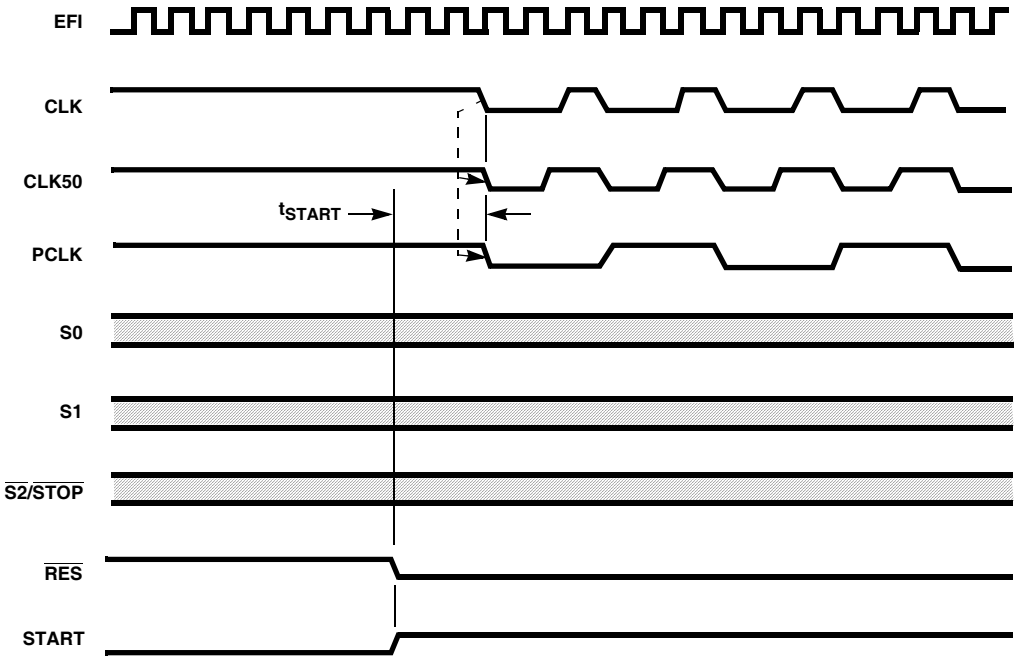


FIGURE 5. CLOCK START (F/$\overline{C}$ HIGH)

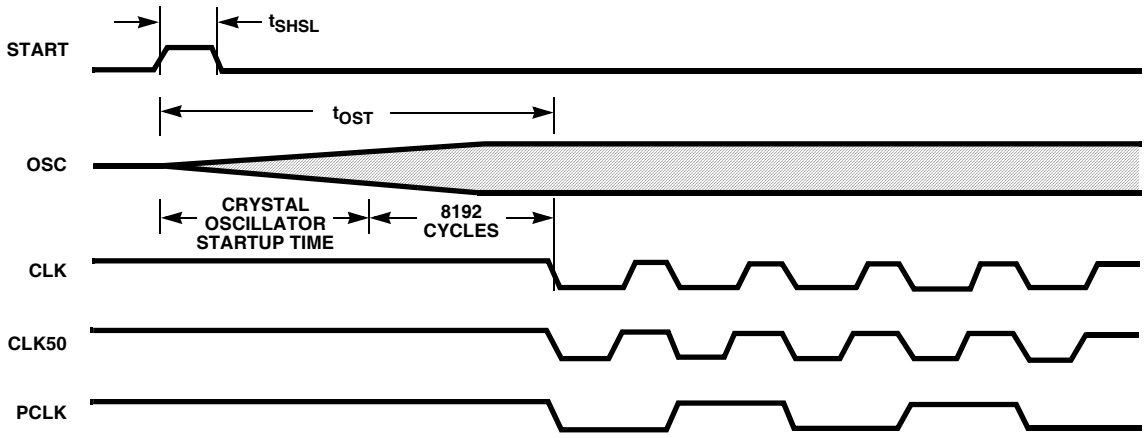


FIGURE 6. CLOCK START (F/$\overline{C}$ LOW)

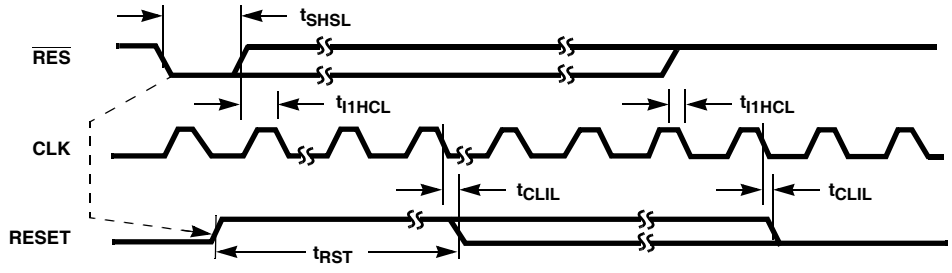


FIGURE 7. RESET TIMING (CLK RUNNING WITH F/$\overline{C}$ LOW - OSC MODE; CLK RUNNING - OR STOPPED WITH F/$\overline{C}$ HIGH EFI MODE)

Waveforms (Continued)

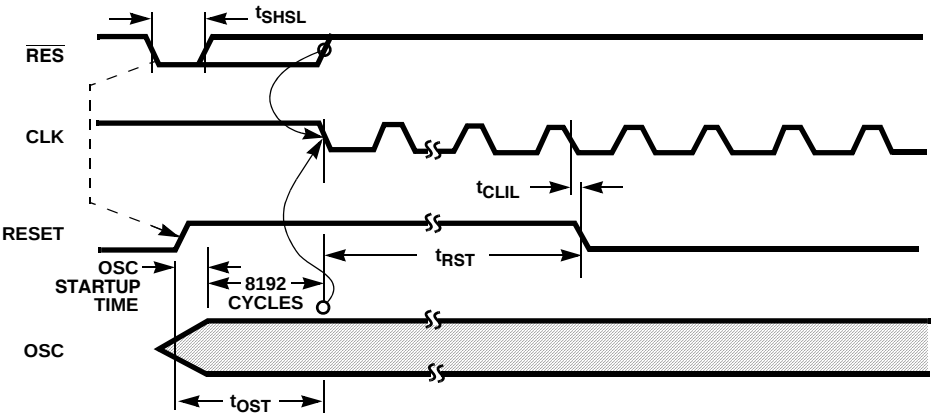


FIGURE 8. RESET TIMING OSCILLATOR STOPPED (F/$\overline{C}$ LOW)

NOTE: CLK, CLK50, PCLK remain in the high state until $\overline{RES}$ goes high and 8192 valid oscillator cycles have been registered by the HS-82C85RH internal counter t_{OST} time period). After $\overline{RES}$ goes high and CLK, CLK50, PCLK become active, the RESET output will remain high for a minimum of 16 CLK cycles (t_{RST}).

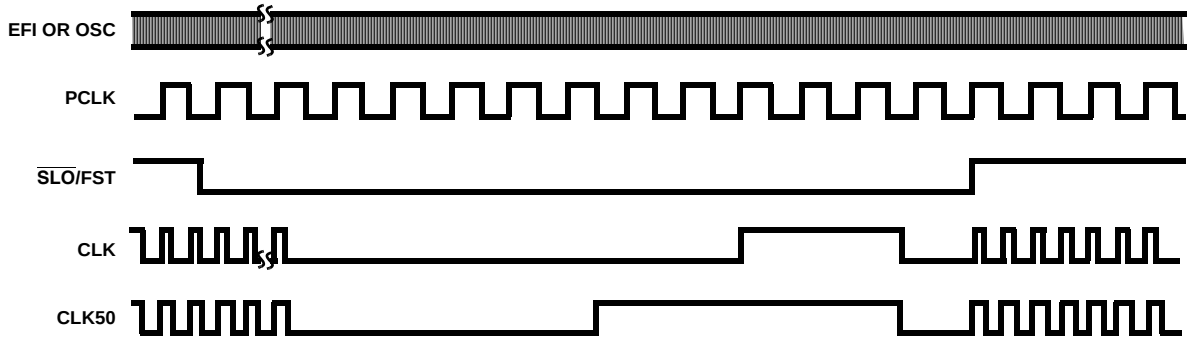


FIGURE 9. SLO/FST TIMING OVERVIEW

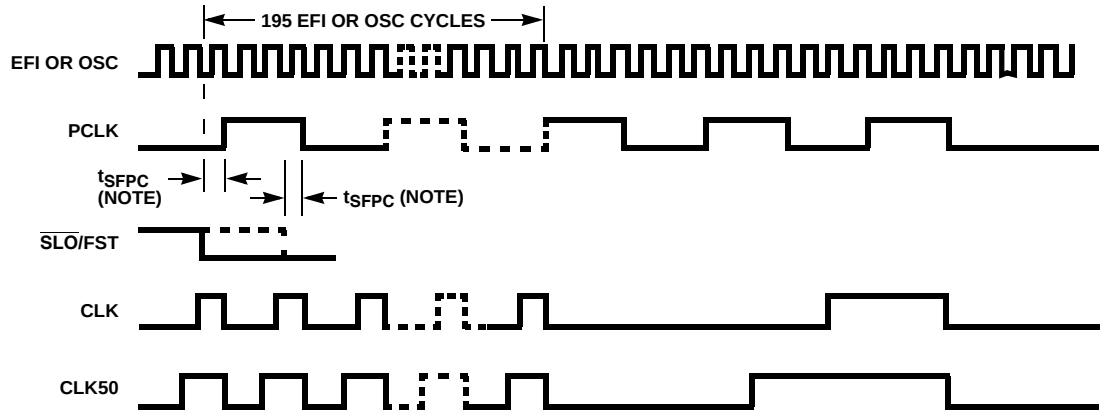


FIGURE 10. FAST TO SLOW CLOCK MODE TRANSITION

NOTE: If t_{SFPC} is not met on one edge of PCLK, $\overline{SLO}$/FST will be recognized on the next edge of PCLK.

Waveforms (Continued)

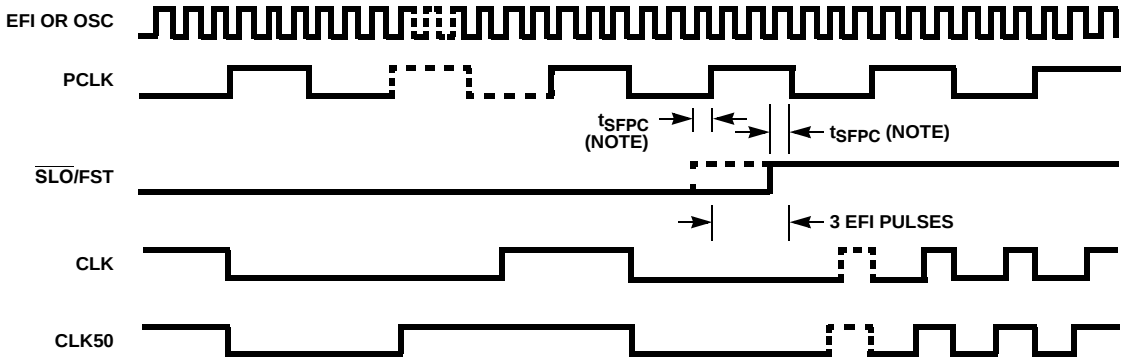


FIGURE 11. SLOW TO FAST CLOCK MODE TRANSITION

NOTE: If t_{SFPC} is not met on one edge of PCLK, SLO/FST will be recognized on the next edge of PCLK.

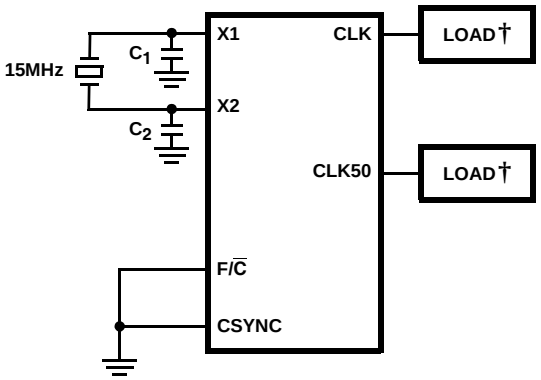


FIGURE 12. CLOCK HIGH AND LOW TIME (USING X1, X2)

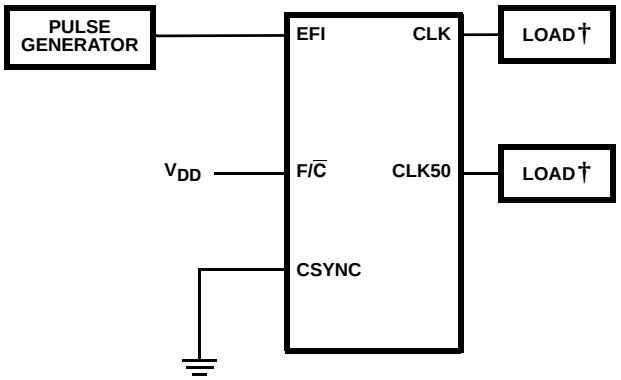


FIGURE 13. CLOCK HIGH AND LOW TIME (USING EFI)

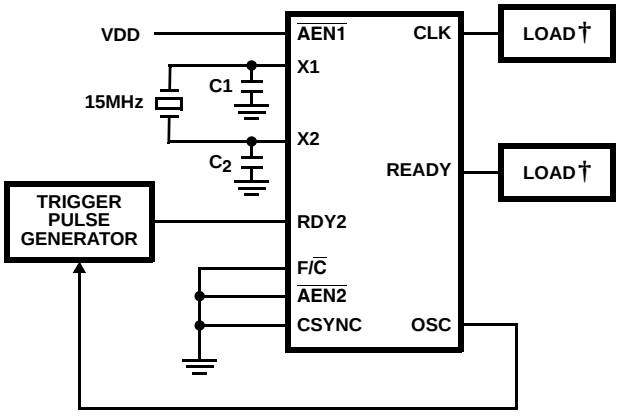


FIGURE 14. READY TO CLOCK (USING X1, X2)

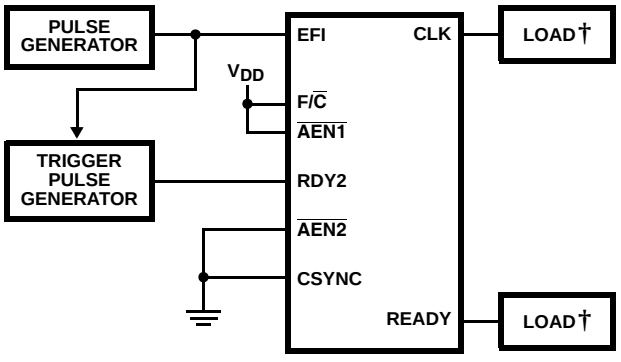
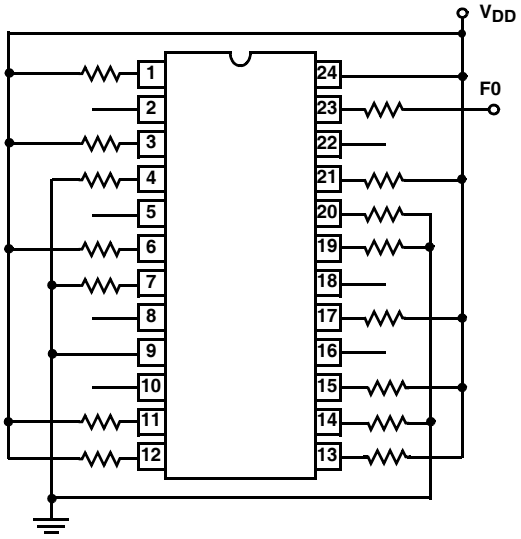


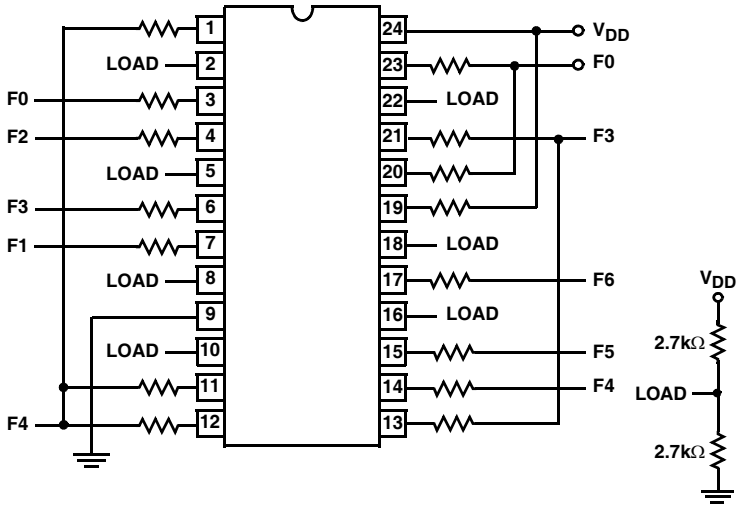
FIGURE 15. READY TO CLOCK (USING EFI)

† C_L = 50pF

Burn-In Circuits



STATIC CONFIGURATION



DYNAMIC CONFIGURATION

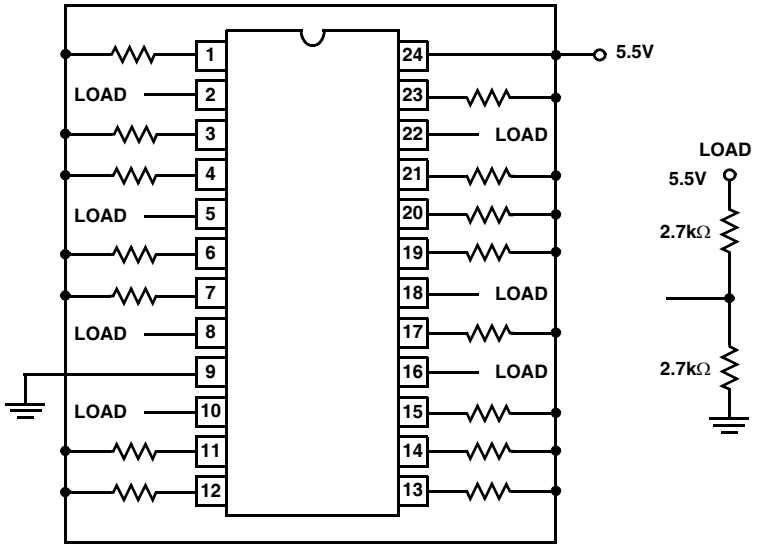
NOTES:

5. R = 10kΩ ±10%.
6. V_{DD} = 6.0V ±5%.
7. T_A = 125°C Min.
8. Package Code: SZ (24 Lead DIP).
9. F0 is 50% duty cycle square wave pulse burst. F0 is left low after pulse burst.

NOTES:

10. R = 10kΩ ±10%.
11. V_{DD} = 6.0V ±5% (Burn-In); V_{DD} = 5.5V ±5% (Life Test).
12. T_A = 125°C Min.
13. Package Code: SZ (24 Lead DIP).
14. F0 = 10kHz, 50% duty cycle.
15. F1 = F0/2; F2 = F1/2; F3 = F2/2, F4 = F3/2; F5 = F4/2.

Irradiation Circuit



NOTES:

16. R = 47kΩ ±10%.
17. Pins tied to V_{SS} (0V): Pin 9.
18. Pins with loads: 2, 5, 8, 10, 16, 18, 22.
19. Pins tied to V_{DD}: 1, 3, 4, 6, 7, 11 - 15, 17, 19 - 21, 23, 24.
20. V_{DD} = 5.5V ±0.5V.

Functional Description

The HS-82C85RH Static Clock Controller/Generator provides simple and complete control of static CMOS system operating modes. The HS-82C85RH can operate with either an external crystal or an external frequency source and can support full speed, slow, stop-clock and stop-oscillator operation. While it is directly compatible with the Intersil HS-80C86RH CMOS 16-bit static microprocessor, the HS-82C85RH can also be used for general purpose system clock control.

Separate signals are provided on the HS-82C85RH for stop and start control of the crystal oscillator and clock outputs. A single control line determines fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. A clock synchronization input is provided to allow the use of multiple HS-82C85RHs in the same system. The HS-82C85RH generates the proper HS-80C86RH reset pulse, and it also handles all data transfer timing by generating the HS-80C86RH ready signal.

Automatic maximum mode HS-80C86RH software HALT instruction decode logic is present to ease the design of software-based clock control systems and provides complete software control of STOP mode operation. Automatic minimum mode software HALT instruction decoding can be easily implemented with a single 74HC74 device. Restart logic insures valid clock start-up and complete synchronization of CLK, CLK50 and PCLK.

Static Operating Modes

The HS-82C85RH Static Clock Controller can be dynamically set to operate in any one of four modes at any one time: FAST, SLOW, STOP-CLOCK and STOP-OSCILLATOR. Each mode has distinct power and performance characteristics which can be matched to the needs of a particular system at a specific time (see Table 1).

Keep in mind that a single system may require all of these operating modes at one time or another during normal operation. A design need not be limited to a single operating mode or a specific combination of modes. The appropriate operating mode can be matched to the power-performance level needed at a specific time or in a particular circumstance.

Reset Logic

The HS-82C85RH reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate there set timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the HS-82C85RH. When in the crystal oscillator (F/$\overline{C}$ = LOW) or the EFI (F/$\overline{C}$ = HIGH) mode, a LOW state on the $\overline{RES}$ input will set the RESET output to the HIGH state. It will also restart the oscillator circuit if it is in the idle state. The RESET output is guaranteed to stay in the HIGH state for a minimum of 16 CLK cycles after a low-to-high transition of the RES input.

An oscillator restart count sequence will not be disturbed by RESET if this count is already in progress. After the restart counter expires, the RESET output will stay HIGH at least for 16 periods of CLK before going LOW. RESET can be kept high beyond this time by a continuing low input on the $\overline{RES}$ input.

If F/C is low (crystal oscillator mode), a low state on $\overline{RES}$ starts the crystal oscillator circuit. The stopped outputs remain inactive, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

This 8192 count requirement insures that the CLK, CLK50 and PCLK outputs will meet minimum clock requirements and will not be affected by unstable oscillator characteristics which may exist during the oscillator start-up sequence. This sequence is also followed when a START command is issued while the HS-82C85RH oscillator is stopped.

TABLE 1. STATIC SYSTEM OPERATING MODE CHARACTERISTICS

OPERATING MODE	DESCRIPTION	POWER LEVEL	PERFORMANCE
Stop-Oscillator	All system clocks and main clock oscillator are stopped	Maximum savings	Slowest response due to oscillator restart time
Stop-Clock	System CPU and peripherals clocks stop but main clock oscillator continues to run at rated frequency	Reduced system power	Fast restart - no oscillator restart time
Slow	System CPU clocks are slowed while peripheral clock and main clock oscillator run at rated frequency	Power dissipation slightly higher than Stop-Clock	Continuous operation at low frequency
Fast	All clocks and oscillators run at rated frequency	Highest power	Fastest response

Oscillator/Clock Start Control

Once the oscillator is stopped (or committed to stop) or at power-on, the restart sequence is initiated by a HIGH state on START or LOW state on $\overline{RES}$. If F/$\overline{C}$ is HIGH, then restart occurs immediately after the START or $\overline{RES}$ input is synchronized internally. This insures that stopped outputs (CLK, PCLK, OSC and CLK50) start cleanly with the proper phase relationship.

If F/$\overline{C}$ is low (crystal oscillator mode), a HIGH state on the START input or a low state on $\overline{RES}$ causes the crystal oscillator to be restarted. The stopped outputs remain stopped, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

Typically, any input signal which meets the START input timing requirements can be used to start the HS-82C85RH. In many cases, this would be the INT output from an HS-82C59A CMOS Priority Interrupt Controller (see Figure 16). This output, which is active high, can be connected to both the HS-82C85RH START pin and to the INTR input on the microprocessor.

When the INT output becomes active (as a result of a "restart" IRQ or a system reset), the oscillator/clock circuit on the HS-82C85RH will restart. Upon completion of the appropriate restart sequence, the CLK signal to the CPU will become active. The CPU can then respond to the still-pending interrupt request.

Oscillator/Clock Stop Control

The S0, S1, and $\overline{S2}$/$\overline{STOP}$ control lines determine when the HS-82C85RH clock outputs or oscillator will stop. These three lines are designed to connect directly to the MAXimum mode HS-80C86RH status lines as shown in Figure 17.

When used in this configuration, the HS-82C85RH will automatically recognize a software HALT command from the HS-80C86RH and stop the system clocks or oscillator. This allows complete software control of the STOP function.

If the HS-80C86RH is used in the MINimum mode, the HS-82C85RH can be controlled using the $\overline{S2}$/$\overline{STOP}$ input (with S0 and S1 held high). This can be done using the circuit shown in Figure 18. Since the HS-80C86RH, when executing a halt instruction in minimum mode, issues a single ALE pulse with no corresponding bus signals ($\overline{DEN}$ remains high), the ALE pulse will be clocked through the 74HC74 and put the HS-82C85RH into stop mode.

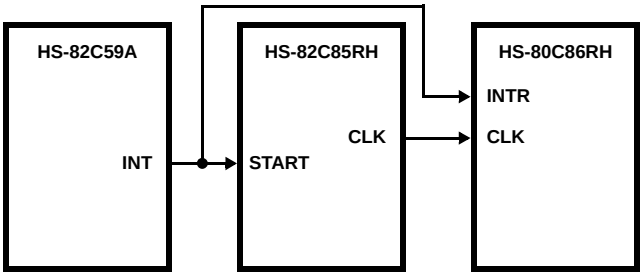


FIGURE 16. START CONTROL USING HS-82C59ARH INTERRUPT CONTROLLER

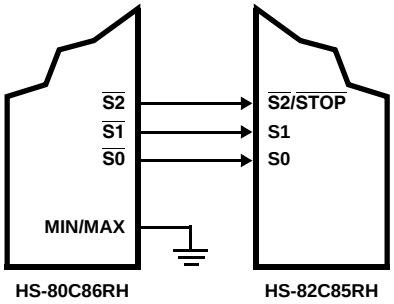


FIGURE 17. STOP CONTROL USING HS-80C86RH MAXIMUM MODE STATUS LINES

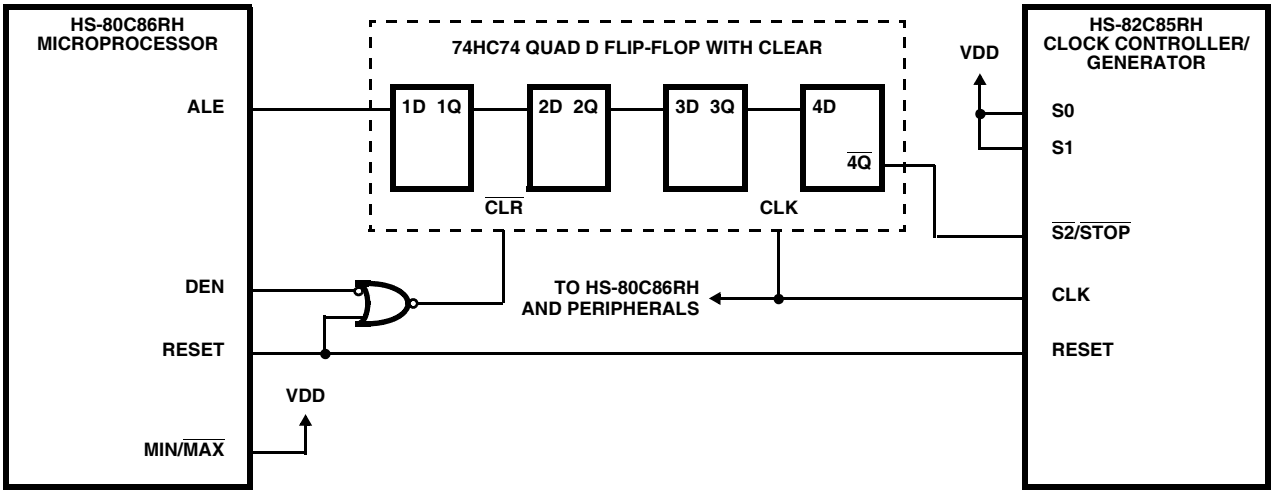


FIGURE 18. STOP CONTROL USING HS-80C86RH IN MINIMUM MODE

The HS-82C85RH status inputs $\overline{S2}/\overline{STOP}$, S1, S0 are sampled on the rising edge of CLK. The oscillator (F/$\overline{C}$ LOW only) and clock outputs are stopped by $\overline{S2}/\overline{STOP}$, S1, S0 being in the LHH state on a low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 will stop in the logic HIGH state after two additional complete cycles of CLK. PCLK stops in its current state (HIGH or LOW). This is true for both SLOW and FAST mode operation.

Stop-Oscillator Mode

When the HS-82C85RH is stopped while in the crystal mode (F/C LOW), the oscillator, in addition to all system clock signals (CLK, CLK50 and PCLK), are stopped. CLK and CLK50 stop in the high state. PCLK stops in its current state (high or low).

With the oscillator stopped, HS-82C85RH power drops to its lowest level. All clocks and oscillators are stopped. All devices in the system which are driven by the HS-82C85RH go into the lowest power standby mode. The HS-82C85RH also goes into standby and requires a power supply current of less than 100mA.

Stop-Clock Mode

When the HS-82C85RH is in the EFI mode (F/$\overline{C}$ HIGH) and a STOP command is issued, all system clock signals (CLK, CLK50 and PCLK) are stopped. CLK and CLK50 stop in the high state. PCLK stops in its current state (high or low).

The HS-82C85RH can also provide its own EFI source simply by connecting the OSC output to the EFI input and pulling the F/$\overline{C}$ input HIGH. This puts the HS-82C85RH into the External Frequency Mode using its own oscillator as an external source signal (see Figure 19). In this configuration, when the HS-82C85RH is stopped in the EFI mode, the oscillator continues to run. Only the clocks to the CPU and peripherals (CLK, CLK50 and PCLK) are stopped.

Clock Slow/Fast Operation

The $\overline{SLO}$/FST input determines whether the CLK and CLK50 outputs run at full speed (crystal or EFI frequency divided by 3) or at slow speed (crystal or EFI frequency divided by 768) (see Figure 20). When in the SLOW mode, HS-82C85RH stop-clock and stop-oscillator functions operate in the same manner as in the FAST mode, and the frequency of PCLK is unaffected.

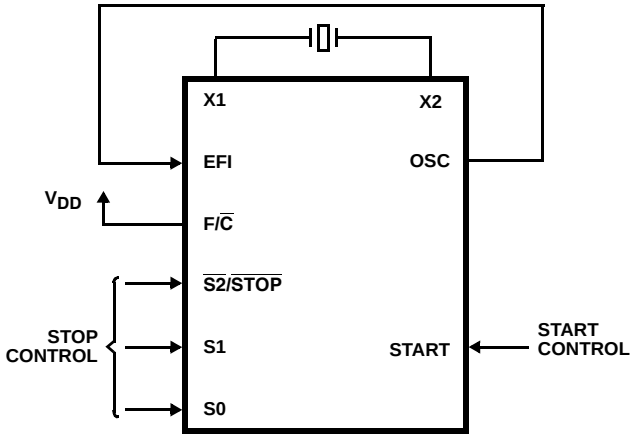


FIGURE 19. STOP-CLOCK MODE IN EFI MODE WITH OSCILLATOR AS FREQUENCY SOURCE

The SLOW mode allows the CPU and the system to operate at a reduced rate which, in turn, reduces system power. For example, the operating power for the HS-80C86RH CPU is 10mA/MHz of clock frequency. When the SLOW mode is used in a typical 5MHz system, CLK and CLK50 run at approximately 20kHz. At this reduced frequency, the average operating current of the CPU drops to 200mA. Adding the HS-80C86RH 500mA standby current brings the total current to 700mA.

While the CPU and peripherals run slower and the HS-82C85RH CLK and CLK50 outputs switch at a reduced frequency, the main HS-82C85RH oscillator is still running at the maximum frequency (determined by the crystal or EFI input frequency.) Since CMOS power is directly related to operating frequency, HS-82C85RH power supply current will typically be reduced by 25% - 35%.

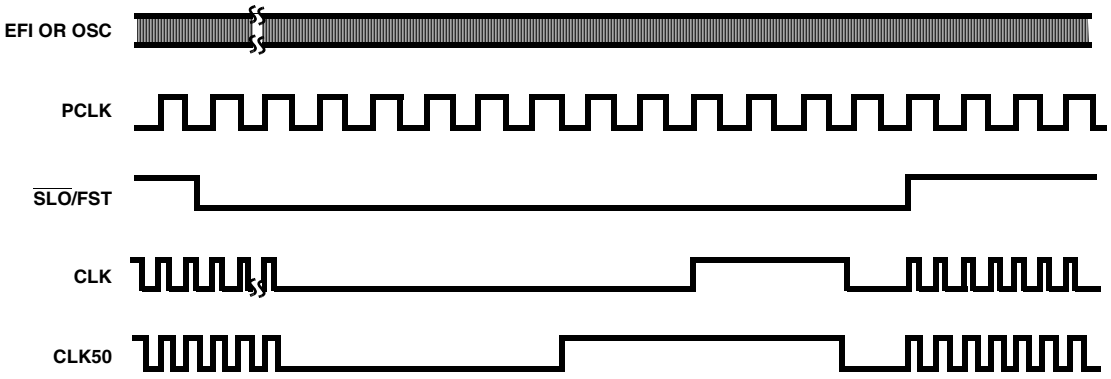


FIGURE 20. SLOW/FAST TIMING OVERVIEW

Internal logic requires that the $\overline{SLO}$/FST pin be held low for at least 195 oscillator or EFI clock pulses before the SLOW mode command is recognized. This requirement eliminates unwanted FAST-to-SLOW mode frequency changes which could be caused by glitches or noise spikes.

To guarantee FAST mode recognition, the $\overline{SLO}$/FST pin must be held high for at least 3 OSC or EFI pulses. The HS-82C85RH will begin FAST mode operation on the next PCLK edge after FAST command recognition. Proper CLK and CLK50 phase relationships are maintained and minimum pulse width specifications are met.

FAST-to-SLOW or SLOW-to-FAST mode changes will occur on the next rising or falling edge of PCLK. It is important to remember that the transition time for operating frequency changes, which are dependent upon PCLK, will vary with the HS-82C85RH oscillator or EFI frequency.

Slow/Fast Mode Control

The HS-82C55ARH programmable peripheral interface can be used to provide slow/fast mode control by connecting one of the port pins directly to the $\overline{SLO}$/FST pin (see Figure 21). With the port pin configured as an output, software control of the $\overline{SLO}$/FST pin is provided by simply writing a logical one (FAST mode) or logical zero (SLOW Mode) to the corresponding port. PORT C is well-suited for this function due to its bit set and reset capabilities.

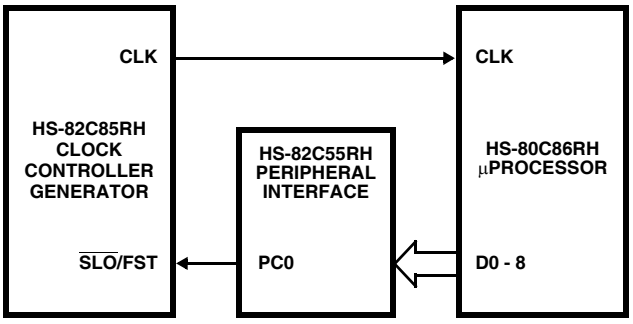


FIGURE 21. SLOW/FAST MODE CONTROL USING HS-82C55RH PERIPHERAL INTERFACE

Alternate Operating Modes

Using alternate modes of operation (slow, stop-clock, stop-oscillator) will reduce the average system operating power dissipation in a static CMOS system (see Table 2). This does not mean that system speed or throughput must be reduced. When used appropriately, the slow, stop-clock, stop-oscillator modes can make your design more power-efficient while maintaining maximum system performance.

Oscillator

The oscillator circuit of the HS-82C85RH is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived. The crystal frequency must be three times the required CPU clock. X1 and X2 are the two crystal input connections. The output of the oscillator is buffered and available at the OSC output (pin 18) for generation of other system timing signals.

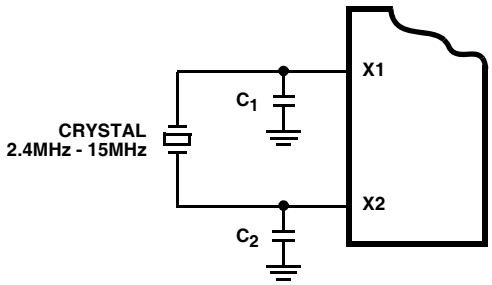
TABLE 2. TYPICAL SYSTEM POWER SUPPLY CURRENT FOR STATIC CMOS OPERATING MODES

	FAST	SLOW	STOP-CLOCK	STOP-OSC
CPU Frequency	5MHz	20kHz	DC	DC
XTAL Frequency	15MHz	15MHz	15MHz	DC
IDD				
HS-80C86RH	50mA	2.5mA	250µA	250µA
HS-82C85RH	24.7mA	16.9mA	14.1mA	24.4µA
HS-82C08RH	1.0mA	10.0µA	1.0µA	1.0µA
82C82	1.7mA	6.5mA	1.0µA	1.0µA
HS-82C54RH	943.0µA	915.0µA	1.0µA	1.0µA
HS-82C55ARH	3.2µA	1.2µA	1.0µA	1.0µA
74HCXX + Other	2.9mA	110.0µA	90.0µA	90.0µA
HS-65262RH	4.0mA	50.0µA	10.0µA	10.0µA
HS-6617RH	6.3mA	52.5µA	12.0µA	12.0µA

NOTE: All measurements taken at room temperature, VDD = +5.0V. Power supply current levels will be dependent upon system configuration and frequency of operation.

For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) are recommended. Capacitors C1 and C2 are chosen such that their combined capacitance matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

The crystal/capacitor configuration and the formula used to determine the capacitor values are shown in Figure 22. Crystal Specifications are shown in Table 3. For additional information on crystal operation, see Intersil publication Tech Brief 47.



$$CT = \frac{C1 \bullet C2}{C1 + C2}$$ (Including stray capacitance)

FIGURE 22. CRYSTAL CONNECTION

TABLE 3. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	2.4MHz to 15MHz
Type of Operation	Parallel Resonant, Fund. Mode
Load Capacitance	20pF or 32pF
R Series (Max)	56Ω (f = 15MHz, C_L = 32pF), 105Ω (f = 15MHz, C_L = 20pF)

Frequency Source Selection

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the source frequency for clock generation. If the EFI input is selected as the source, the oscillator section (OSC output) can be used independently for another clock source. If a crystal is not used, then crystal input X1 (pin 23) must be tied to VDD or GND and X2 (pin 22) should be left open. If the EFI mode is not used, then EFI (pin 20) should be tied to VDD or GND.

Clock Generator

The clock generator consists of two synchronous divide-by-three counters with special clear inputs that inhibit the counting. One counter generates a 33% duty cycle waveform (CLK) and the other generates a 50% duty cycle waveform (CLK50). These two counters are negative-edge synchronized, with the low-going transitions of both waveforms occurring on the same oscillator transition. The CLK and CLK50 output frequencies are one-third of the base input frequency when $\overline{SLO}$/FST is high and are equal to the base input frequency divided by 768 when $\overline{SLO}$/FST is low.

The CLK output is a 33% duty cycle clock signal designed to drive the HS-80C86RH microprocessor directly. CLK50 has a 50% duty cycle output synchronous with CLK, designed to drive coprocessors and peripherals requiring a 50% duty cycle clock.

PCLK is a peripheral clock signal with an output frequency equal to the oscillator or EFI frequency divided by 6. PCLK has a 50% duty cycle. PCLK is unaffected by $\overline{SLO}$/FST. When the HS-82C85RH is placed in the STOP mode, PCLK will remain in its current state (logic high or logic low) until a $\overline{RES}$ or START command restarts the HS-82C85RH clock circuitry. PCLK is negative-edge synchronized with CLK and CLK50.

Since PCLK continues to run at the same frequency regardless of the state of the $\overline{SLO}$/FST pin, it can be used by other devices in the system which need a fixed high frequency clock. For example, PCLK could be used to clock an HS-82C54RH programmable interval timer to produce a real-time clock for the system or as a baud rate generator to maintain serial data communications during SLOW mode operation.

Clock Synchronization

The clock synchronization (CSYNC) input allows the output clocks to be synchronized with an external event (such as another HS-82C85RH clock signal). CSYNC going active causes all clocks (CLK, CLK50 and PCLK) to stop in the HIGH state.

It is necessary to synchronize the CSYNC input to the EFI clock using two flip-flops as shown in Figure 23. Multiple external flip-flops are necessary to minimize the occurrence of metastable (or indeterminate) states.

Ready Synchronization

Two RDY inputs (RDY1, RDY2) are provided to accommodate two system buses. Each RDY input is qualified by its corresponding $\overline{AEN}$ input ($\overline{AEN1}$, $\overline{AEN2}$). Reception of a valid RDY signal causes the HS-82C85RH to output READY high, informing the HS-80C86RH that the pending data transfer may be concluded (see HS-80C86RH data sheet system timing).

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY set up and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of RDY synchronization operation. When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time TR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go HIGH.

Negative-going asynchronous RDY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the RDY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing (TR1VCL) on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first RDY flip-flop is bypassed in the RDY synchronization logic. RDY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. $\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

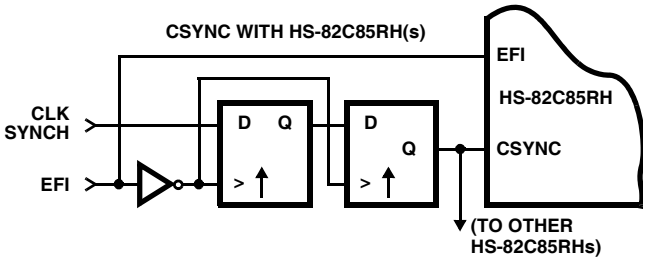


FIGURE 23. CSYNC SYNCHRONIZATION METHODS

Die Characteristics

DIE DIMENSIONS:

2770µm x 3130µm x 483µm ±25µm

INTERFACE MATERIALS:

Glassivation:

Type: SiO2
Thickness: 8kÅ ±1kÅ

Top Metallization:

Type: Al/Si
Thickness: 11kÅ ±2kÅ

Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

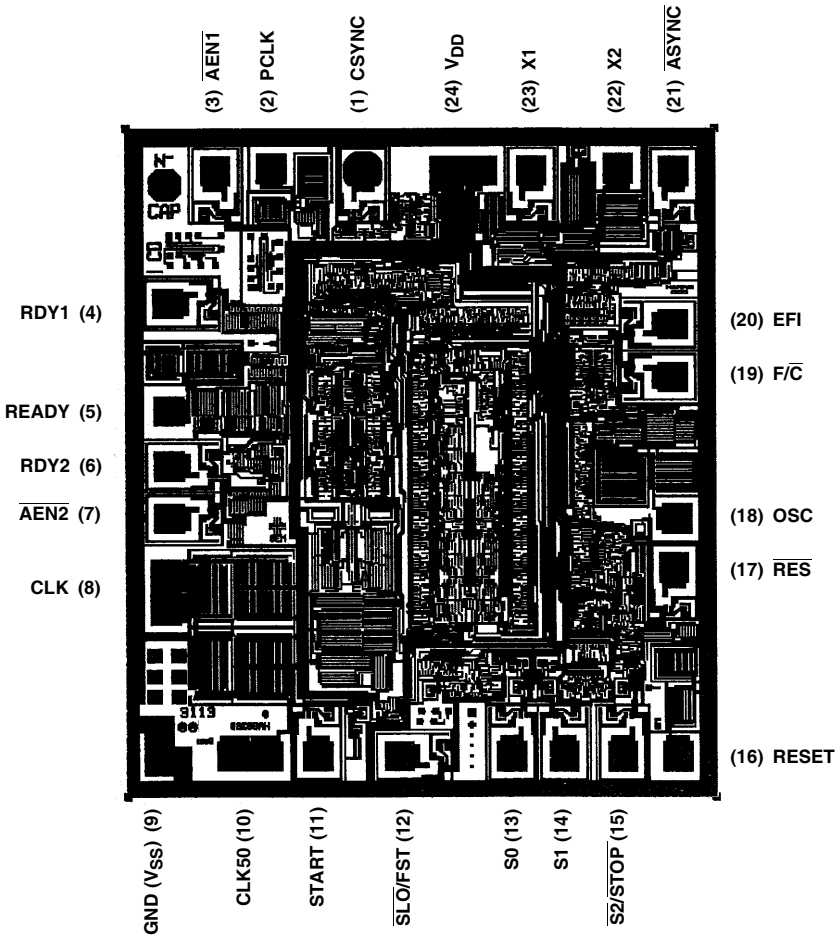
ADDITIONAL INFORMATION:

Worst Case Current Density:

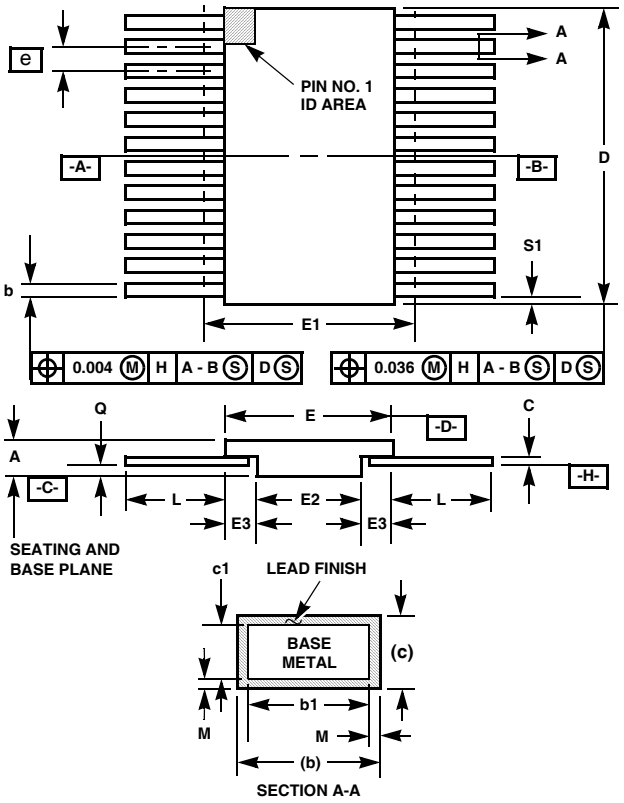
1.6×10^4 A/cm^2

Metallization Mask Layout

HS-82C85RH



Ceramic Metal Seal Flatpack Packages (Flatpack)



K24.A MIL-STD-1835 CDFP4-F24 (F-6A, CONFIGURATION B)
24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

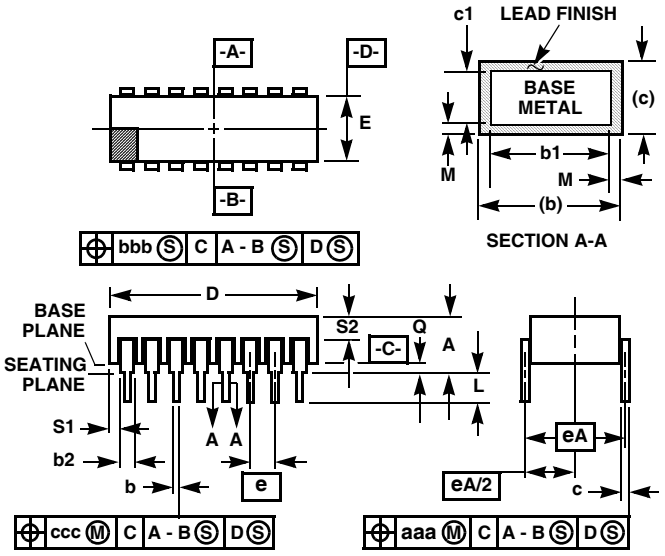
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.640	-	16.26	3
E	0.350	0.420	9.14	10.67	-
E1	-	0.450	-	11.43	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	24		24		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C)
24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

Rev. 0 4/94