TMS416100
16 777 216-BIT
DYNAMIC RANDOM-ACCESS MEMORY

SMKS610B–NOVEMBER 1990–REVISED JANUARY 1993

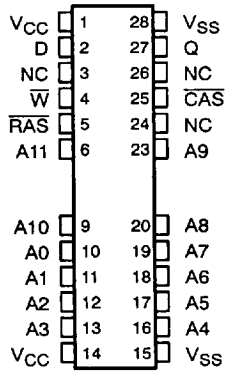
This data sheet is applicable to all TMS416100s symbolized with Revision "A" and subsequent revisions as described on page 22.

- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

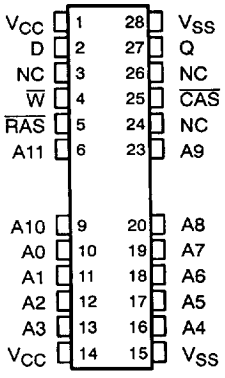
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS416100-60	60 ns	15 ns	30 ns	110 ns
TMS416100-70	70 ns	18 ns	35 ns	130 ns
TMS416100-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 4096 Cycle Refresh In 64 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range 0°C to 70°C**

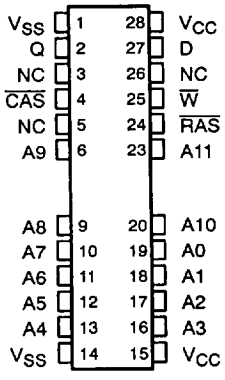
DZ PACKAGE†
(TOP VIEW)



DGC PACKAGE†
(TOP VIEW)



DGD PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

description

The TMS416100 series are high-speed, 16 777 216-bit dynamic random-access memories, organized as 16 777 216 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

All inputs, outputs, and clocks are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416100 is offered in 400-mil 24/28-pin surface mount SOJ (DZ suffix) and 400-mil 24/28-pin surface mount thin SOP (DGC and DGD suffixes) packages. This device is characterized for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
Q	Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

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operation

enhanced page mode

Enhanced page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$-low width.

The column address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS416100 to operate at a higher data bandwidth than conventional page-mode parts since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if tAA max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set up on inputs A0 through A11 and latched during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. Twelve column-address bits are set on inputs A0–A11 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the fallling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

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refresh

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. *Valid data is* maintained at the output throughout the hidden refresh cycle. An internal address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

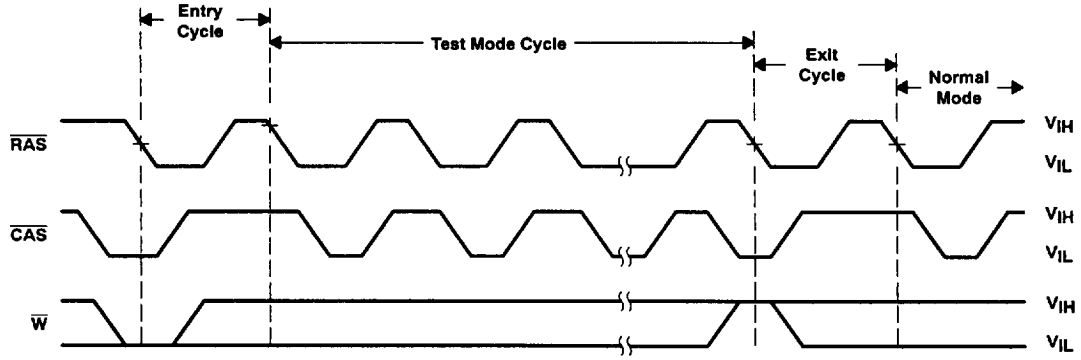
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits the test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

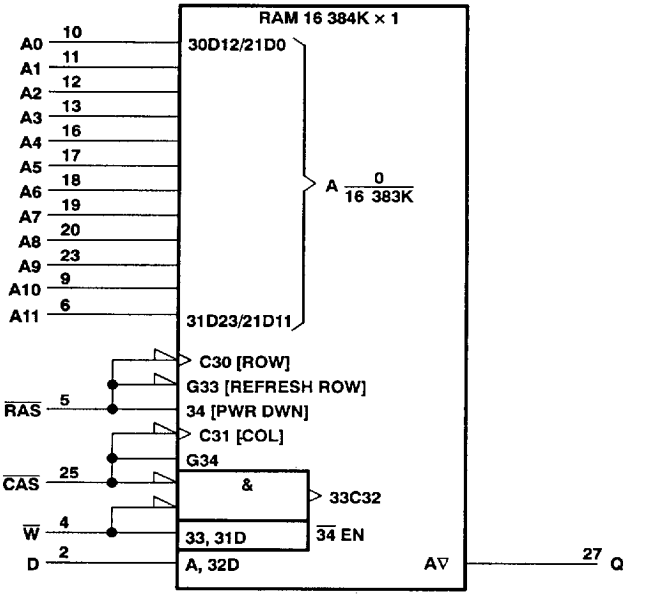
Test mode causes the part to be internally reconfigured into a 1024K × 16 bit device with 16-bit parallel read and write data path. Column addresses CA0, CA1, CA10, and CA11 are not used. During a read cycle all 16 bits of the internal data bus are compared. If all bits are the same data state, the output pin will go high. If one or more bits disagree, the output pin will go low. Test time in test mode can thus be reduced by a factor of 16, compared to normal memory mode.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

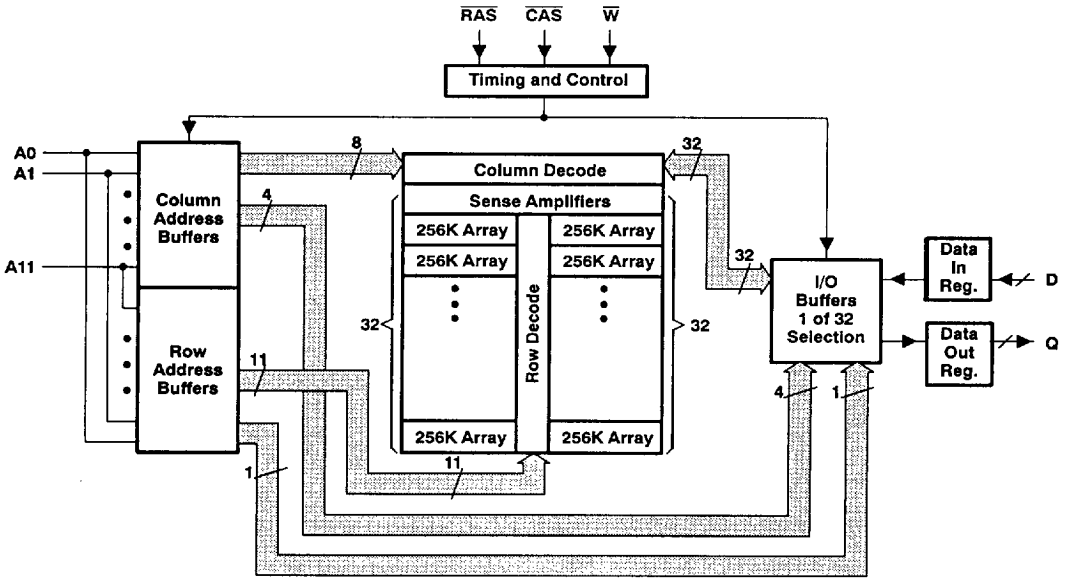
Figure 1. Test Mode Cycle†

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 24/28 pin SOJ package (DZ suffix) and the 24/28-pin thin SOP package (DGC suffix).

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note1) ..... −1 V to 7 V
Voltage range, V_{CC} ..... −1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS416100-60		TMS416100-70		TMS416100-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Notes 3 and 5)	Minimum cycle, V_{CC} = 5.5 V		90		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} −0.2 V (CMOS)		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Notes 3 and 5)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		90		80		70	mA
I_{CC4}	Average page current (see Notes 4 and 5)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50	mA
I_{CC7}	Standby current output enable (see Note 5)‡	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.
5. Measured with no load connected.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 6: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS416100-60		TMS416100-70		TMS416100-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS416100-60		TMS416100-70		TMS416100-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 8)	110		130		150		ns
t_{RWC}	Read-write cycle time	130		153		175		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	40		45		50		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 12)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns

Continued next page.

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		TMS416100-60		TMS416100-70		TMS416100-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	60		70		80		ns
t_{CPRH}	$\overline{RAS}$ hold time form $\overline{CAS}$ precharge	35		40		45		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	35		40		45		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION

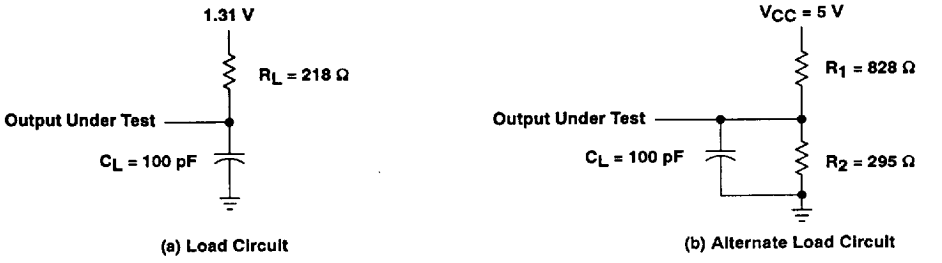
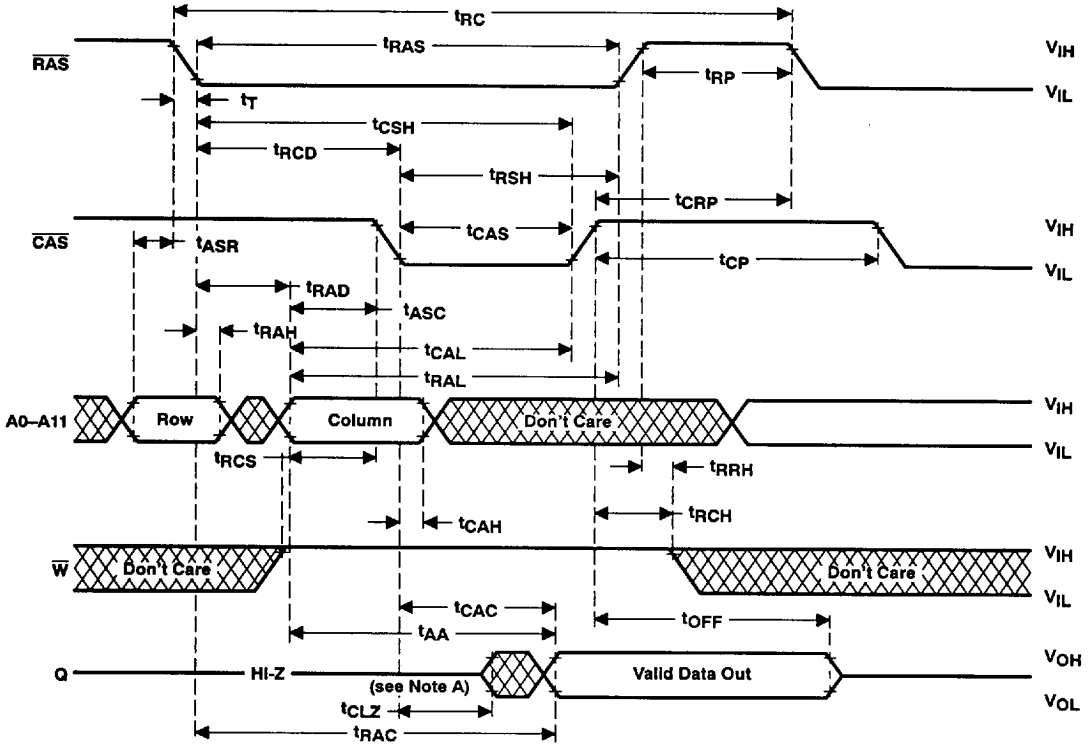


Figure 2. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

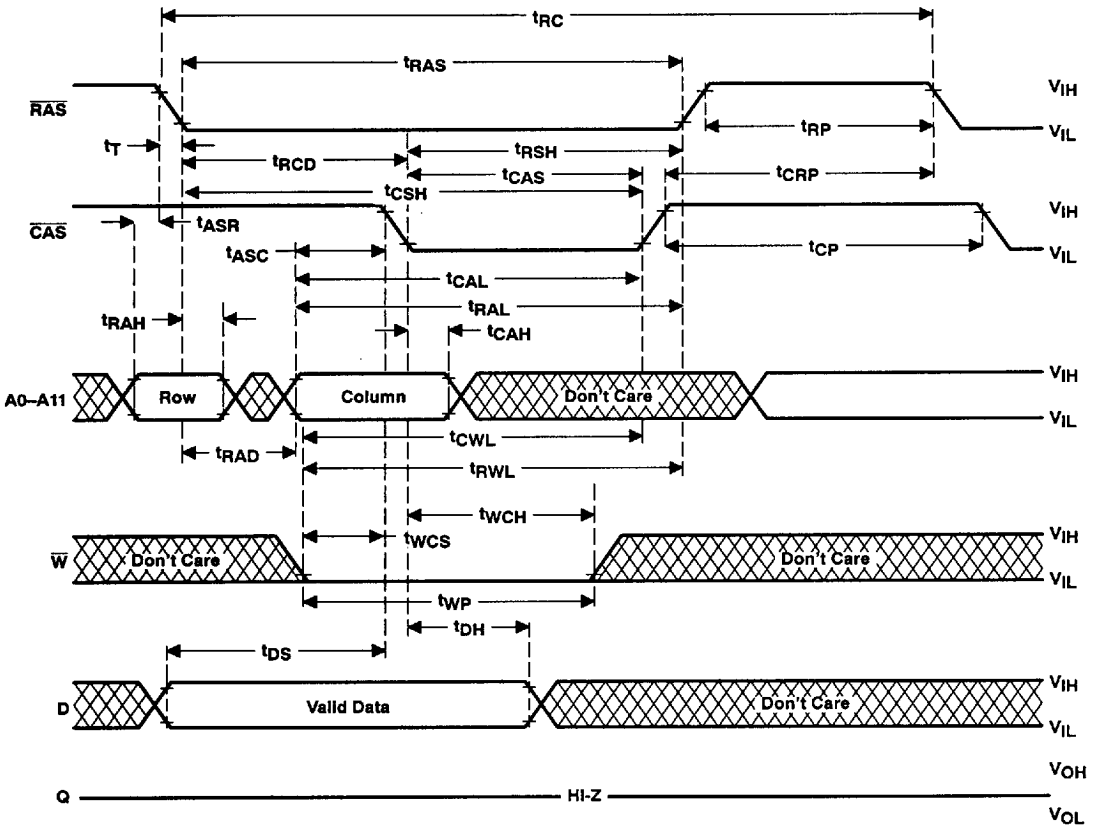


Figure 4. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

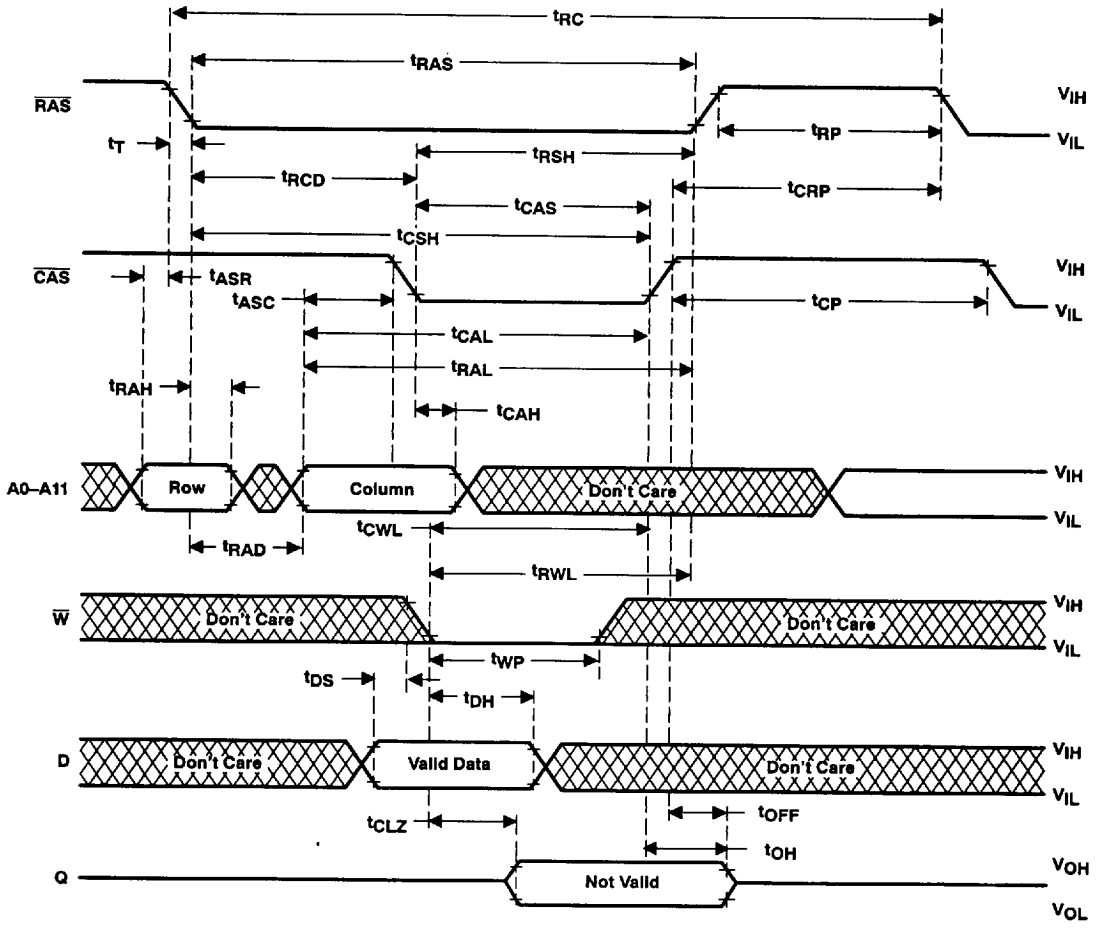
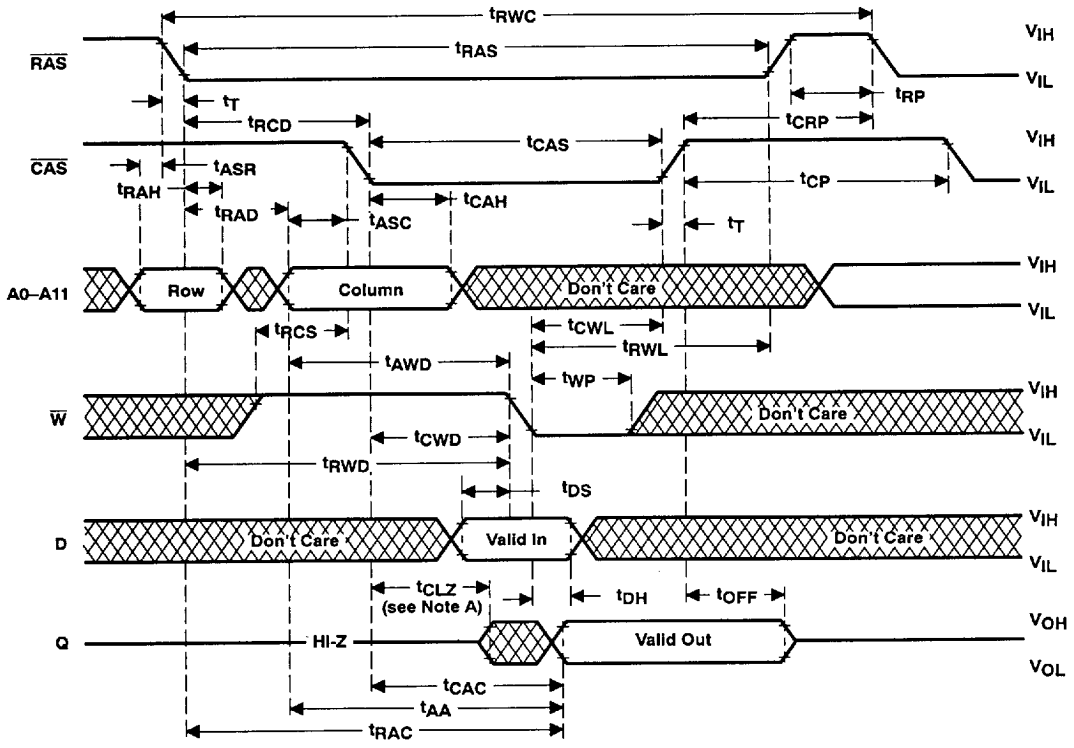


Figure 5. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write Cycle Timing

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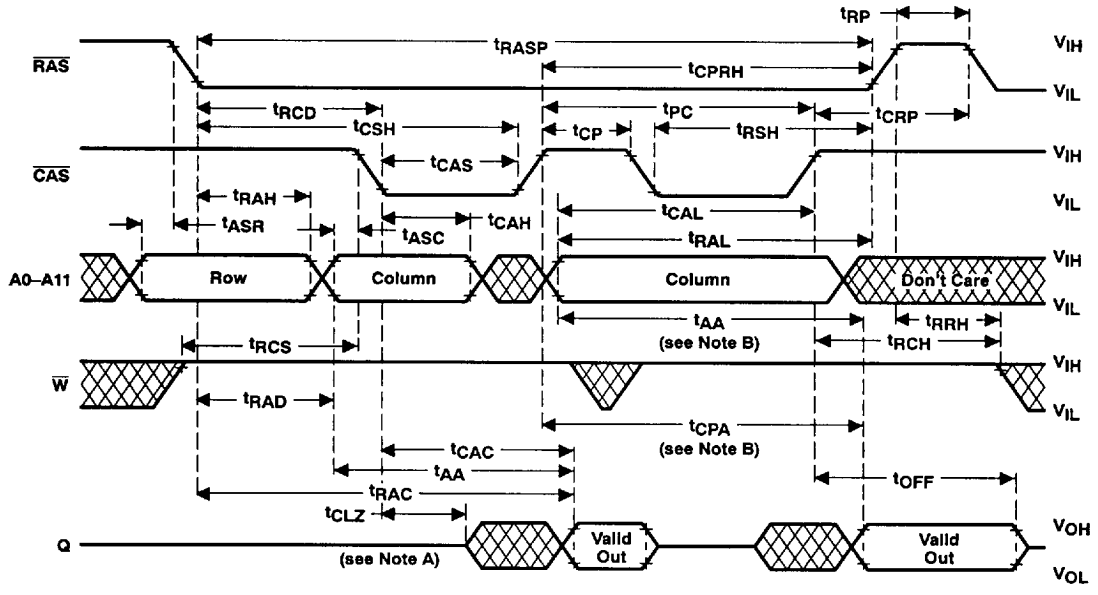
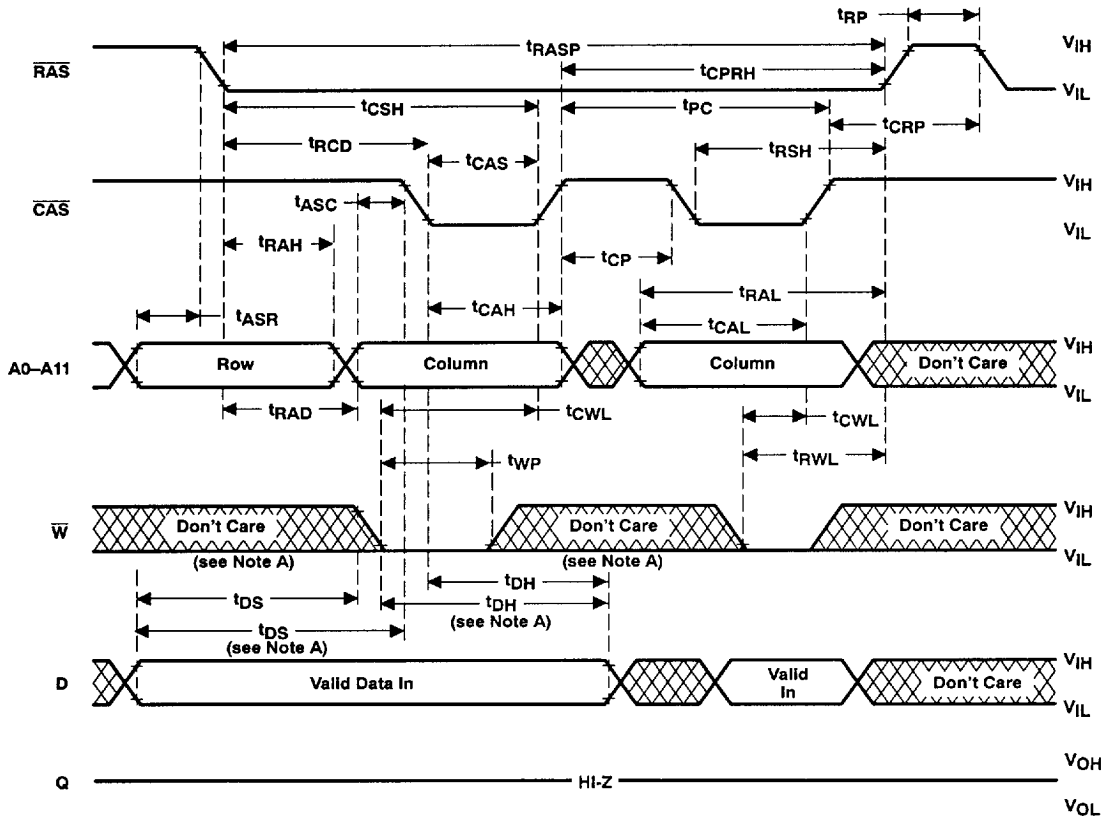
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 7. Enhanced Page-Mode Read Cycle Timing

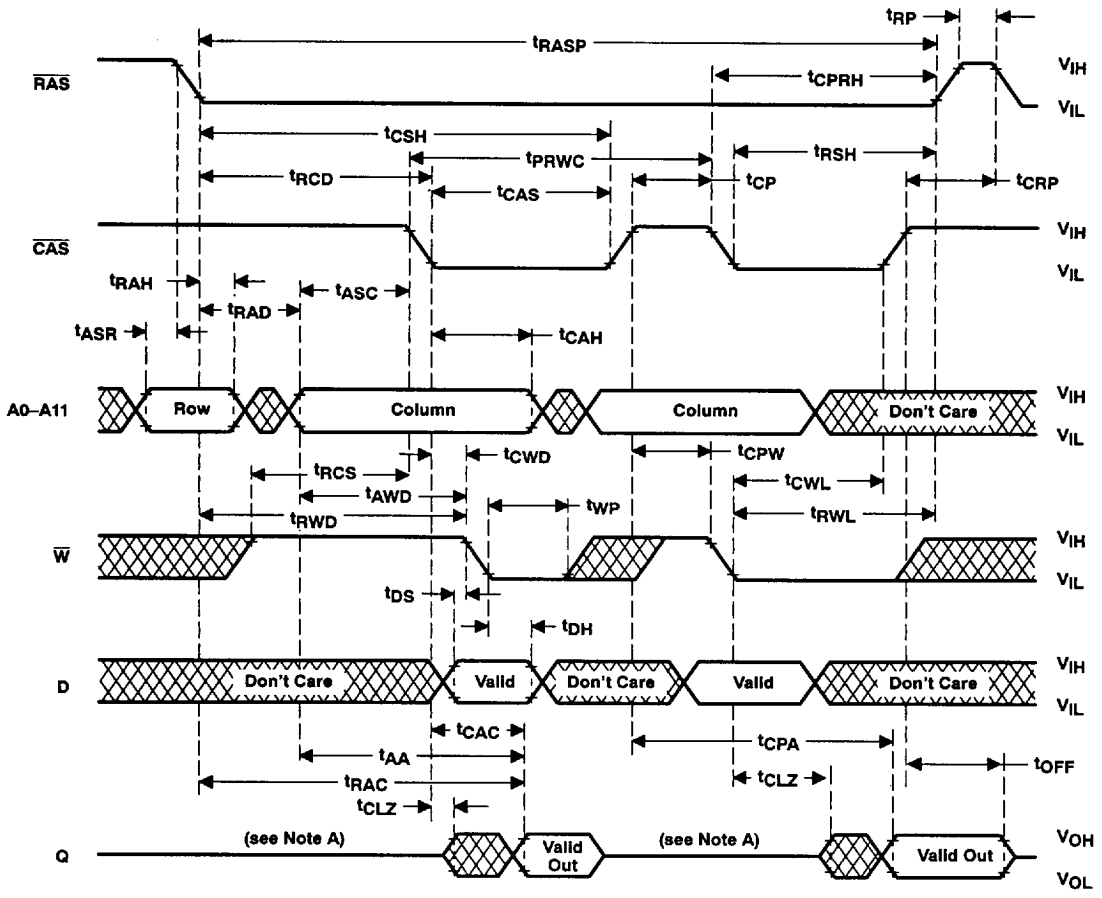
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

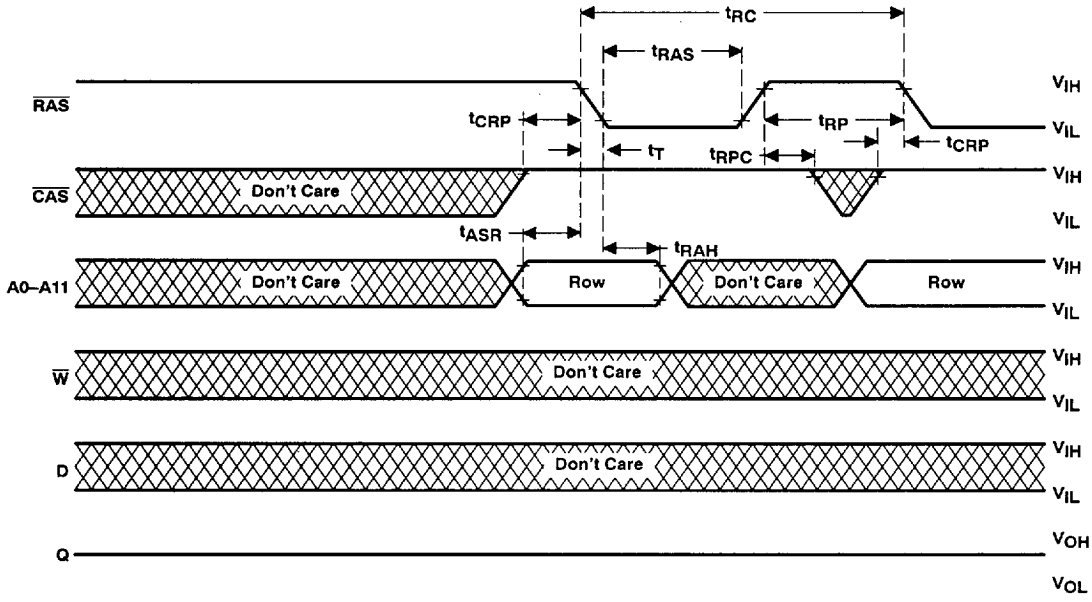


Figure 10. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

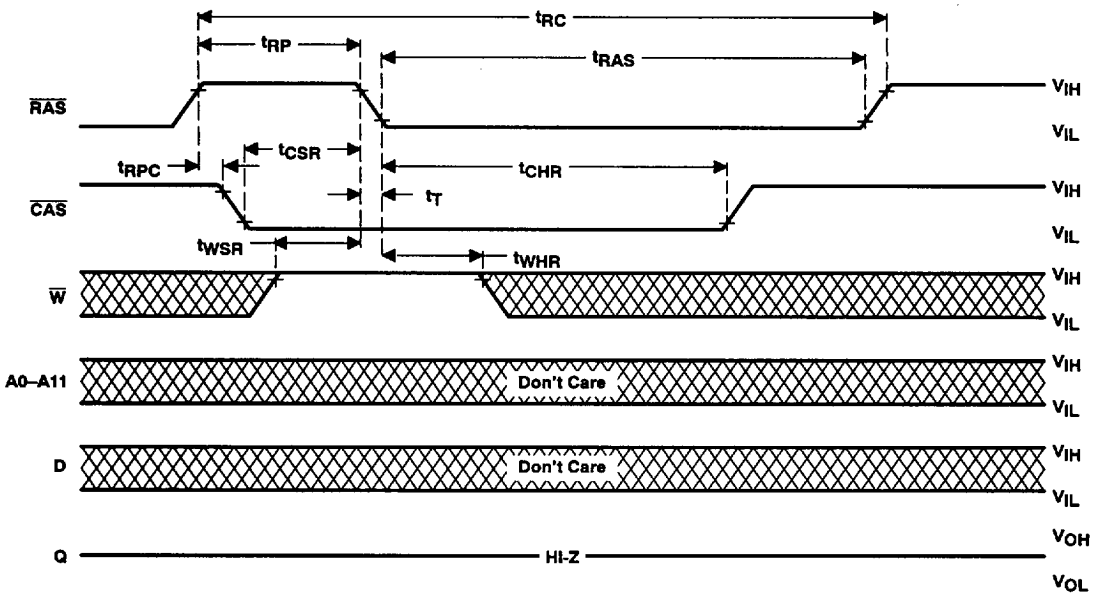


Figure 11. Automatic ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

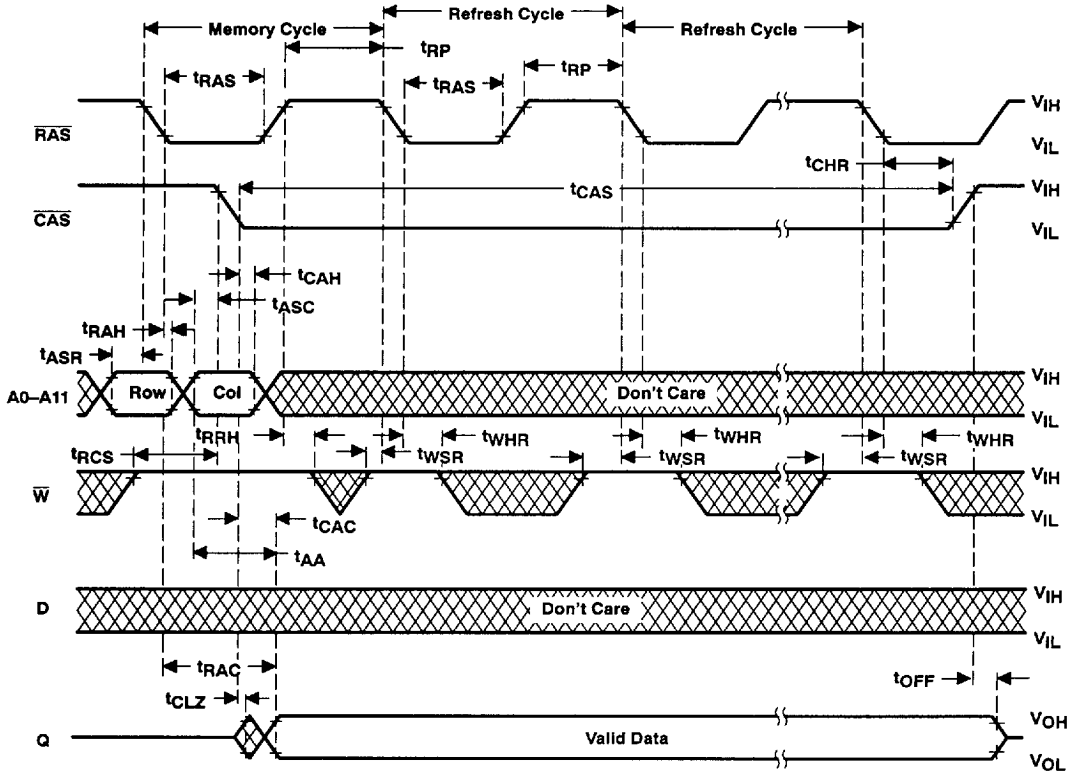


Figure 12. Hidden Refresh Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

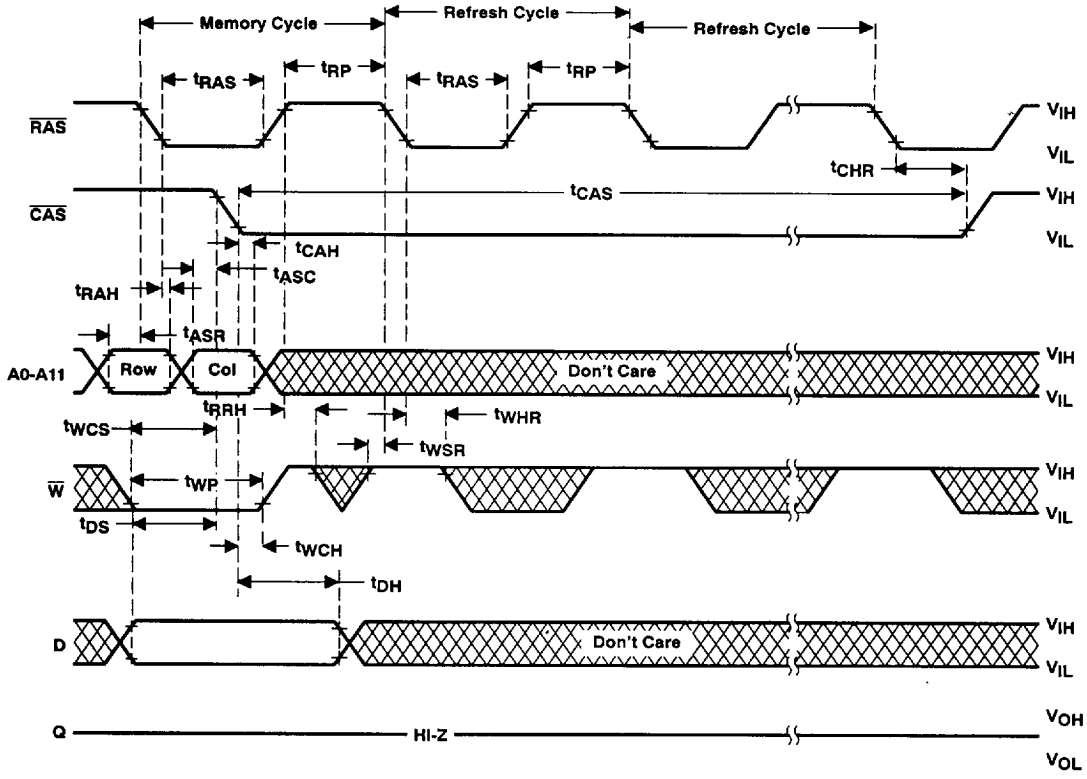


Figure 13. Hidden Refresh Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

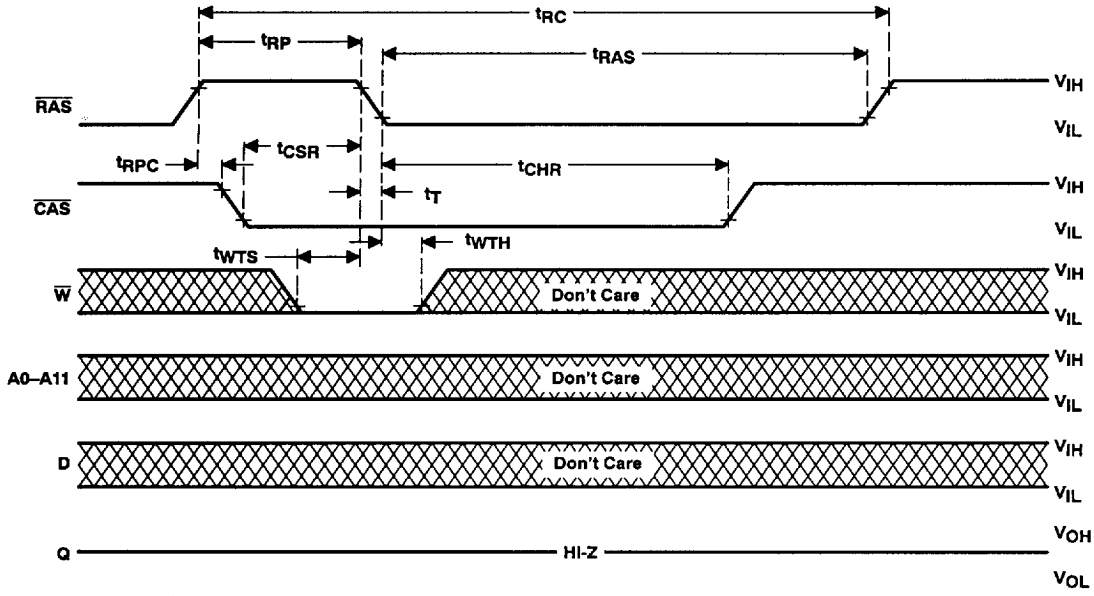


Figure 14. Test Mode Entry Cycle

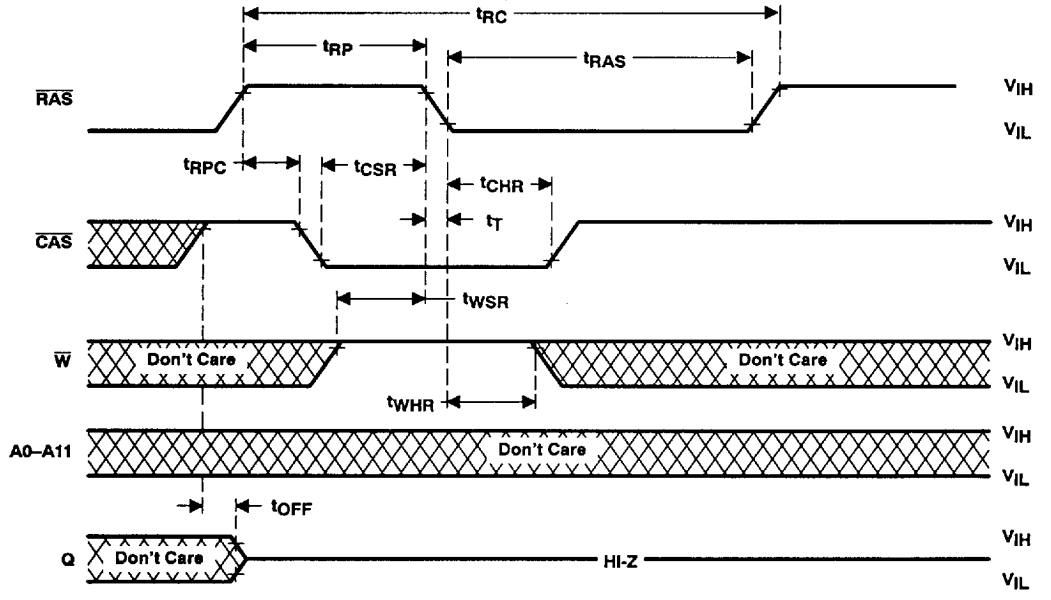


Figure 15. Test Mode Exit Cycle (CAS-Before-RAS Refresh Cycle)

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