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SSI 32H6829/6829A
Servo and Spindle Predriver

Advance Information

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DESCRIPTION

The SSI 32H6829 Servo and Spindle Predriver, a CMOS monolithic integrated circuit housed in a 64-lead TQFP package operates from +5V and +12V supplies. It is designed to drive a voice coil actuator and a 3-phase, Hall-sensorless motor with external power MOSFETs. The device is intended for use in 12V disk drive applications.

The actuator driver includes a saturation detector to monitor the loop compensation amplifier for saturation, an uncommitted opamp for input signal conditioning, a voltage reference to provide a precise voltage level for internal PWM buffers, and reduced power dissipation.

The spindle driver includes a µP controlled startup ramp to replace the imprecise analog ramp, an external PWM input to allow PWM frequencies above the audible range, active pullup on the P driver, adjustable N-channel slew rate, and improved spindle brake performance.

A precision low voltage monitor circuit is also added to monitor +5V and +12V supplies and to initiate servo head retracts during voltage faults.

The SSI 32H6829A is the SSI 32H6829 housed in a 48-lead TQFP package intended to be a drop-in, pin-for-pin replacement for the SSI 32H6825. As such the SSI 32H6829A does not implement the following functions of the SSI 32H6829: Voltage Reference, Voltage Fault, PWM Buffers, PSNS Comparator, and Dual Level Retract. Also, the 6825 $\overline{\text{WRPROT}}$ function is replaced with the similar but more useful $\overline{\text{SAT}}$ function.

FEATURES

- **Small footprint 64- or 48-lead TQFP package**
- **Spindle driver is PWM during run and start**
- **Commutator is driven by a phase lock loop for high jitter immunity**
- **Adjustable slew rate to minimize stress in the power MOSFETs**
- **Microprocessor controlled spindle startup**
- **Saturation detector to monitor loop compensation amplifier status**
- **Precision low voltage monitor circuitry for both +5V and +12V supplies, 32H6829 only**
- **Dual level retract scheme includes adjustable pulse mode, 32H6829 only**

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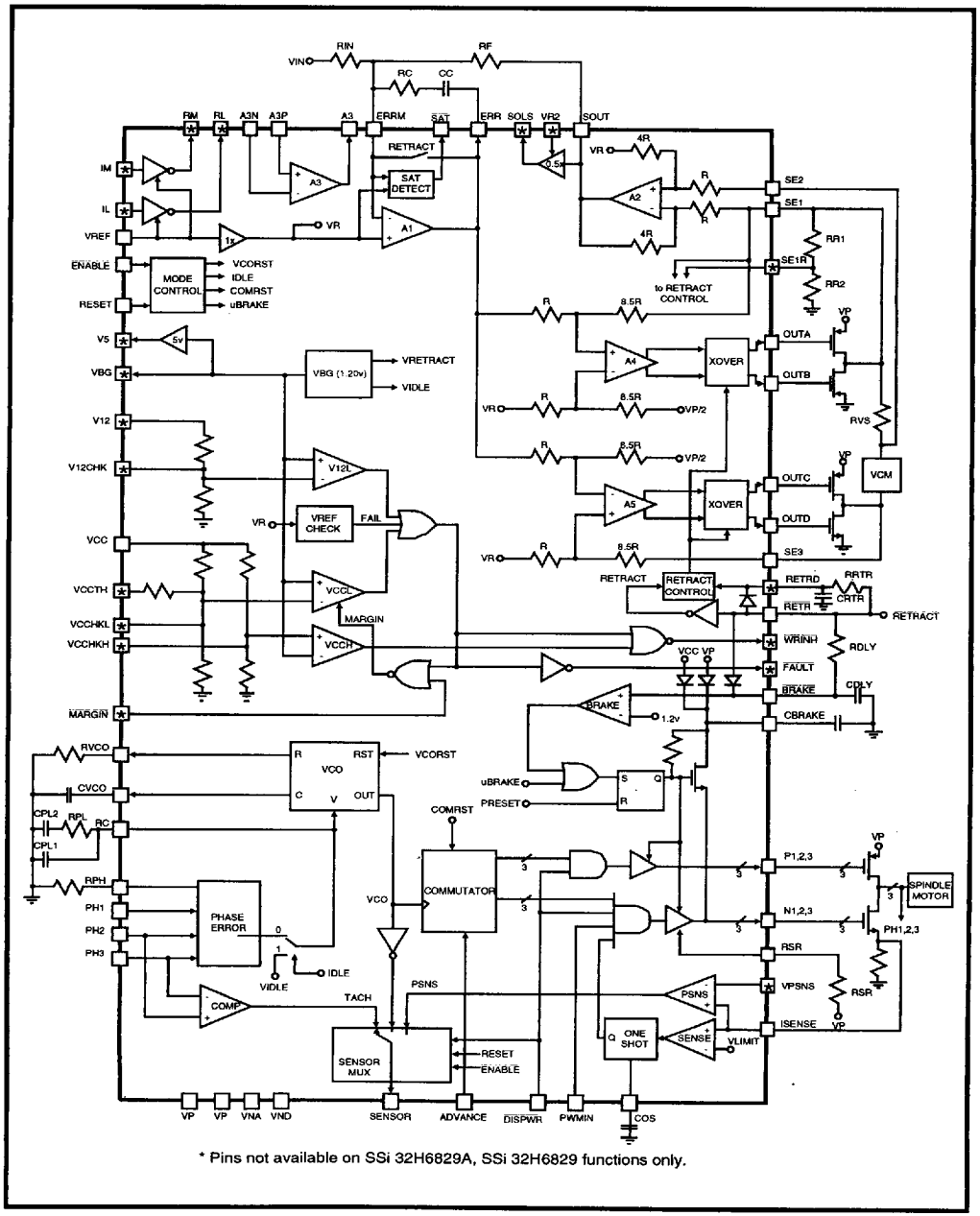
BLOCK DIAGRAM



* Pins not available on SSi 32H6829A, SSi 32H6829 functions only.

FUNCTIONAL DESCRIPTION

The SSI 32H6829 contains an actuator predriver with PWM interface, a spindle predriver with PLL commutator, and a low voltage monitor circuit.

ACTUATOR PREDRIVER

The actuator predriver serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration. It has two modes of operation, normal (linear) and retract. The retract mode is activated by an external command at $\overline{\text{RETR}}$. Otherwise, the device operates in linear mode. It consists of a 5V reference, A1 through A5, a saturation detector, and XOVER blocks. It is functionally similar to the 32H6825.

Positioner PWM Interface

The 5V voltage reference provides a precision and stable voltage source for two on-chip PWM buffers and therefore eliminates logic swing uncertainty of PWM signals. The PWM buffer outputs are then filtered by an external RC low pass network constructed with the on-chip uncommitted opamp to generate an analog input.

Loop Compensation Amplifier

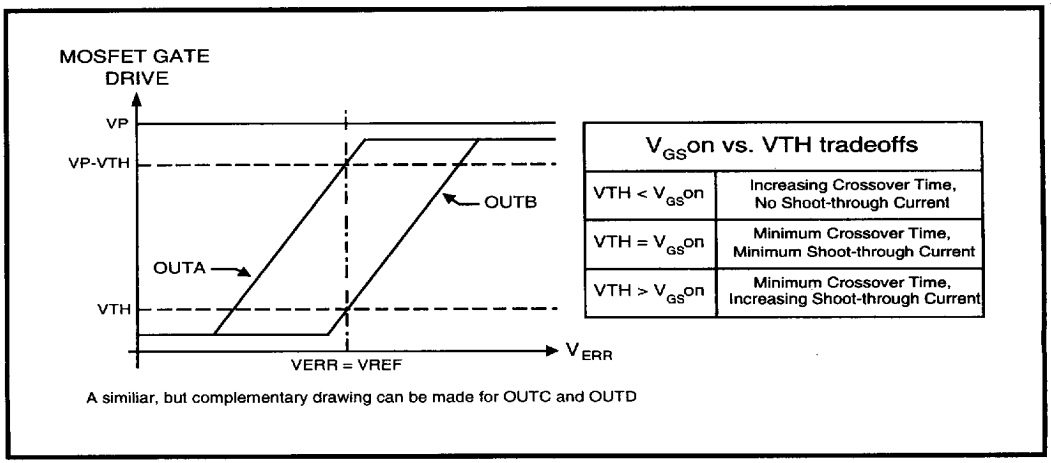
During linear operation, the acceleration signal is applied through amplifier A1. RC components may be used to provide loop compensation at this stage. The saturation detector monitors amplifier A1 and indicates when saturation is detected.

MOSFET Drivers

ERR, the output signal of A1, drives two precision amplifiers, each with a gain of 8.5. The first of these two amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed similarly from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a current sense resistor are connected in series between SE1 and SE3.

Crossover Protection Blocks

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold VTH, illustrated below, is the maximum drive on any MOSFET gate when the motor current changes sign.



V_{GS}on vs. VTH tradeoffs	
VTH < V_{GS}on	Increasing Crossover Time, No Shoot-through Current
VTH = V_{GS}on	Minimum Crossover Time, Minimum Shoot-through Current
VTH > V_{GS}on	Minimum Crossover Time, Increasing Shoot-through Current

FIGURE 1: Crossover Protection

ACTUATOR PREDRIVER (continued)

Retract Function

The 6829 incorporates a dual level retract scheme. When retract is initiated, a fixed voltage (level 1) is applied across the actuator to force a constant retract velocity. After an externally adjustable amount of time, a higher voltage (level 2) is briefly applied to the actuator. At the end of level 2, the actuator is floated (i.e., zero current).

The timing and amplitude of the level 2 phase can be adjusted with external components. RRTR, CRTR, and an internal discharge resistor which is activated during level 2 control the retract timing. When $\overline{\text{RETR}}$ is first lowered, RRTR discharges CRTR until the RETRD pin reaches the level 2 trigger threshold (nominally 0.85V). At this time, the level 2 retract amplitude is applied to the actuator and the internal discharge resistor (nominally 32k) quickly discharges CRTR. When CRTR has been discharged to half of the trigger voltage all retract current is turned off and the actuator is floated. The level 1 retract amplitude is internally fixed (0.85V nominal). During level 2, SE1R is fed back to the retract amplifier instead of SE1. Thus the level 2 amplitude will be increased by the factor (1 + RR1 / RR2).

A second external RC delay is used between $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ to program the brake delay and ensure the actuator has enough time to retract before the spindle is braked.

Current Sense Amplifier

Actuator current is sensed by a small series resistor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired current and the actual motor current. SOUT, referenced to VREF, is also connected to a level-shifter to generate SOLS, which is referenced to VR2.

PWM Inverters

Two PWM inverters powered from VREF are provided to generate power supply insensitive square waves from two pulse width modulation digital data streams. The two outputs may be weighted and summed into a low pass filter constructed with A3. To facilitate bonding to a 48-lead package, IL is pulled to ground with a 100k resistor. When the inverters are not used, IL may be floated, but IM must be tied to either ground or VREF.

SPINDLE PREDRIVER

The spindle driver section monitors spindle back-emf and generates drive signals to 3 MOSFET power bridges. It includes current limit, a back EMF monitoring circuit to determine optimal commutation points, a phase locked loop to properly phase the commutation times, and a delayed spindle brake circuit.

Commutator

The commutator drives the spindle motor windings in proper sequence to operate a 3-phase spindle motor. In run mode, the commutator is clocked by the VCO output. In start mode, the commutator is clocked by external pulses applied at the ADVANCE pin. The table below shows the commutator sequence and identifies which power FETs are on.

TABLE 1: Commutation Sequence

STATE	N1	N2	N3	P1	P2	P3
Reset	Off	On	Off	On	Off	On
A	Off	Off	On	On	Off	Off
B	Off	Off	On	Off	On	Off
C	On	Off	Off	Off	On	Off
D	On	Off	Off	Off	Off	On
E	Off	On	Off	Off	Off	On
F	Off	On	Off	On	Off	Off

Phase Error Amplifier

The phase error circuit compares the undriven winding voltage with the average of the winding voltages. Depending on the result of the comparison and the state of the commutator, a positive or negative current is applied to the RC pin. The table below shows which winding is undriven and the polarity of the output current when that winding is positive with respect to the average.

The phase error circuit is only used during run and coast modes. In all other modes, RC is forced to V_{IDLE}, an internally generated voltage that will cause the VCO to idle at approximately 1/20 of the run rate.

The magnitude of the current at RC is the sum of a constant current and a current proportional to the VCO frequency. The constant current value is set by RPH which is biased to 2.4V nominally. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on CVCO is nominally 2.0V. The frequency formula is:

$$F_{VCO} = \frac{V_{RC}}{8.0\ R_{VCO}\ C_{VCO}}$$

The VCO will be reset whenever $\overline{ENABLE}$ = High and RESET = Low. During VCO reset, the VCO output is forced low. The first VCO clock will occur immediately after the VCO exits reset. This timing relationship is shown in Figure 2.

One Shot

The one shot is triggered whenever ISENSE exceeds VLIMIT. When the one shot times out, it will remain high if ISENSE is still above VLIMIT. During the time the one shot output is high, the N drivers are turned off. This behavior implements PWM over-current limit, where the peak current is V_{LIMIT}/R_{MS}.

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TABLE 2: Undriven Winding and Polarity

COMMUTATOR	UNDRIVEN WINDING	POLARITY
A	PH2	Source
B	PH1	Sink
C	PH3	Source
D	PH2	Sink
E	PH1	Source
F	PH3	Sink

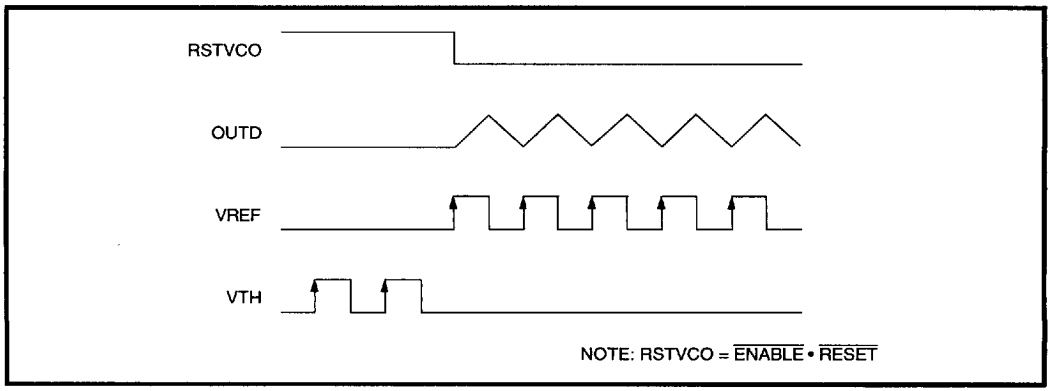

FIGURE 2: VCO Timing Diagram

SPINDLE PREDRIVER (continued)

NOUT and POUT

The NOUT drivers drive the gates of the N channel power FETs. They have an adjustable source current set by an external resistor at RSR. In brake mode, the NOUT drivers are disabled and all N channel power FETs are turned on. The POUT drivers drive the P channel power FETs. The POUT drivers are deactivated during brake but not during each PWM cycle.

Spindle Modes of Operation

The spindle driver modes of operation are governed by the RESET, $\overline{\text{ENABLE}}$, and $\overline{\text{DISPWR}}$ inputs according to Table 3. The brake mode, whether activated by $\overline{\text{ENABLE}}$ and RESET or by a power failure is internally latched and can only be turned off by asserting the preset mode.

LOW VOLTAGE MONITOR

Precision low voltage monitor circuitry is included to monitor VREF and both supplies, +5V and +12V. The circuitry includes a precision voltage reference generator, VCC reset comparator, +12V reset comparator, write inhibit comparator, and associated logic.

The voltage reference circuit generates a precision voltage reference VBG at 1.20V. From VBG, it also generates, $V_{RETRACT}$ (nominally 0.82V), V_{IDLE} (nominally 0.1V), VLIMIT (nominally 0.1V), and several other internal voltage and current references.

Both supplies are individually divided down by on-chip resistor dividers and then compared to VBG. The VCC low side monitor includes a resistor attenuator connected to VCCTH which permits the exact trip point to be externally adjusted if necessary. When a low voltage is detected on either supply, $\overline{\text{FAULT}}$ is pulled low. The threshold voltage of VCC reset comparator will be pulled to a lower value if $\overline{\text{MARGIN}}$ is asserted while $\overline{\text{FAULT}}$ is high. This allows the VCC reset comparator to be effectively disabled during power supply margin testing.

A write inhibit function is also provided by the low voltage monitor circuitry. When +5V supply is out of its specified limits or +12V supply falls below its threshold, WRINH is pulled low.

DIGITAL INPUTS

To ensure a known state during system power failure, the digital inputs at $\overline{\text{DISPWR}}$, PWMIN, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{RETR}}$ are pulled to ground with a 20 kΩ (minimum) resistor, while the digital input at $\overline{\text{MARGIN}}$ is pulled to VCC with a 20 kΩ (minimum) resistor.

TABLE 3: Spindle Modes of Operation

RESET	$\overline{\text{ENABLE}}$	$\overline{\text{DISPWR}}$	MODE	SENSOR	RC	VCO	COMMUTATOR
1	1	X	Preset	$\overline{\text{VCO}}$	V_{IDLE}	Idle	Reset
0	1	X	Start	PSNS	V_{IDLE}	Reset	Run
0	0	1	Run	$\overline{\text{VCO}}$	Run	Run	Run
0	0	0	Coast	TACH	Run	Run	Run
1	0	X	Brake	$\overline{\text{VCO}}$	V_{IDLE}	Idle	Reset

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VND, VNA	Ground	Digital and Analog Grounds. They are shorted externally.
VCC	Supply	System 5V power supply. Used by digital I/O circuits.
VP	Supply	The 12V supply, diode protected from system 12V. This is also the bridge supply for the spindle and actuator MOSFETs.

ACTUATOR PREDRIVER

VREF	Input (A)	Actuator Voltage Reference. All actuator analog signals are referenced to this voltage, except SOLS.
ERRM	Input (A)	Position Error Inverting Input. Inverting input to the loop compensation amplifier.
ERR	Output (A)	Position Error. The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3-SE1 = 17(ERR-VREF)
SOUT	Output (A)	Motor Current Sense Output. This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF = 4(SE2-SE1)
SOLS	Output (A)	Motor Current Sense Output - This output provides a voltage equal to one half of SOUT and is referenced to VR2. SOLS-VR2 = 0.5(SOUT-VREF)
VR2	Input (A)	Voltage Reference. The reference for SOLS.
$\overline{SAT}$	Output (D)	Saturation Detect Output - Active low, with an on-chip 10 kΩ pullup resistor. It is asserted when the current flowing through the summing node at ERRM exceeds the saturation detector limits.
SE2	Input (A)	Motor Current Sense Input. Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	Input (A)	Motor Voltage Sense Input. This input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor that is in series with the motor. The gain to this point from ERR is: SE1-VREF = -8.5(ERR-VREF)

ACTUATOR PREDRIVER (continued)

NAME	TYPE	DESCRIPTION
SE3	Input (A)	Motor Voltage Sense Input. This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3-VREF = 8.5(ERR-VREF)
OUTA, OUTC	Output (A)	P-FET Drive. Drive signal for a P-channel MOSFET connected between one side of the motor and VP.
OUTB, OUTD	Output (A)	N-FET Drive. Drive signal for an N-channel MOSFET connected between one side of the motor and ground. Crossover protection circuitry ensures that the P- and N- channel devices connected to the same side of the motor are never enabled simultaneously.
V5	Output (A)	5V Reference Output. The output of the 5V voltage reference.
RM, RL	Output (A)	PWM Inverter Outputs.These pins are connected to an external low pass filter network to generate the analog positioner input.
IM, IL	Input (D)	PWM Inverter Inputs. These pins are driven by PWM digital waveforms. IL is pulled down with an internal 100k resistor. IM must not float, if unused it should be tied to VREF or GND.
A3P	Input (A)	Non-inverting A3 Input. Positive input to A3, the uncommitted opamp.
A3N	Input (A)	Inverting A3 Input. Negative input to A3, the uncommitted opamp.
A3	Output (A)	A3 Output. The output of A3, the uncommitted opamp.

SPINDLE PREDRIVER

P1, P2, P3	Output (A)	P-Channel Spindle FET Drivers.These pins are connected to the three P-channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	Output (A)	N-Channel Spindle FET Drivers. These pins are connected to the three N-channel power MOSFETs in the spindle motor power bridge.
RSR	Component	Source Current Limit. An external resistor is connected between this pin and VP to set 1/20 of the peak current at N1,N2,N3.
ISENSE	Input (A)	Spindle Current Sense. Connects to the high side of the spindle current sense resistor RMS.
VPSNS	Input (A)	Sense Comparator Input. The input to the Sense comparator. The comparator output is asserted when ISENSE exceeds VPSNS.
COS	Component	One Shot Capacitor. Sets the time delay in the one shot. The one shot is clocked whenever the current in the spindle exceeds a limit controlled by RMS.

SPINDLE PREDRIVER (continued)

NAME	TYPE	DESCRIPTION
PWMIN	Input (D)	Pulse Width Modulation Input. Modulates the N-channel power MOSFETs to control spindle motor current. When low, the NMOSFETs are turned off.
$\overline{\text{DISPWR}}$	Input (D)	Disable Power. Active low, this input turns off the high and low sides of the spindle drivers. A brake command will over-ride $\overline{\text{DISPWR}}$. An internal pulldown resistor guarantees a logic low when $\overline{\text{DISPWR}}$ floats.
ADVANCE	Input (D)	Commutation Advance. A rising edge on this pin will cause the commutator to advance whenever RESET is low. While high, ADVANCE prevents other commutation clocks from occurring.
SENSOR	Output (D)	Digital MUX Output. A totem pole output, which is multiplexed from the VCO output, the TACH comparator output and the sense comparator output according to Table 3.
RVCO	Component	VCO Resistor. Sets the speed range of the VCO. The voltage at RVCO is forced to track RC.
CVCO	Component	VCO Capacitor. Sets the speed range of the VCO.
RC	Component	PLL Loop Filter. Sets the time constant for the PLL in run mode. In all other modes, it is connected to a DC voltage, VIDLE. VIDLE determines the VCO frequency at which crossover from Start to Run should occur (by lowering $\overline{\text{ENABLE}}$).
RPH	Component	Phase Error Current Set. The pump current in the phase error amplifier is the sum of the VCO current (through RVCO) and the current through RPH.
PH1, PH2, PH3	Input (A)	Spindle Motor Terminals. These pins are used to detect the phase error in the PLL.

LOW VOLTAGE MONITOR AND RETRACT

$\overline{\text{ENABLE}}$, RESET	Input (D)	Mode Controls. These inputs control the spindle modes of operation according to Table 3.
VBG	Output (A)	Bandgap Voltage Output. A voltage reference output at 1.2V. It is used internally as a reference voltage in the low voltage monitor circuitry.
VCCHKH	Input (A)	Write Inhibit Comparator Input. The input to the write inhibit comparator and the connection to a bypass capacitor. VCC is divided down at this pin by an on-chip resistor divider and then compared to VBG. If VCCHKH exceeds VBG, $\overline{\text{WRINH}}$ will be pulled low.
V12	Input (A)	System +12V Supply. The upper side connection of the resistor divider for +12V reset comparator.
V12CHK	Input (A)	+12V Reset Comparator Input. The input to the +12V reset comparator and the connection to a bypass capacitor. V12 is divided down at this pin by an on-chip resistor divider and then compared to VBG. If V12CHK falls below VBG, $\overline{\text{FAULT}}$ and $\overline{\text{WRINH}}$ are asserted.
VCCTH	Component	VCC Resistor Divider Output. The VCCHKL trip point can be adjusted by connecting an external VCC resistor divider to this pin.

LOW VOLTAGE MONITOR AND RETRACT (continued)

NAME	TYPE	DESCRIPTION
VCCHKL	Input (A)	VCC Reset Comparator Input. The input to the VCC reset comparator and the connection to a bypass capacitor. If VCCHKL falls below VBG, $\overline{\text{FAULT}}$ and $\overline{\text{WRINH}}$ are asserted.
$\overline{\text{MARGIN}}$	Input (D)	Margin Control Input. Sets the threshold voltage of VCC reset comparator. It is set high by an internal pullup resistor under normal operation. If it is asserted low externally while $\overline{\text{FAULT}}$ is high, the threshold voltage of the comparator will be lowered.
$\overline{\text{FAULT}}$	Output (D)	Power Fault. Active low, with an on-chip 10 kΩ pullup resistor. It is asserted when a low voltage condition is detected on either VREF, +5V, or +12V supply.
$\overline{\text{WRINH}}$	Output (D)	Write Inhibit. Active low, with an on-chip 10 kΩ pullup resistor. It is asserted when a low voltage condition is detected on either +5V or +12V supply or an excessive voltage condition is detected on +5V supply.
SE1R	Input (A)	Alternate SE1 connection to the retract amplifier. This input is selected during the level 2 phase of retract. An external resistor divider connected to this pin programs the retract amplitude during the level 2 phase.
RETRD	Input (A)	Delayed $\overline{\text{RETR}}$. When this input decays below the trigger level for level 2, the retract amplifier selects SE1R as the feedback instead of SE1. It also activates a pull down resistor connected to RETRD. When RETRD has decayed to 50% of the trigger level, the level 2 phase of retract is terminated.
$\overline{\text{RETR}}$	Input (D)	Retract. Active low, this digital input must be asserted by external circuitry to force an actuator retract.
$\overline{\text{BRAKE}}$	Input (A)	Brake. Active low, this input must be pulled low by external circuitry to perform a delayed brake.
CBRAKE	Component	Brake Capacitor. A large capacitor is connected to CBRAKE to provide pullup to the N-channel spindle MOSFETs during brake.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING
VP	0 to 14V
VCC	0 to 7V
IM, IL, RM, RL, V5, RVCO, CVCO, RC, RPH, PSNS, ISENSE, VREF, V12CHK	0 to 6V
N1, N2, N3, $\overline{\text{BRAKE}}$, CBRAKE, V12	0 to 15V
PH1, PH2, PH3, SE1, SE1R, SE2, SE3	-2 to VP+2
$\overline{\text{RETR}}$, $\overline{\text{DISPWR}}$, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{FAULT}}$, SENSOR, $\overline{\text{WRINH}}$, PWMIN, $\overline{\text{SAT}}$	0 to 7V
All other pins	0 to VP
Storage temperature	-45 to 165°C
Solder temperature - 10 sec duration	260°C

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RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VP	Normal Mode	9	12	13.2	V
	Retract/Brake Mode	3.5		14.0	V
VCC		4.5	5	5.5	V
VREF		4.5	5	5.2	V
VR2		2	2.49	3	V
Ambient temperature		0		70	°C
V_{RC} Dynamic Range		0	2	3	V
RVCO		11.8k	12.0k	12.2k	Ω

DC CHARACTERISTICS

VP current				40	mA
VCC current				2.5	mA
V12 current				2	mA
VR2 current	VR2 = 2.493V SOUT = 2.5V wrt VREF			0.5	mA
VREF current	SE2 = VREF			0.1	mA

ELECTRICAL SPECIFICATIONS (continued)

ACTUATOR PREDRIVER

A1, Loop Compensation Amplifier

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input bias current				100	nA
Input offset voltage				±10	mV
Voltage swing	wrt VREF	±1			V
Load resistance	wrt VREF	10			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB
Retract Switch Resistance	Retract Mode, VP > 9V			1	kΩ

A2, Current Sense Amplifier

Input Impedance	SE1	SE2 = VREF	1.5	2.4		kΩ
Input Impedance	SE2	SE1 = VREF	3.2	4.2		kΩ
Input offset voltage		SE1 = SE2 = VREF			±3	mV
Output voltage swing	V_{OH}	wrt VREF, VP≥10.3V	+3			V
	V_{OL}	wrt VREF			-3	V
Common mode range	V_{IL}				-0.2	V
	V_{IH}		VP + 0.2			V
Load resistance		wrt VREF	20			kΩ
Load capacitance					100	pF
Output impedance					25	Ω
Gain (SOUT - VREF)/(SE2 - SE1)		No DC load	3.9	4.0	4.1	V/V
Unity gain bandwidth			0.5			MHz
CMRR			55			dB
PSRR			60			dB

A3, Amplifier

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input bias current				100	nA
Input offset voltage				±10	mV
Output voltage swing V_{OL}				1.0	V
V_{OH}, wrt VP		-2.0			V
Common mode range V_{IL}				1.0	V
V_{IH}, wrt VP		-3			V
Load resistance	wrt VREF	20			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB

SOLS Output (VREF = 5V)

Output voltage swing V_{OL}	wrt VR2			-1.0	V
V_{OH}	wrt VR2	1.0			V
Input offset voltage	SOUT = VREF			±5	mV
Load resistance	wrt VR2	20			kΩ
Load capacitance				100	pF
Output impedance				200	Ω
Gain (SOLS-VR2)/(SOUT-VREF)	No DC load	0.4875	0.5	0.5125	V/V

5V Voltage Reference

Output impedance	I_{OUT} = 0 to 6mA			20	Ω
Gain V5/VBG	No DC load	4.05	4.17	4.3	V/V
Load capacitance				0.1	µF

Saturation Detector

ERRM threshold current	$\overline{SAT}$ falling				
sink		5		20	µA
source		5		20	µA
Hysteresis			2.3		µA

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ACTUATOR PREDRIVER (continued)

Actuator MOSFET Drivers

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SE3 Input impedance	to VREF	10	25		kΩ
OUTA, OUTC voltage swing	|Iout| < 1 mA	1.5		VP-1	V
OUTB, OUTD voltage swing	|Iout| < 1 mA	1		VP-1.5	V
VTH, crossover threshold				1.6	V
Slew rate, OUTA..D	CL < 1000 pF	0.5			V/µs
Crossover time	±300 mV step at ERR			5	µs
Output impedance, OUTA..D			80		kΩ
Transconductance I(OUTA..D)/(ERR-VREF)			8		mA/V
Gain (SE3-SE1)/(ERR-VREF)		16	17	18	V/V

Retract Circuit

Retract voltage, $V_{RETRACT}$	VP > 5V, level 1	0.7	0.82	1.0	V
RETRD discharge resistor	VP > 5V, level 2	22	32	42	kΩ
RETRD trigger voltages					
VT1: level 1 to level 2	VP > 5V, level 1	0.75	0.85	0.95	V
VT2: level 2 to float	VP > 5V, level 2	45	50	55	%
RETRD input bias current	level 1			100	nA
SE1R input bias current				100	nA

VREF Monitor

VREF fail threshold	VREF falling	1.4	1.55	1.7	V
Hysteresis			85		mV

PWM Buffers

ROUT	Pch				15	Ω
ROUT	Nch				15	Ω
IL pull down resistor				100		kΩ

SPINDLE PREDRIVER

VCO (Unless otherwise specified: C_{VCO} = 0.01 µF, R_{VCO} =12 kΩ)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Typical frequency			$\frac{V_{RC}}{8.0\ R_{VCO}\ C_{VCO}}$		Hz
Run Frequency	V_{RC} = 2V	1925	2145	2420	Hz
Idle Frequency	Mode = Reset	70		180	Hz
Reset Phase Error	V_{RC} = V_{IDLE}			18	deg

Phase Error Amplifier (Unless otherwise specified: R_{VCO} = 12 kΩ, R_{RPH} = ∞)

V_{RC}(V_{IDLE})	Mode = Reset		100		mV
Pump Current at RC					
Start Mode	V_{RC} = V_{IDLE}, R_{RPH} = ∞		4.5		µA
Run Mode, at speed	V_{RC} = 2V		82		µA
Source/Sink Current Mismatch	V_{RC} = 2V			5	%
PH1 Input Offset, State B	PH2 = VP, PH3 = 0	-100		100	mV
PH1 Input Offset, State E	PH2 = 0, PH3 = VP	-100		100	mV
PH2 Input Offset, State A	PH1 = VP, PH3 = 0	-100		100	mV
PH2 Input Offset, State D	PH1 = 0, PH3 = VP	-100		100	mV
PH3 Input Offset, State F	PH1 = VP, PH2 = 0	-100		100	mV
PH3 Input Offset, State C	PH1 = 0, PH2 = VP	-100		100	mV
RPH Voltage	R_{RPH} = 120 kΩ		2.4		V

Motor Current Control

ISENSE threshold (VLIMIT)		95	100	105	mV
One shot off time	Cos = 0.002 µF	10	25	40	µs

Braking Circuit

$\overline{\text{BRAKE}}$ threshold	VP = 4V	1.0		1.4	V
$\overline{\text{BRAKE}}$ VP threshold	$\overline{\text{BRAKE}}$ = 1.6V			3.8	V
Bias current at $\overline{\text{BRAKE}}$				0.1	µA
CBRAKE current - run	Run mode, CBRAKE = VP			2	µA
CBRAKE current - brake	Brake mode, VP = 0, CBRAKE = 10V			0.2	µA

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SPINDLE PREDRIVER (continued)

NMOS Motor Driver Outputs (N1, N2, N3)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Source current	V_{OUT} = 4V, R_{RSR} = 50 kΩ	3		6	mA
	V_{OUT} = 4V, R_{RSR} = 100 kΩ	2		4	mA
Sink current	V_{OUT} = 4V	9		35	mA
Output Low voltage	I_{SINK} = 5 mA			1	V
Output High voltage, wrt VP	I_{SOURCE} = 0.1 mA	-2.5			V

PMOS Motor Driver Outputs (P1, P2, P3)

Source current	Vout = VP - 4V	20			mA
Sink current	Vout = VP - 4V	9		35	mA
Output Low voltage	Isink = 1 mA			1.5	V
Output High voltage, wrt VP	Isource = 5 mA, V_N = 6V	-1			V

TACH Comparator

SENSOR rising edge threshold	PH3 - PH2	30	100	170	mV
SENSOR falling edge threshold	PH2 - PH3	30	100	170	mV

SENSE COMPARATOR

Input voltage offset	VPSNS = 0.1V			±10	mV

VOLTAGE FAULT MONITOR

VBG Output

Output voltage	No DC Load		1.20		V
Load capacitance				0.1	µF

VCC Reset Comparator

Trip voltage, regular mode (VCC falling, $\overline{MARGIN}$ = VCC)	VCCTH = VCCHKL	4.26	4.35	4.44	V
	VCCTH = 0	4.635	4.74	4.843	V
	VCCTH = VCC	3.493	3.57	3.647	V
Trip voltage reduction (VCC falling, $\overline{MARGIN}$ = 0)		10	14	16	%
Hysteresis		30	40	50	mV
Input resistance at VCCTH		90	140	250	kΩ

VCC Write Inhibit Comparator ($\overline{MARGIN}$ = High)

Trip voltage	VCC rising	5.64	5.82	6.00	V
Hysteresis		60	80	100	mV
Input resistance at VCCHKH			13		kΩ

+12V Reset Comparator ($\overline{\text{MARGIN}}$ = High)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Trip voltage	V12 falling	9.20	9.50	9.80	V
Hysteresis		60	80	100	mV
Input resistance at V12CHK			14		kΩ

DIGITAL I/O

Digital Input ($\overline{\text{DISPWR}}$, PWMIN, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{RETR}}$)

Input voltage	V_{IL}		0.8			V
	V_{IH}				2.0	V
Input bias current	I_{IH}	Vin = 0.5V			300	µA
Open circuit voltage					0.4	V

Digital Input ($\overline{\text{MARGIN}}$)

Input voltage	V_{IL}		0.8			V
	V_{IH}				2.0	V
Input bias current	I_{IL}	V_{IN} = 0.5V			300	µA
Open circuit voltage			2.4			V

Digital Output (SENSOR)

Output voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 1 mA	-1			V

Digital Output ($\overline{\text{FAULT}}$)

Output voltage	V_{OL}	I_{SINK} = 8 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-2	-1.0		V

Digital Output ($\overline{\text{WRINH}}$, $\overline{\text{SAT}}$)

Output voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-2.0	-1.0		V

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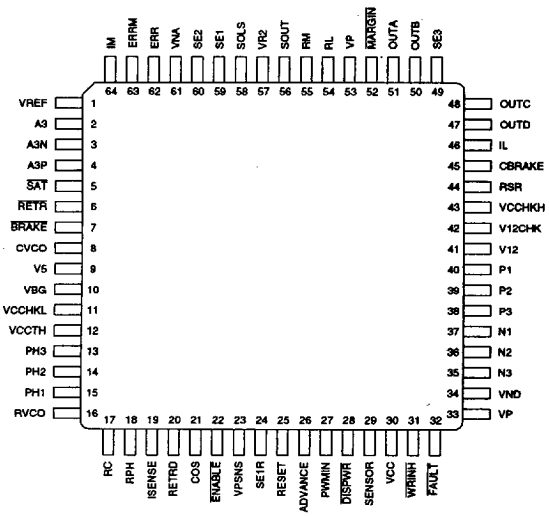
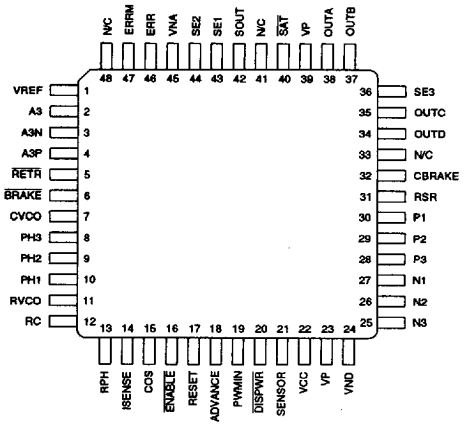
SSI 32H6829/6829A
Servo and
Spindle Predriver

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32H6829
64-Lead TQFP



32H6829A
48-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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